Capital University of Science and Technology

Department of Computer Science

CS2513 - Digital Logic Design

Course Title:	Digital Logic Design (CS2513)
Pre-requisite(s):	None
Credit Hours:	3
Instructor(s):	
Text Book(s):	• Digital Design, Authors: Morris Mano, Michael D. Ciletti, 6th Edition.
Reference Book(s):	• Digital Fundamentals, Author: Thomas L Floyd, 11th Edition. • Logic And Computer Design Fundamentals, Authors: Morris Mano, Charles Kime, Tom Martin, 5th Edition.
Web Reference:	• https://circuitverse.org/simulator [Circuit simulator]

Course Introduction:

Digital Logic Design is a core course of the BS CS program. This course introduces the basic concepts behind digital logic and design methodology. From an introduction to logic gates and circuits, the course will lead to the design of logic systems, many of which are the building blocks that modern computers and machines are comprised of. The course has an associated lab where students will get hands on experience in building digital systems, and will understand how real-world problems can be solved using digital machines.

Course Objectives:

• Describe and identify fundamental concepts of digital logic design including basic and universal gates, number systems, binary coded systems, basic components of combinational and sequential circuits

- Transform the acquired knowledge to apply techniques related to the design and analysis of digital electronic circuits including Boolean algebra and multi-variable Karnaugh map methods
- Analyze small-scale combinational and sequential digital circuits
- Design small-scale combinational and synchronous sequential digital circuit using Boolean algebra and K-maps

Course Learning Outcomes (CLOs):

At the end of this course, the students should be able to:

CLO1: Explain fundamental concepts of digital logic design including basic and universal gates, number systems, binary coded systems, basic components of combinational and sequential circuits (Level: C2-Understand)

CLO2: Demonstrate the acquired knowledge to apply techniques related to the design and analysis of digital electronic circuits including Boolean algebra and multi-variable Karnaugh map methods (Level: C3- Apply)

CLO3: Analyze small-scale combinational and sequential digital circuits (Level: C4)

CLO4: Design small-scale combinational and synchronous sequential digital circuit using Boolean algebra and K-maps (Level: C6)

CLOs – PLOs Mapping:

	CLO:1	**CLO:2**	**CLO:3**	**CLO:4**
PLO:1 (Academic Education)				
PLO:2 (Knowledge for Solving Computing Problems)	√	√		
PLO:3 (Problem Analysis)			√	
PLO:4 (Design/Development of Solutions)				√
PLO:5 (Modern Tool Usage)				

Course Contents:

Week	Contents
1	Introduction, Digital Systems, Binary Numbers Number-Base Conversions, Octal and Hexadecimal Numbers
2	Complements of Numbers, Signed Binary Numbers Binary Codes, Binary Storage and Registers, Binary Logic
3	Digital logic gates, Boolean Postulates Boolean Functions and their Complements
4	Sum of MinTerms Product of MaxTerms
5	Standard forms, SOP (Sum of Products), POS (Product of Sums)
6	Karnaugh Maps, Two Variable Maps Three Variable Maps, Four Variable Maps
7	Don't care conditions Digital Circuits using Gates
8	Digital Circuits using NAND gates Combinational Logic, Analysis and Design, Code Converters
Mid-Term Exam	
9	Half Adder, Full Adder Binary parallel Adder, CLA
10	Multiplier, Decoders Encoders, Multiplexers, Demultiplexers
11	Sequential Circuits, Latches SR latch with NOR gate, SR latch with NAND gate, D-latch

12	Flip Flops (D Flip Flop, JK Flip Flop, T Flip Flop) Characteristic Tables, Characteristic Equations.
13	Analysis of Clocked Sequential Circuits (State Equations, State Tables, State Diagrams)
14	Simple registers, Registers with parallel Load Shift Registers/Serial to parallel Converters
15	Universal Shift Register, Asynchronous counters Synchronous Counter, Ripple Counters
16	Binary Counter, BCD Counter, Up-Down Binary Counter.

Grading Policy:

S.No	Grading	% of Total Marks
1	Assignments	20
2	Quizzes	20
4	Mid-term Exam	20
5	Final Exam	40
	Total	**100**