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A Novel Hybrid HVDC Circuit Breaker Topology with Minimized Current Interruption Time and Regeneration Capability

by

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Dedicated To My Beloved Parents,

Muhammad Mansha Sahi & Naseem Akhtar

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This is to certify that the research work presented in the dissertation, entitled "**A Novel Hybrid HVDC Circuit Breaker Topology with Minimized Current Interruption Time and Regeneration Capability**" was conducted under the supervision of **Dr. Imtiaz Ahmed Taj**. No part of this dissertation has been submitted anywhere else for any other degree. This dissertation is submitted to the **Department of Electrical & Computer Engineering, Capital University of Science and Technology** in partial fulfillment of the requirements for the degree of Doctor in Philosophy in the field of **Electrical Engineering.** The open defence of the dissertation was conducted on **March 14, 2025**.

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It is certified that the following publication(s) have been made out of the research work that has been carried out for this dissertation:

Journals:

1. **Q. Arooj**, I. A. Taj, "A hybrid multi-port HVDC circuit breaker that improves interruption and reset time through shared energy dissipation and fault current regeneration," *Results in Engineering*, vol. 23, 102701, 2024.

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1. **Q. Arooj**, U. A. Khan, "An improved hybrid dc circuit breaker with battery banks for energy storage in HVDC system," *19th International Bhurban Conference on Applied Sciences and Technology (IBCAST)* pp. 603–608, 2022.
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Abstract

High-voltage direct current (HVDC) transmission systems present a cost-effective solution to the global energy crisis. However, protecting these systems is particularly challenging due to absence of current zero-crossings, which complicates fault current interruption. The low line impedance of direct current systems causes fault currents rise abruptly, necessitating rapid fault interruption to fully leverage the benefits of multi-terminal direct current (MTDC) networks. Despite their advantages, the MTDC systems have been hindered by the lack of an efficient direct current circuit breaker (DCCB). The available circuit breakers face limitations such as prolonged fault current interruption times, substantial fault energy dissipation, delayed reset times, large physical sizes, and high operational costs.

Aimed at addressing the challenges mentioned above based on a comprehensive review of existing literature, this research first deals with the problem of large fault energy dissipation in the MTDC systems by proposing two hybrid DCCB topologies: modular hybrid DCCB with fault current self-adaptive control and protective coordination (MHDCCB) and improved hybrid DCCB with battery banks for energy storage (HDCCB). The proposed MHDCCB uses a two-stage current limiting mechanism for effective fault management, while the improved HDCCB uses a resistor-inductor-capacitor resonance to create current zero-crossings and store inductive energy from network faults in battery banks for future use. Simulation results show that battery banks effectively store charge during fault events, but increased system cost due to occasional faults and battery degradation and remaining unused the rest of the time are major setbacks of these topologies.

To address the limitations of installing battery banks for breakers' energy storage after fault interruption, further research is being conducted, and a novel regenerative hybrid high-voltage direct current circuit breaker (HDCCB) and a hybrid multi-port direct current circuit breaker (HMPDCCB) topologies are proposed. These breakers aim to use fewer controlled switches, simplifying control algorithms and integrating current commutation stages to reduce fault current magnitude before interruption. The regenerative HDCCB topology has four operational stages: a normal operation, a current

commutation to prevent long-term arc generation, a primary current limiting to control fault current rise, and a current regeneration stage to recover fault energy. The HMPDCCB topology employs a shared main breaker branch for fault energy dissipation at multiple transmission lines, significantly reducing the breaker size and the overall cost. A simplified controller monitors the voltage across current-limiting inductors (CLIs) in the transmission lines to identify fault lines, using a port with minimum voltage as the receiving port for regenerated energy. The HMPDCCB delivers selective protection for all connected direct current lines, incorporating CLIs to manage fault current surges while keeping costs low. The proposed circuit breaker topologies deploy insulated gate bipolar transistors (IGBTs) and thyristors, which offer turn-on times in the nanosecond and microsecond, respectively. The simplified control scheme and fewer components in the HDCCB enable quick fault current interruption, minimizing the energy dissipation pressure on surge arresters.

The proposed regenerative HDCCB and HMPDCCB designs were modelled and simulated using MATLAB Simulink®/Simpowersystems and rigorously analysed through current, voltage, and energy analysis, confirming their capability to deliver rapid fault current interruption and quick reset times. The simulation results demonstrate that the proposed HDCCB and HMPDCCB topologies achieve fault current interruption times of 2ms and 1.8ms, reset/recovery times of 5ms and 3ms, and regenerate fault energy of 1.5MJ and 0.35MJ, respectively. In addition, the proposed topologies support bi-directional fault current interruption, making them promising candidates for enhancing the reliability and cost-effectiveness of the HVDC systems. Furthermore, in comparison with the existing work, the proposed HDCCB and HMPDCCB outperform some of the state-of-the-art circuit breaker models in the literature.

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Abbreviations

AC	Alternating current
ACCB	Alternating current circuit breaker
ABB	ASEA Brown Boveri
BBCS	Battery bank charging stage
CB	Circuit breaker
CFC-IHCB	Current flow controller integrated with hybrid DC circuit breaker
CIGRE	Council on large electric systems
CHIL	Controller hardware-in-the-loop
CLI	Current limiting inductor
CCM	Current commutation module
DCCB	Direct current circuit breaker
DC	Direct current
EAB	Energy absorption branch
EMF	Electromotive force
FACTS	Flexible AC transmission system
FB	Freewheeling branch
FCL	Fault current limiter
HCB	Hybrid circuit breaker
HDCCB	Hybrid high-voltage direct current circuit breaker
HMPDCCB	Hybrid multi-port DC circuit breaker
HVAC	High-voltage alternating current
HVDC	High-voltage direct current
HVSS	High-voltage solid-state switches
IEGT	Injection-enhanced gate transistor

IGBTB	Insulated-gate bipolar transistor
LCC	Line commutated converters
LCS	Load commutation switch
LVDC	Low-voltage direct current
MBB	Main breaker branch
MCB	Mechanical circuit breaker
MHCB	Multi-port hybrid DC circuit breaker
MHDCCB	Modular hybrid direct current circuit breaker
MMC	Modular multi-level converter
MOV	Metal oxide varistor
MS	Main selector
MTDC	Multi-terminal direct current
PCLS	Primary current limiting stage
SiC JFET	Silicon carbide junction field-effect transistor
SM	Sub-module
SSCB	Solid-state circuit breaker
UFD	Ultra-fast disconnector
VCB	Vacuum circuit breaker
VSC	Voltage source converter
WG	Working group
ZSCB	Z-source circuit breaker

Symbols

A	Ampere
kA	Kiloampere
V	Volt
kV	Kilovolt
Ω	Unit of resistance
J	Joule
MJ	Mega Joule
H	Henry
mH	Millihenry
W	Watt
MW	Megawatt
s	Second
ms	Millisecond
ns	Nanosecond
ps	Picosecond
Hz	Hertz
kHz	Kilohertz
km	Kilometer
R	Resistor
R_{lim}	Limiting branch resistor
R_L	Load resistor
C	Capacitor
C_{eqn}	Equivalent capacitor
C1 & C2	Capacitor 1 and 2

L	Inductor
L_{eqn}	Equivalent inductor
L_{lim}	Limiting branch inductor
S1 & S2	Mechanical switches 1 and 2
D1 & D2	Freewheeling diodes 1 and 2
T1, ..., Tn	Thyristors 1 to n
T_1', ..., T_n'	Complement thyristors 1 to n
ON	Turn-on time
OFF	Turn-off time
T_{trip}	Current breaking time
T_{off}	The switching delay
$N_{SM-IGBT}$	Number of parallel branches
$M_{SM-IGBT}$	Number of IGBTs
α	Damping frequency
ω	Resonance frequency
β	Ringing frequency
ω_r'	Resonant frequency
I	Current
I_{dc}	Current rated
I_L	Current across the inductor
i_{load}	Current across the load
$i_s(t)$	Source current
$i_2(p)$	Regenerated current
I_o	Source current before trip starts
$I_R(average)$	Average regenerated current
$I_{\text{fault}_{(t_1)}}$	Fault current at time t_1
I_{SA}	Short circuit current
I_{limit}	Limiting current
V	Voltage
V_{dc}	DC voltage
V_{source}	Source voltage
U_{dc}	Voltage rated

V_{ground}	Ground voltage
V_{main}	Source voltage
V_{rms}	Root mean square voltage
$V_{\text{UFD}n}$	Voltage across ultra fast disconnector n
$V_{\text{LCS}n}$	Voltage across load commutation switch n
$V_{\text{CLI}n}$	Differential voltage across CLIn
V_{TL}	Voltage across transmission line
$V_{\text{TH - IGBT - LCS}}$	LCS's IGBTs threshold voltage
$V_{Gate-Emitter-LCS}$	Gate to emitter voltage of LCS
V_{Breaker}	Voltage across the breaker
U_{MOV}	Voltage across metal oxide varistor
$V_{aux(n)}$	Load side voltage
$V_{aux(differential)}$	Differential voltage at load side
V_{GK}	Gate to cathode voltage
E	Energy
E_s	Source energy
E_{load}	Load energy
E_{c1}	Energy in the capacitor 1
E_{L}	Energy sent back from the breaker's inductor
R	Resistance
R_s	Source resistance
R_{load}	Load resistance
R_{AC-ON}	Anode to cathode resistance
R_{a1}, ..., R_{an}	Line resistances from line-1 to n
R_{CLI}	Branch resistance of CLI
L	Inductance
L_s	Source inductance
L_{a1}, ..., L_{an}	Line inductance from line-1 to n
X	Reactance
X_{CLI}	Reactance of CLI
X/R	Reactance to resistance ratio

Chapter 1

Introduction

This chapter discusses the limitations of high-voltage alternating current (HVAC) systems and highlights the benefits of high-voltage direct current (HVDC) systems over conventional alternate current (AC) systems. It also introduces multi-terminal direct current (MTDC) systems, their benefits, and key hurdles in their development, including the design of direct current circuit breakers (DCCB) for MTDC systems. In addition, the research objectives of this thesis are given in this chapter along with the research contributions. In the end, the thesis organisation is provided.

1.1 Background of High-Voltage Direct Current Transmission

The concept of HVDC transmission was already widely recognized prior to the discovery of HVAC. In 1882, Marcel Deprez implemented the first practical direct current (DC) transmission system, capable of transmitting 1.5kW over 35 miles at a 2kV potential. The concept of AC/DC coexistence gained prominence in the late 19^{th} century. Then, Herwit's mercury-vapour rectifier, designed in 1901, converted AC into DC, and in 1928, controlled rectification and inversion were implemented [1].

In 1939, Dr. Uno Lamm developed the most successful mercury-arc valve design in the

development of HVDC conversion. In 1954, the first mercury arc-based HVDC transmission system was installed between Sweden and Gotland, with a capacity of 20MW and 100kV potential [2], [3]. Solid-state technology replaced Mercury-arc valves as an HVDC conversion unit 34 years later, with the Nelson River Bipole being the last commercial system with a maximum capacity of 6,500MW at 450kV-DC, an 895km long link.

Thyristors, or silicon-controlled rectifiers, were introduced in the 1950s with low electrical characteristics. Rapid development in the 1960s led to their use in HVDC systems, reducing maintenance, extending voltage range, and removing arc backs. The first fully thyristor-based HVDC transmission system was two dual bridge converter stations as discussed in [3].

ASEA Brown Boveri (ABB) constructed the first HVDC link in Sweden in 1954. Thyristor valves in the 1960s improved efficiency, power density, and control flexibility, leading to a dominant HVDC market. Insulated-gate bipolar transistor (IGBT) valves were introduced in the late 1990s [4], offering enhanced grid-support services and improved power quality control. HVDC technology enhances efficiency, stability, reliability, and transmission capacity, but cost is crucial.

1.1.1 Traditional High-Voltage Alternating Current Systems

The HVAC method has been the primary method for transmitting electrical energy for the past century. Fig. 1.1 illustrates the typical AC power system, from generation to delivery, illustrating the relationship between industrial, commercial, and domestic consumers. An AC system simplifies voltage conversion, allowing high power and insulation levels within one unit with lower conversion losses and minimal maintenance, making it a simple and efficient device. Furthermore, a three-phase synchronous generator outperforms a DC generator in all aspects.HVAC method has been the primary method. However, in certain application areas, the performance of AC systems may not be satisfactory and may necessitate the use of alternative methods. A few of the significant disadvantages of HVAC systems are discussed in the studies [5, 6].

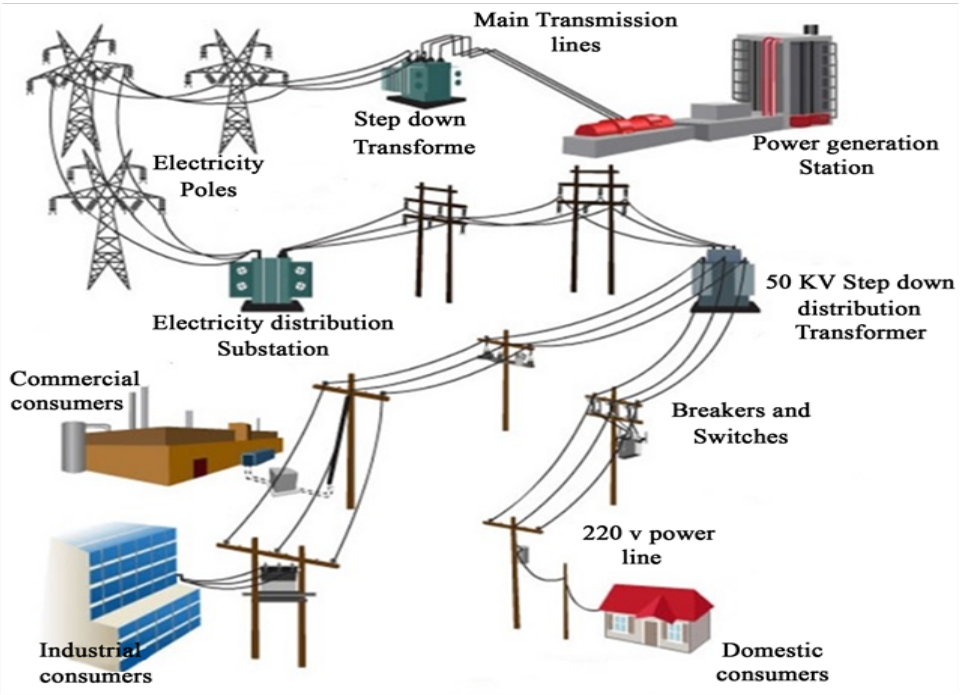

FIGURE 1.1: A high-voltage alternating current transmission network [2].

- The inductive and capacitive elements of overhead lines and cables limit the transmission capacity and distance of AC transmission links. As line length increases, so does the inductance and capacitance, increasing the reactive power compensation requirement and resulting in higher HVAC costs.

- The transmission distance of AC transmission is limited by the reactive power, especially for submarine cables, which can only reach 40km to 100km due to the charging current due to the capacitive element of the cable.

- It is impossible to link two AC systems directly that operate at different frequencies.

- It may be impossible to establish a direct connection between two AC systems that operate at the same frequency or to establish a new connection inside a grid that is linked together due to the instability of the system, excessively high short-circuit levels, or unfavourable power flow scenarios.

- The skin effect occurs when AC flows through a conductor, causing an increase in the effective resistance.herefore, HVDC systems are the preferred choice for long-distance bulk power transmission This occurs when the current density is

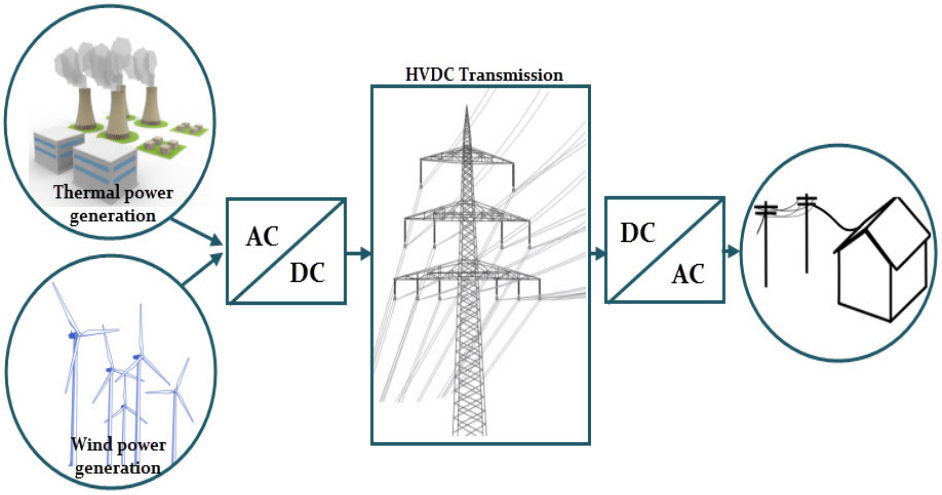

FIGURE 1.2: A high-voltage direct current transmission from source to end-users [3].

highest near the surface and decreases with deeper depths, necessitating a larger conductor cross-section to reduce resistive losses.

Due to these and other similar reasons, electrical engineers have been engaged over generations in the development of HVDC technology as an alternative to HVAC systems.

1.1.2 How HVDC Systems Have Replaced HVAC Systems?

HVDC systems are ideal for applications where HVAC systems are insufficient or economically unfeasible due to their high cost and inability to function. Despite the high cost of HVDC converter stations compared to HVAC systems, the number of HVDC installations annually continues to rise in the early 21stcentury [7]. The typical HVDC transmission system is shown in Fig. 1.2.

The HVDC technology is generally preferred in the following fundamental application area [8].

1.1.2.1 Long-Distance Overhead Lines

Longer HVAC transmission lines necessitate variable reactive power compensation, while HVDC systems are not affected by the inductive and capacitive elements of these lines.

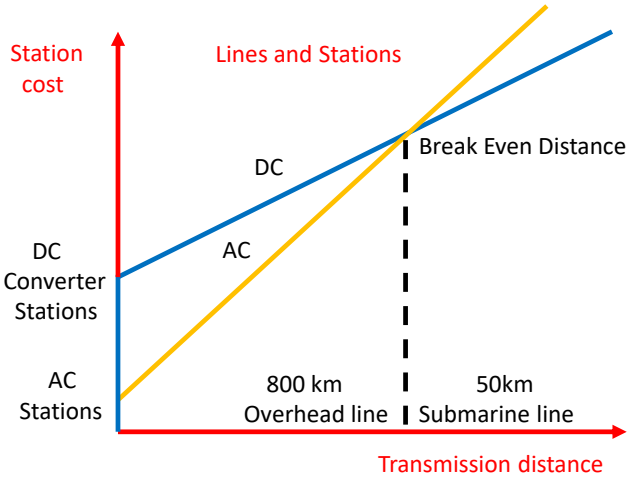

FIGURE 1.3: HVAC vs. HVDC cost comparison and qualitative break-even distance assessment [8].

Therefore, HVDC systems are the preferred choice for long-distance bulk power transmission due to their lower losses and increased flexibility. The break-even distance for HVDC systems is typically 200-450km, making them more economically feasible than HVAC systems as depicted in Fig. 1.3.

1.1.2.2 Subsea Cables Power Transmission

HVDC is the technology of choice for reliably and efficiently transmitting large amounts of power over long distances with minimal losses. ABB's Power Grids division's president, Claudio Facchin, announced the project's completion as ideal for integrating remote renewable energy into the power grid [9]. Siemens has completed similar projects. One example is the Basslink HVDC interconnector, which is a one-pole metallic return scheme with a rated DC voltage of 400kV, a rated current of 1,250A, and a rated continuous power of 500MW. These values are set at the DC terminal of the rectifier converter station, which can be seen in Fig. 1.4. The HVDC converter stations in Loy Yang (Victoria) and George Town (Tasmania) are designed to transmit rated power in either direction.HVDC is the technology of choice for reliably and efficiently transmitting large amounts of power over long distances with minimal losses. ABB's Power Grids division's president, Claudio Facchin, announced the project's completion as ideal for integrating remote renewable energy into the power grid [9]. Siemens has completed similar projects.hese values are set at the DC terminal of the rectifier.

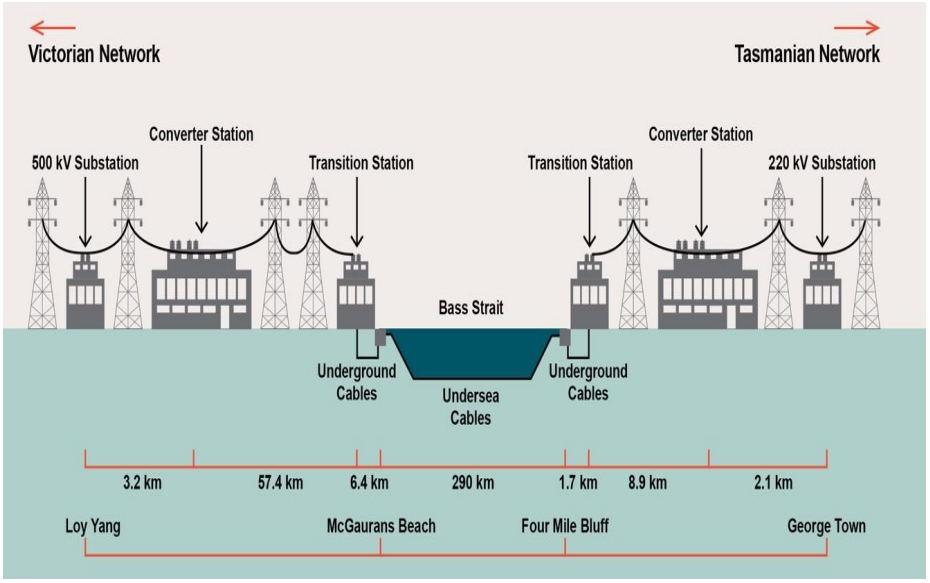

FIGURE 1.4: The high-voltage direct current transmission of Basslink Australia [10].

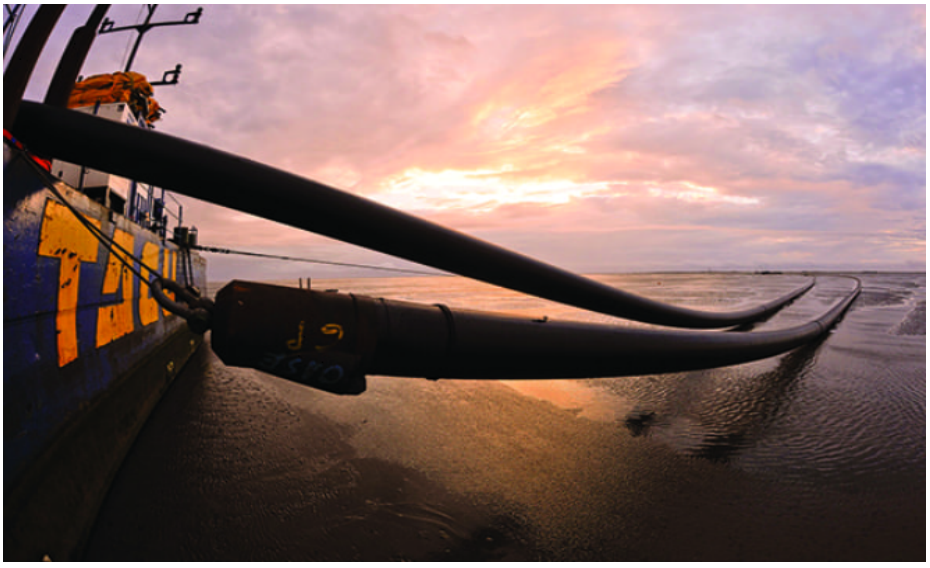

FIGURE 1.5: Power generated by the Nordsee One, Gode Wind I, and Gode Wind II offshore wind farms is transmitted to land via HVDC subsea cables [10] .

1.1.2.3 Bulk Power Transmission

The expansion of bulk power transmission through HVDC across developing countries presents new challenges, but classic HVDC remains cost-effective. Advancements in power electronics have marked a new era for HVDC technology, with the voltage source converter (VSC) being a promising flexible transmission system with a strong future [11]. The expansion of bulk power transmission through HVDC across developing countries presents new challenges, but classic HVDC remains cost-effective. Advancements in

power electronics have marked a new era for HVDC technology, with the voltage source converter (VSC) being a promising flexible transmission

1.1.2.4 Interconnection of AC systems with different frequencies:

The interconnection of AC systems with different frequencies requires efficient power conversion, where HVDC transmission is the preferred solution. MMCs enable HVAC-to-HVDC conversion and back, facilitating seamless integration of asynchronous AC grids with independent frequency control. While matrix converters offer compact design, bidirectional power flow, and improved power quality, their use in high-power systems is limited by scalability constraints, complex control, and increased semiconductor losses. Additionally, they generate significant harmonics, require sophisticated fault protection, and face efficiency and reliability issues for large-scale HVDC applications. In contrast, HVDC transmission provides superior efficiency, reduced transmission losses, enhanced voltage stability, and improved fault ride-through capability, making it the optimal choice for large-scale, long-distance power interconnection by ensuring grid stability and minimizing power oscillations as discussed in studies as well [10, 12].

1.1.2.5 Controllable Power Exchange Between Two AC Networks Trading

In the AC transmission system, impedances of transmission lines affect the flow of electricity, making it unreliable to regulate individual lines. However, HVDC systems can directly control electricity flow and actively participate in the electricity trade. This is a key motivation for developing MTDC systems for the global electricity trade [13].

1.1.2.6 Smaller Requirement of Right of Way

AC transmission requires a three-phase system with three to four conductors for successful electric power transmission, while HVDC systems require only two thinner conductors for the same power transmission [14]. AC transmission requires a three-phase system with three to four conductors for successful electric power transmission.

TABLE 1.1: Comparison of HVAC with HVDC transmission sourced from [15].

Feature	**HVAC Systems**	**HVDC Systems**
Power capacity and distance	Suitable for medium-distance power transmission, but efficiency decreases over long distances.	Highly efficient for long-distance, bulk power transmission with reduced losses.
Losses of power	Higher losses due to skin effect and corona discharge	Lower losses in transmission and conversion, particularly over long distances.
Initial cost of investment	Generally lower due to the wide availability of parts and established infrastructure.	Higher initial cost due to specialized equipment and converter stations.
Asynchronous interconnection	Limited; requires additional systems for interconnecting grids with different frequencies.	Efficient and straightforward interconnection of grids with different frequencies.
Insulation	More insulation is required	Less insulation is required
Voltage regulation and controllability	High controllability and voltage regulation.	Low controllability and voltage regulation
Short-circuit currents	Can contribute to increased short-circuit current levels in the grid.	Does not contribute to short-circuit currents, enhancing grid stability.

1.1.3 Comparison of HVDC with HVAC Systems

The section compares HVDC systems with HVAC systems, highlighting the enhancement of grid performance through HVDC transmission, as presented in Table 1.1 from [15]. The most cost-effective and practical approach is to leverage the experience and lessons learned from the decades of traditional AC power system operation and control. The application of certain solutions or concepts to the DC case could significantly shorten the process of operating and controlling MTDC grids in cohabitation with existing AC power systems. This would involve more efficient design of hierarchical control structures, power-sharing, voltage control, and power flow control, based on AC system design lessons as mentioned in [16]. This summary identifies and describes critical challenges in the operation and control of MTDC systems. The most cost-effective and practical approach is to leverage the experience and lessons learned from the decades.

1.1.4 Multi-Terminal Direct Current Systems

1.1.4.1 Prospects of MTDC Systems

MTDC technology enables power transmission between multiple power sources or receiving ends [17].

1. Multiple converter stations can access sources or loads, transmitting electricity to islands or different load centres.
2. The MTDC interconnections can facilitate cross-regional electrical energy communication trade.
3. The MTDC interconnection has revolutionized the reliability, flexibility, and diversification of electrical power transmission systems.

1.1.4.2 Hurdles in the Development of an MTDC Grid Globally

The most cost-effective and practical approach is to leverage the experience and lessons learned from the decades of traditional AC power system operation and control. The application of certain solutions or concepts to the DC case could significantly shorten the process of operating and controlling MTDC grids in cohabitation with existing AC power systems. This would involve more efficient design of hierarchical control structures, power-sharing, voltage control, and power flow control, based on AC system design lessons as mentioned in [16]. This summary identifies and describes critical challenges in the operation and control of MTDC systems.

1. **System Integration** The MTDC system architecture is well-defined, but the next step is to establish objectives, primary functions, and operational procedures, and identify feasible interactions between AC and DC systems. The optimal performance of the MTDC grid requires a sound integration of both systems [18].
2. **Power Flow Control** In AC grids, flexible AC transmission system (FACTS) is

devices are used for power flow control. In MTDC grids, DC bus voltages are characterized by their amplitude, and transmission line impedances do not present any imaginary component in steady-state at zero frequency. The only magnitudes used for controlling power flow are voltage and current amplitudes. Point-to-point HVDC transmission systems typically arrange power flow control with one terminal controlling the DC-link voltage and the other controlling active power. However, this is not an optimal or flexible control solution for modern power systems. Future MTDC grids need to integrate other devices to make power flow control flexible.

3. **Dynamic Behaviour** The power electronics-based power converter is the crucial component in an MTDC grid, providing faster power exchange due to its additional control capabilities and lack of mechanical inertia. Therefore, precise modelling of power converters and their controllers is essential for assessing the dynamic behaviour of the MTDC grid.

4. **Stability** The MTDC grids lack synchronous frequency components for voltages and currents, and active power flow depends on DC bus voltage differences. Stability analysis for these grids requires a different approach. To ensure dynamic voltage stability, detailed state-space models for the grid, power converters' controllers, and AC network should be elaborated. Systematic analyses should be conducted to define gains for VSC controllers and to know the speed at which they should react to prevent grid collapse.

5. **Protections and HVDC Breaker** Three primary fault types are anticipated to occur in MTDC grids. Firstly, faults on the AC side of power conversion stations, either single or multi-phase, can cause a loss of generation or load in the MTDC grid. For the successful development of MTDC grids, it is imperative that a fault in one AC power system does not propagate through the MTDC grid to another AC system. Secondly, faults may occur at the power converter DC side. This fault type is much more challenging to handle than AC faults. During a DC fault, all interconnected power converters' DC buses severely contribute to the fault current and, due to the low impedance characteristic of DC cables, the direct bus voltages

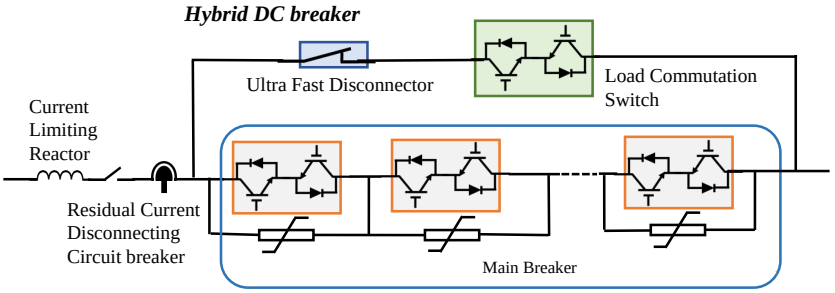

FIGURE 1.6: A representation of ABB's hybrid HVDC breaker [20].

in the MTDC grid are thereby substantially reduced, nearly stopping the power flow.

A fault can occur inside the power converter station itself, which can trip a section of the MTDC grid, and may lead to loss of generation or load The development of appropriate protection devices and strategies for MTDC grids is a challenging issue and the lack of efficient protection strategies is a biting constraint on the pace of development of MTDC technology. In this regard, ABB has launched the world's first HVDC breaker as a promising device for MTDC grid protection [19]. As shown in Fig 1.6, the ABB hybrid breaker combines an ultrafast disconnector with IGBT valves of the main breaker to form a hybrid HVDC breaker. It is a benchmark model used to develop hybrid breakers for the future.

6. **Standardization** Several organizations have initiated research activities in the MTDC grids through their study committees. For instance, CIGRE's B4 study committee on HVDC and power electronics has several working groups (WGs), some held jointly with other committees, studying various aspects of MTDC grids with specific aims and objectives [21]. The aims and objectives of certain WGs include the following:

   - The guidelines provide guidelines for preparing connection agreements or grid codes for the MTDC grids.
   - This guide provides a comprehensive guide for creating models for HVDC converters in the MTDC grids.
   - The study explores load flow control devices and direct voltage control methodologies in an MTDC grid.

- The focus is on designing high-voltage and current distribution grids for optimal reliability and availability performance.
- Definitions of reliability and availability for the MTDC grids.
- Control and protection of the MTDC grids.
- Technical specifications of the state-of-the-art DC switching equipment.
- Recommended voltages for the HVDC grids.

Although in all of the above areas, some progress has been made, be it system integration, power flow control, dynamic behaviour, or stability standardization, the world has been stuck on protections in multi-terminal DC, and hardly any breaker is available commercially. Thus, the main focus of this research is on protection and HVDC circuit breakers.

1.1.4.3 Challenges in the Local Development of HVDC Grids

The Matiari to Lahore 765 kV HVDC transmission project is a major step in Pakistan's energy infrastructure, but it faces several key challenges:

1. **Frequent Tripping and Grid Instability** The system has experienced multiple unexpected shutdowns and power fluctuations, affecting grid stability and causing blackouts in some regions.
2. **Load Management Issues** The transmission system was designed to transport 4,000MW, but demand fluctuations and supply inconsistencies sometimes create operational inefficiencies.
3. **Synchronization Problems with the AC Grid** The HVDC system needs seamless integration with Pakistan's existing AC transmission network, but differences in grid frequency and load balancing have led to technical difficulties.
4. **Converter Station & Equipment Maintenance** The high-tech converter sta-

-tions in Matiari and Lahore require specialized maintenance, but Pakistan currently lacks sufficient local expertise, making troubleshooting and repairs challenging.

5. **Voltage Drop and Power Losses** Despite being an HVDC system, some voltage drop issues have been reported, especially during peak load conditions, impacting efficient power transmission.

6. **Chinese Firm's Operational Control** The project is operated by a Chinese company under a 25-year agreement, leading to concerns about technical dependency and costly maintenance contracts.

7. **Security and Weather-Related Threats** The transmission infrastructure passes through various terrains, making it vulnerable to extreme weather, sabotage, and physical damage.

   These challenges highlight the need for better grid management, technical expertise, and long-term operational planning to ensure the system runs smoothly and delivers the intended benefits.

1.1.5 Fundamentals of DC Fault Current Interruption

The proposed research focuses on HVDC circuit breaker design and introduces the fundamentals of DC fault current interruption. There are two methods to break current flow in an electrical circuit: shutting down the power source or interrupting the flowing current. In an electrical grid, shutting down is not feasible when the current needs to be broken in only a small portion, so interrupting the flowing current is considered the standard practice.

When a circuit breaker's current-carrying contacts are opened, an arc is generated between them as plasma bridges the gap as shown in Fig. 1.7. This arc can carry large currents, but if allowed to flow for an extended period, it can permanently damage the contacts. The interruption process occurs when the electric arc between the contacts is extinguished. In this section, we will briefly compare the AC and DC fault current

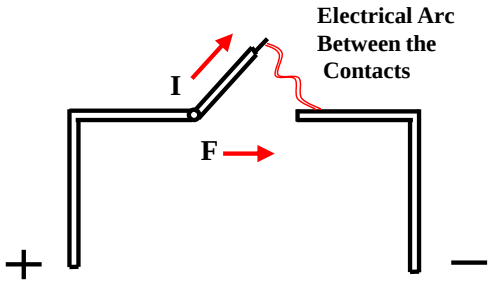

FIGURE 1.7: Opening a circuit breaker creates an arc between the contacts, allowing current to flow through the arc plasma [22].

interruption methods and highlight challenges in the interruption of DC fault current. Later on, we will talk about the various methods adopted to interrupt DC fault currents.

1.1.5.1 AC Fault Current Interruption

The AC grid has become a mature technology over the past 100 years, specializing in generation, transmission, distribution, transformers, and circuit breakers. The circuit breaker is a crucial component of an electrical grid, serving as the heart of modern AC grids. Its ability to quickly isolate faulted networks from the healthy grid ensures continuous power supply, as a single fault in a small part can shut down the entire power network.

HVAC grid protection is a reliable and resilient technology with numerous circuit breaker topologies. The AC passes through zero twice during each cycle as depicted in Fig. 1.8, automatically extinguishing the arc at zero-crossing. HVAC circuit breakers effectively interrupt HAVC fault currents by preventing re-ignition of the arc between contacts.

1.1.5.2 DC Fault Current Interruption

The DC fault current increases rapidly due to the lower impedance of DC transmission lines, potentially damaging the entire HVDC system within milliseconds due to its lack of zero-crossing as shown in Fig. 1.9. The arc ignited between circuit breaker contacts cannot be interrupted once they have opened. To achieve a successful current interruption, a fault current must be forced to zero through the creation of RLC oscillation

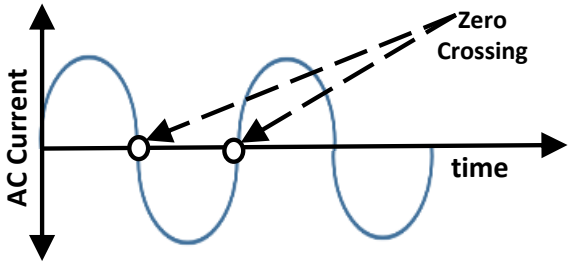

FIGURE 1.8: A depiction of AC fault current with zero-crossings [23].

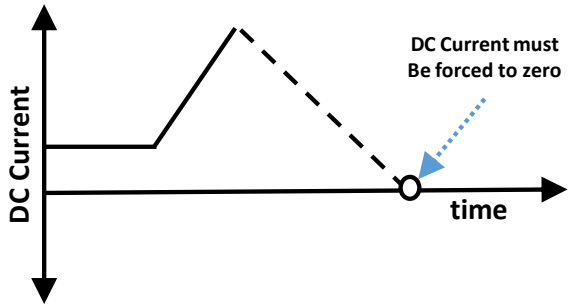

FIGURE 1.9: The current in HVDC before and after a fault is analyzed [20].

topology in DC circuit breaker design or by dumping fault energy in the arc distinguishing chambers metal oxide varistors (MOVs). The DC fault current can be forced to zero by various methods, as described below:

1. By increasing the arc voltage above the system voltage, the DC fault current will decrease.
2. The DC fault current will be zero when a reverse current flow is injected.
3. Generate oscillations in the DC fault current that will force the DC fault current to cross zero level.

DCCBs are essential for preventing rising DC fault currents from reaching zero. They are designed to isolate the circuit using simple electro-mechanical contacts. The surge impedance of HVDC systems is low, unlike HVAC systems, due to the absence of reactive components. The fault current can reach high values quickly, requiring a quick reaction from the DCCB. If the DCCB fails to form a DC current zero, a severe arc can form, melting the contacts and causing thermal runaway, potentially destroying the DCCB and the entire HVDC transmission system as well as discussed in [21]. Fig. 1.10 shows a

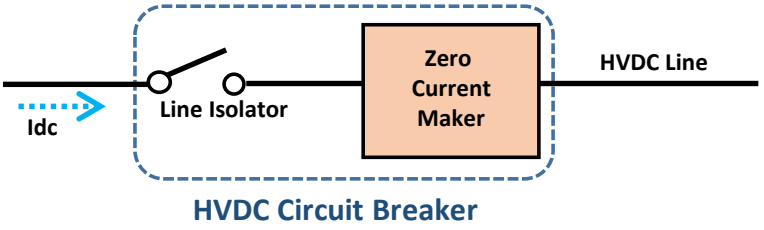

FIGURE 1.10: A generic layout of a universal direct current circuit breaker [24].

generic layout of a universal DCCB. The DCCB fundamental parts and their functions are:

1. **Zero-current generator:** This DCCB part is responsible for ensuring the DCCB fault current is zero before opening contacts to isolate the HVDC line.

2. **Line separator:** This part, resembling a conventional HVAC circuit breaker, physically breaks the electrical circuit at zero DC current, isolating the faulted HVDC line.

1.2 Research Objectives

The key research objectives of this thesis are as follows:

1.2.1 Literature Review Towards the Development of a Novel Direct Current Circuit Breaker Topology

This research aims to develop advanced DCCB topologies by conducting a comprehensive literature review. It begins by exploring the fundamentals of circuit breakers, then analyzes various types of DCCBs, focusing on the HDCCBs due to their superior performance. Existing HDCCB designs will be reviewed, highlighting their key features like fault interruption and energy dissipation capabilities. The concept of multi-port HDCCBs will be explored, offering insights into their ability to handle multiple transmission lines in complex systems. The research will identify a gap in existing work, on which a problem statement could be built.

1.2.2 Minimize Interruption Time and Enable Bidirectional Fault Protection

Multi-terminal direct current transmissions face significant fault current challenges due to the low impedance of HVDC transmission lines, and to protect against cascading failures, circuit breaker topology must minimize interruption time while addressing faults in both directions. Thus, a DCCB must swiftly interrupt fault current, preventing severe over-current and system destruction within milliseconds.

1.2.3 Regenerate Fault Current After Interruption and Minimize Breaker Size

In the case of MTDC systems, fault energy is significantly large. Installing a large surge arrester to dissipate this fault energy for fault clearance, even after the fault has been interrupted, is impractical due to the size and inefficiency of such a solution. An alternative approach involves regenerating the fault energy and sending it back to the grid, which can reduce the strain on the surge arrester. This allows for a more compact circuit breaker design. HVDC circuit breaker designs currently depend on lossy impedance networks to handle fault energy. However, these networks are not ideal as they not only increase the overall size of the system but also cost.To ensure protection in the HVDC system.

1.2.4 Minimize Fault Current Magnitude Before the Inter--ruption and Prioritize HVDC Source Protection

To ensure protection in the HVDC system, it is crucial to reduce the fault current magnitude before opening the breaker contacts, thereby commutating the current beforehand and avoiding long-term electric arcs. In the case of HVDC systems, protecting the expensive source is paramount, making source protection a key consideration while designing DCCBs.To ensure protection in the HVDC system, it is crucial to reduce.

1.2.5 Enable a Single DCCB to Protect Multiple HVDC Transmission Lines

The installation of a single DCCB for multiple transmission lines can significantly lower protection costs by eliminating the need for separate breakers at each end. Additionally, minimizing components within the breaker topology enhances both turn-on and interruption times, streamlining control schemes and enabling more compact designs.

1.2.6 Reduce Breaker Reset Time to Bring Back System for Next Operation

The breaker reset stage is a crucial phase in HVDC hybrid circuit breakers, ensuring the system returns to normal operation after a fault. It involves triggering semiconductor devices to manage system current and prevent inertial current interference. When the inertial current decays to zero, the breaker begins its re-closing procedure, closing ultra-fast disconnector switches, triggering load commutation switches, and blocking submodules. The successful execution of these operations ensures the system recovers to its normal state, minimizing breaker reset time and ensuring the HVDC network can return to normal operation after a fault. The research will conduct a comprehensive comparative analysis of the proposed DCCB topologies

1.2.7 Comparative Analysis to Validate the Proposed Design

The research will conduct a comprehensive comparative analysis of the proposed DCCB topologies, against existing high-performance circuit breaker topologies. The evaluation will consider factors such as current interruption time, breaker reset or recovery time, regeneration capability, breaker size, cost, and control complexity. The research will conduct a comprehensive comparative analysis DCCB topologies. The aim is to demonstrate that the proposed topologies meet or exceed the performance of existing solutions, making them more effective and reliable options for future MTDC networks.

1.3 Research Contributions

The primary contributions of this research work are listed as follows:

- The research addresses the large fault energy dissipation in MTDC systems by proposing two novel hybrid DCCB topologies: modular hybrid DCCB with fault current self-adaptive control and protective coordination (MHDCCB) and improved hybrid DCCB with battery banks for energy storage (HDCCB). The MHDCCB features a two-stage current limiting mechanism that extends the current limiting duration and adapts to primary and backup protection, ensuring effective fault management and this was published in [25]. Another topology, specifically proposed for large fault energy dissipation issues is the improved HDCCB topology that uses a resistor-inductor-capacitor resonance to create current zero-crossings, afterwards, storing inductive energy from network faults in battery banks for future use and this work is published in [26]. Both topologies integrate battery banks to store the breaker's inductor energy during fault events. Simulation results show that battery banks successfully store charge generated during fault events. However, the major setback is increased system cost due to occasional faults and battery degradation or unused usage.

- To address the limitations of installing battery banks for breakers' energy storage after fault interruption, further research is conducted, and a novel regenerative hybrid high-voltage direct current circuit breaker (HDCCB) topology is proposed. This approach introduces the concept of fault current regeneration, which involves regenerating fault energy during fault occurrence and sending it back to the grid for future use. The novel topology minimizes fault current interruption and breaker reset time, allowing fault interruptions under 2ms and restoration to normal operation within 5ms. It features a current-limiting branch to reduce peak fault currents and a compact topology with reduced component count, simplifying control schemes and improving integration with HVDC systems. The regeneration feature, enables the recovery and reuse of 1.5MJ of fault energy, surpassing the traditional topology of 17.07kJ. Furthermore, this research provides a comprehen-

sive analysis of the proposed HDCCB compared to existing topologies, evaluating its performance in terms of fault interruption, reset time, regeneration capability, and control complexity. This contribution as a journal article is under review in *IEEE Access*. Although the proposed topology ensures promising results in terms of interruption, breaker reset time, and regeneration, the limitation of this topology is it is needed separately for the protection at each end.

- Moving forward, a novel hybrid multi-port direct current circuit breaker (HMPDCCB) topology is proposed for the protection of multiple transmission lines using a single HMPDCCB. The innovative design utilizes a common main breaker branch for all transmission lines during a fault event, significantly reducing the breaker's size and cost. This topology efficiently protects the HVDC systems by reducing current interruption time to under 1.8ms and resetting within 3ms. Additionally, the breaker incorporates a fault current regeneration feature, retrieving 0.35MJ of energy, which helps manage energy dissipation. Current-limiting inductors (CLIs) are employed to prevent sudden fault current surges, while a simplified controller monitors the voltage across CLIs to identify fault lines. The controller selects the port with the minimum voltage as the receiving port for regenerated energy. This compact, cost-effective solution delivers selective protection across all connected HVDC lines and enhances system efficiency, making it superior to existing circuit breaker topologies. Our contribution as a journal article was published in [27].

1.4 Thesis Organization

The research thesis is divided into six sections, each with its own focus. Chapter 1 introduces HVDC systems, DC fault current interruption, and the MTDC system, highlighting the importance of direct current circuit breakers (DCCB) and the research objectives and key contributions. Chapter 2 discusses the need for hybrid DCCBs in MTDC development, reviewing various types of DCCBs and literature. It also explores multi-port hybrid DC circuit breakers, analyzing existing literature constraints, gap analysis, and presenting a problem statement. Chapter 3 discusses modifications in existing literature

for hybrid DCCBs to store fault energy after fault current interruption, demonstrating the concept of installing battery banks for energy storage and potential regeneration in the future. Chapter 4 presents an efficient regenerative hybrid HVDC circuit breaker topology with an interruption time under 2ms and a reset time below 3ms, featuring regeneration capability. Chapter 5 introduces a hybrid multi-port HVDC circuit breaker that enhances interruption time to under 2ms and reset time to below 3ms through shared energy dissipation and fault current regeneration. Chapter 6 concludes the research work and presents propositions for future research.

Chapter 2

Literature Review

The HVDC systems are essential for integrating large-scale renewable energy sources like wind and solar power into electrical grids. They offer reduced power losses and stability, making them suitable for connecting remote sites to population centres. However, the development of HVDC grids introduces new technical challenges, particularly in fault protection. The direct current circuit breaker is crucial for ensuring safe and reliable operation of the HVDC grids.

This chapter will provide a comprehensive analysis of HVDC circuit breaker topologies and conversion technologies. It compares the capabilities of alternating current circuit breakers (ACCBs) and direct current circuit breakers (DCCBs) in handling fault currents, establishing the unique requirements and challenges faced by HVDC systems. The chapter also explores essential characteristics required from high-voltage DCCBs, the commercial technologies available, and ongoing challenges in developing efficient HVDC circuit breakers.

In addition, a critical survey and analysis of various topologies, including mechanical, solid-state, and hybrid breakers, followed by a discussion of research gaps and proposed methodologies, will be presented. The chapter also discusses the main technical challenges in developing HVDC circuit breaker topologies capable of effective fault current interruption. Furthermore, a review of traditional HVDC circuit breaker topologies, including mechanical circuit breaker (MCB), solid-state circuit breaker (SSCB), hybrid

circuit breaker (HCB), and Z-source circuit breaker (ZSCB) topologies will be given. A comprehensive critical survey of single-terminal hybrid HVDC circuit breaker topologies is conducted, and protection schemes for multi-terminal HVDC networks using multi-port circuit breaker topologies are evaluated, followed by the limitations of these topologies.

This chapter will then conclude with a problem statement addressing gaps and challenges identified from the critical analysis of the existing research in HVDC circuit breaker topologies, outlining a proposed methodology to tackle these issues and the chapter will end with a summary of the literature review. A concluding summary, highlighting the key findings and setting the stage for subsequent chapters.

2.1 Comparison of ACCBs and DCCBs in Handling HVAC/HVDC Fault Currents

This section compares alternating and direct current circuit breakers based on their operational parameters, such as interruption time, mechanisms, and development status, also detailed in Table 2.1. ACCBs have a commercially available interruption time of tens of milliseconds, typically between 80ms to 100ms, and utilize the natural zero crossing of the alternating current waveform to safely interrupt and dissipate fault current. They benefit from established standards like IEEE C37.06 mentioned in [20], ensuring consistency and reliability in their design and application.

DCCBs, on the other hand, are still in the research and development phase with no formalized standards governing their design. They have faster interruption times of 2ms to 10ms, making them more efficient in cutting off fault currents in direct current systems as discussed in [28, 29]. However, DCCBs have a lower maximum breaking current capacity of 16kA to 25kA compared to ACCBs, reflecting a gap in performance for handling large fault currents.

The commercial availability of ACCBs and robust standards make them a mature, reliable solution for AC systems, while DCCBs face challenges in achieving widespread

TABLE 2.1: A general comparison between ACCBs and DCCBs [28].

Feature	**ACCBs**	**DCCBs**
Interruption time	Tens of milliseconds (80ms–100ms)	2ms–10ms
Interruption mechanism	Utilizing natural zero crossing in fault current to extinguish the arc and interrupt the AC fault current	Utilizing additional branches to create a current zero crossing for the fault current interruption
Max. breaking current	40kA–60kA	16kA–25kA
Standardization	IEEE c37.06	No standards for DCCB
Development state	Commercially available	In research and development stage

standardization. Their development is crucial for the future of DC power systems, particularly in renewable energy integration and HVDC applications. Therefore, the behaviour of converters during DC faults presents a challenging issue in the MTDC systems.

2.2 Essential Characteristics Required from High-voltage Direct Current Circuit Breaker

HVDC circuit breakers should exhibit key characteristics such as fast fault isolation, low conduction losses, and high reliability to ensure efficient power system protection. These essential features are illustrated in Fig. 2.1 for a comprehensive understanding:

- Fault Current Interruption Time: Rapid fault clearance with a response time typically below 3ms to maintain system stability.
- Maximum Current Breaking Capability: Handles high fault currents without damage or sustained electric arcing.
- Over-Voltage Protection: Safeguards system by limiting voltage spikes that could damage equipment. It ensures stable performance by suppressing excess voltage.

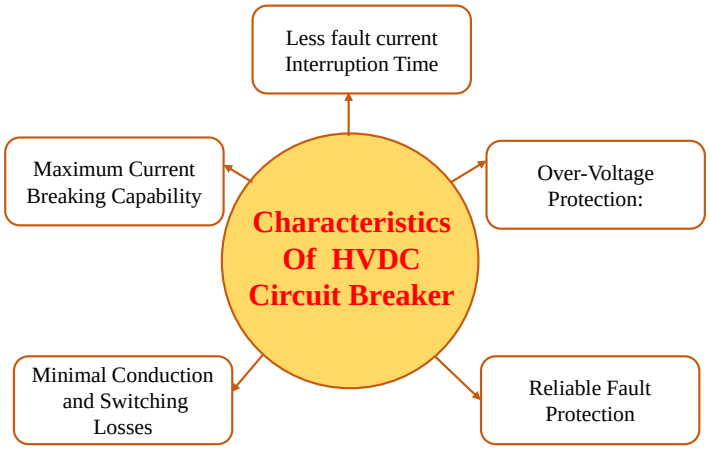

FIGURE 2.1: The characteristics of HVDC circuit breakers [28].

- Minimal Conduction and Switching Losses: Ensures energy-efficient operation by reducing losses during switching transitions [30].
- Reliable Fault Protection: Offers robust and efficient protection against all types of faults with minimal downtime.

2.3 Commercial HVDC Conversion Technologies and their Key Characteristics

HVDC technology is a promising solution for transmitting large amounts of power through long-distance and asynchronous network interconnections, with demand increasing due to large renewable energy installations. Table 2.2 compares line-commutated converters (LCC) and self-commutated voltage source converters (VSC) for HVDC conversion technologies. LCC has higher voltage and power capabilities but requires reversing voltage polarity for power flow control. It's suitable for AC. It's suitable for stronger AC networks but faces communication failures. and specialized MI cables as discussed in the study [31]. Using IGBT-based systems, VSC offers independent control of active and reactive power, greater operational flexibility, and easier integration with weak AC grids. As mentioned in [32], despite higher costs, VSC offers reduced harmonic filtering needs, better black start capabilities, and compatibility with grid requirements, making it a promising conversion technique for future HVDC systems.

TABLE 2.2: The principal characteristics of HVDC conversion methodologies [14].

Characteristic	**LCC technology**	**VSC technology**
Basic element	Thyristor technology	IGBT technology
Capability	More power capability and voltage—good overload capacity	Reduced power capability and voltage—weaker overload capacity
Power flow reversal	Reversal of power by alteration of voltage polarity	Reversal of power by alteration of current flow direction
Active/reactive power	Consumes a significant quantity of reactive power	Separate control over reactive and active power
Overall cost	Reduced capital costs—Lower station losses	Larger capital costs due to higher station losses
Harmonic-related factors	Large site area needed—harmonic filters	Small/no need for filters—Very portable area
AC network limits	stronger AC systems are required.	Connectability to less powerful AC systems
Black start	Additional equipment is required for black start capabilities.	Black start functionality
Form of storing energy	Inductively storing energy	Capacitive energy storage
Commutation issues	Failures in commutation could occur	avoiding the failure of commutation
Cables	Require use of MI cables	Ideal for use with XLPE cables
Fault-related performance	DC fault current tolerance—AC side faults are vulnerable	More sensitive to DC side faults

2.4 Key Challenges in Developing HVDC Circuit Breaker Topologies for Effective Fault Current Interruption

A severe DC fault current in MTDC is large d_i/d_t and cannot be interrupted using conventional electro-mechanical circuit breaker technology. MTDC protection systems are anticipated to tackle three significant challenges. MTDC protection systems are anticipated to tackle three significant challenges. The interruption of DC fault current in MTDC is highly challenging due to three main challenges described in the following

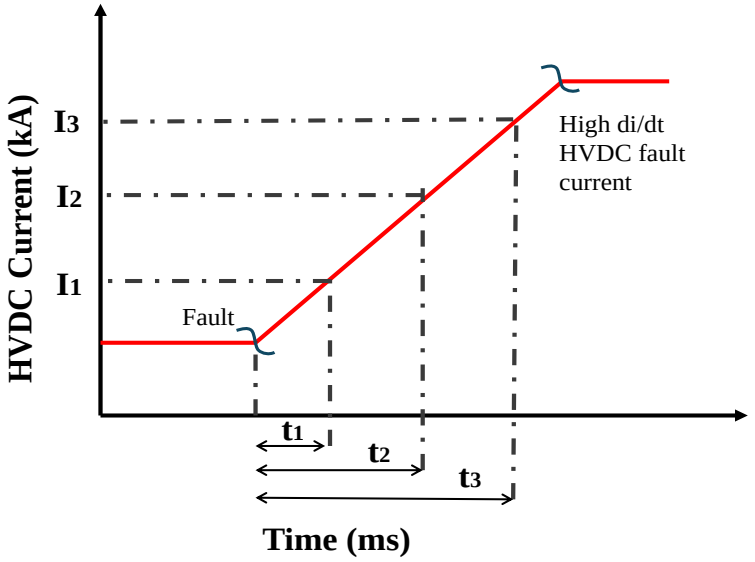

FIGURE 2.2: MTDC fault current with very large d_i/d_t, the delay in interruption time leads to increased fault current towards its maximum threshold ($t_3 > t_2 > t_1$ causes $I_3 > I_2 > I_1$) [23].

sub-sections.

2.4.1 Large DC Fault Current Magnitude

In MTDC, a DC fault current rises much more rapidly and has a larger magnitude than in point-to-point HVDC systems and even conventional AC grids. The reason for this is the integration of multiple power sources into various converter stations. Also, due to the parallel integration of all the HVDC lines, the MTDC has a much lower surge impedance as compared to point-to-point HVDC systems as elaborated with detail in the book [14].

The MTDC fault current has a large d_i/d_t, becomes unbreakable due to its large amplitude, and has a large prospective value. This causes significant voltage and energy stresses for the DCCB components, making them difficult to develop in practical applications due to their large voltage rating, energy dissipation requirement, enlarged size, and high costs. The breaker's time to interrupt increases the magnitude of the fault current, making it difficult to interrupt later. Therefore, it's crucial to interrupt. Therefore, it's crucial to interrupt the fault current as soon as possible to protect the overall HVDC transmission from cascaded failure, as shown in Fig. 2.2.

2.4.2 Large Fault Energy Dissipation

A large fault energy dissipation is a critical challenge in HVDC transmission systems, particularly in multi-terminal grids. These systems are designed to link multiple sources and loads, making them efficient for transmitting bulk power over long distances with minimal losses. However, when a fault occurs in any transmission line within this network, the relatively low line impedance of HVDC systems can cause significant challenges in managing the resulting fault current. This requires the fault energy to be rapidly dissipated to protect the system and maintain stability.

HVDC systems are characterized by low line impedance, which allows for efficient power transmission with minimal voltage drops and reduced losses. However, this same characteristic can lead to complications in fault conditions, such as short circuits or ground faults, where the low impedance path results in a rapid and uncontrolled increase in fault current. Fig. 2.3 represents a fault in line-1 of an MTDC network that disrupts normal power flow, causing fault currents from all nodes to surge towards the fault point and reverse the direction of current at point B and through line-2. This presents a serious risk to HVDC system components, such as converters, transformers, and cables, if the fault is not managed quickly, as highlighted in the book [33]. In contrast to AC systems, HVDC systems lack zero-crossings, meaning that DC faults can be more severe, requiring faster and more effective protection schemes to isolate the fault and dissipate the large amount of energy generated during the fault condition. Possible solutions to the fault energy dissipation problem include hybrid DC circuit breakers, energy storage systems, and advanced DC circuit breakers.

2.4.3 Consideration of Bi-directional Current Interruption

Current interruption in MTDC faces challenges due to the bi-directional flow of DC. AC has a specific direction, while AC has both positive and negative portions in every cycle. AC interruption is not concerned with the direction of current flow, but hybrid DCCBs, composed of solid-state components, cannot ignore the direction of DC. It is crucial to identify whether MTDC can have a change in the current direction, which

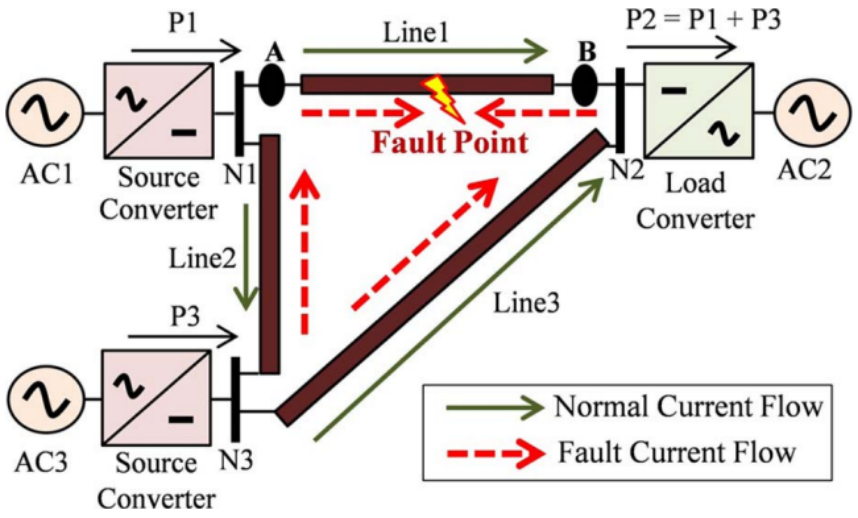

FIGURE 2.3: A fault in line-1 of an MTDC network disrupts normal power flow, causing fault currents from all nodes to surge towards the fault point, and reverse the direction of current at point B and through line-2 [24].

can cause difficulties for DCCBs to interrupt DC fault current as discussed in [34]. In VSC-HVDC MTDC, power flow is controlled by changing the current direction, while voltage remains constant. This differs from LCC-HVDC, where the current direction is constant and voltage is interchanged to control power flow. Therefore, in VSC-HVDC MTDC, power flow and DCCBs at the terminating ends of each HVDC transmission line must be able to interrupt current in both forward and reverse directions during normal operation [35].

2.5 Commercialized HVDC Circuit Breakers Availability and Limitations

The key specifications and design challenges of circuit breakers from ABB, Alstom, and Siemens are compared in Table 2.3. ABB's circuit breaker has a high-rated voltage of 320kV and a substantial current-breaking capability of 9kA, allowing fast switching and reducing response time during faults. However, it struggles with high peak currents associated with direct current faults, a significant drawback for high-stress applications as discussed in study [36]. Alstom's circuit breaker, rated lower at 160kV and 7.5kA, addresses high fault currents through thyristor stacks in series with capacitors, but its

TABLE 2.3: A comparison of ABB, Siemens, and Alstom HDCCBs [38].

HDCCB Type	**Features**
ABB	- Rated voltage: 320kV - Current breaking capacity: 9kA - IGBTs are deployed in auxiliary branches in series connection. - Fast switching capabilities - Not designed for high peak current during DC faults.
Alstom	- LCS water cooling system - Requires 160kV rated voltage. - Has 7.5kA current breaking capability. - It uses thyristor stacks in series with a capacitor. - Resists high fault currents. - Main issue: turning off thyristors.
Siemens	- Employs uncharged capacitors in place of power electronic switches within auxiliary branches. - Can use one or more varistors with a CB. - Primary issue: high impedance fault current breaking.

reliance on a water cooling system increases maintenance and infrastructure complexity. Turning off the thyristors after a fault presents a major operational challenge, indicating a potential weak point in its fault-clearing capability. Siemens uses an uncharged capacitor instead of electronic switches in its auxiliary branch, reducing complexity but introducing limitations, such as dealing with high impedance fault currents mentioned in the study [37]. Siemens also explores the possibility of using one or more varistors in combination with the circuit breaker, which may provide additional flexibility but complicate system design and integration.

2.6 Traditional HVDC Circuit Breakers

Types of DCCB topologies discussed in the literature for fault current breaking in HVDC applications. Traditional CBs use line commutated converter topology, but they are slow and not effective for fast switching as elaborated with detail in Section 2.3. However, voltage source converter technology offers a promising conversion topology with fast

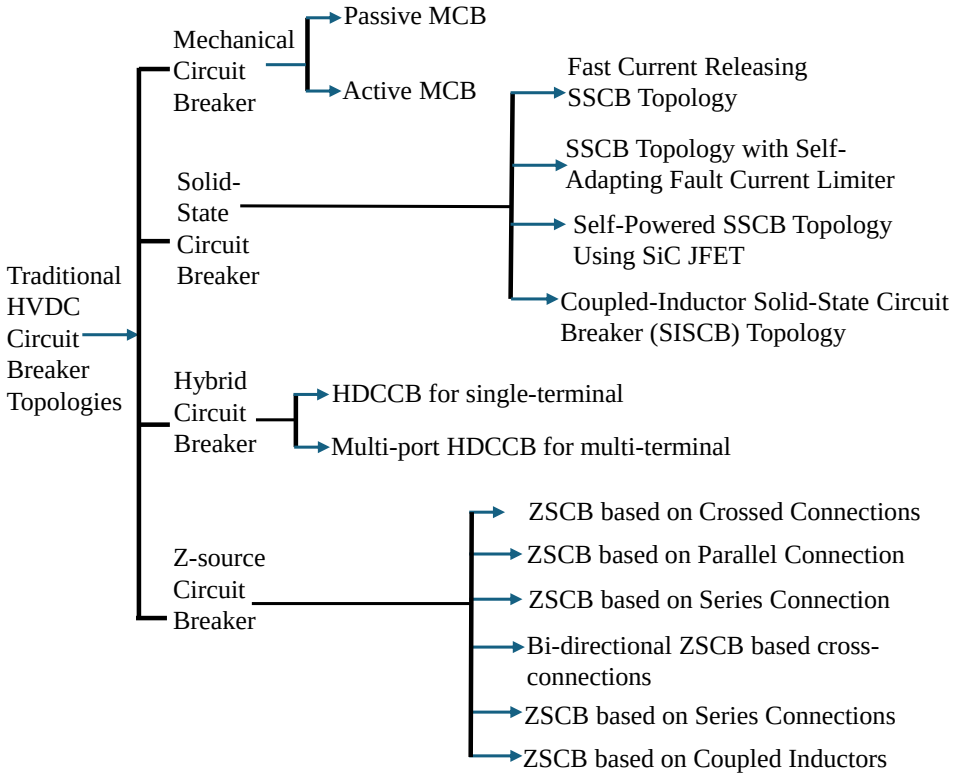

FIGURE 2.4: A Comprehensive review of the traditional HVDC circuit breaker topologies [23, 39, 40].

switching, reducing fault current interruption time for HVDC grid protection. Therefore, it is crucial to develop fast DCCBs to protect VSC-based HVDC grids. The general classification of DCCBs is explained in the following section.

2.6.1 Mechanical Circuit Breakers

A mechanical circuit breaker has a low on-state loss and high reliability. However, the fault current interruption time of the MCB can be delayed to tens of milliseconds or longer due to the long-term operation of a mechanical switch, which reduces the safety for MTDC grid protection as illustrated in [41–47]. It is a conventional ideal switch. It helps to limit voltage through a metal oxide varistor (MOV). MOV acts as an absorber element. MCB is comprised of a mechanical switch, MOV, and a commutation circuit as depicted in Fig. 2.5. The drawbacks of MCB include the slow pace of operation and limited current interruption capabilities [48, 49]. DC fault current interruption using mechanical DCCBs involves creating an artificial zero crossing in the fault current.

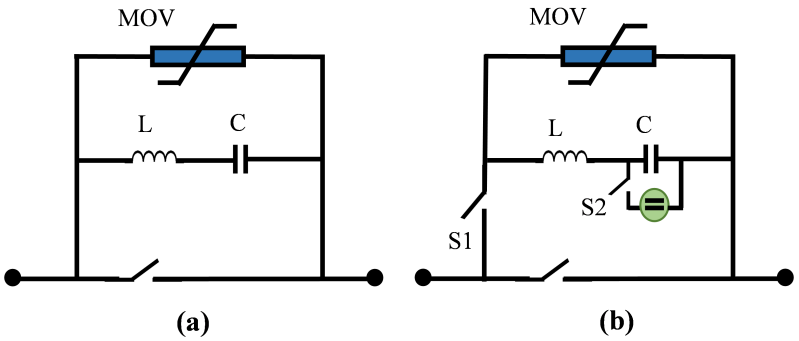

FIGURE 2.5: The diagram of (a) Passive MCB and (b) Active MCB.

These MCBs are typically built using a mechanical interrupter, commutation branch, and energy dissipation branch. As shown in Fig. 2.5(a) passive resonant MCBs have a simple structure and high breaking reliability, but their operational speed is slow. A new passive MCB has been proposed, which can generate zero crossings in a short time.

Active MCBs consist of a pre-charged capacitor, an inductance, and a switch as depicted in Fig. 2.5(b). These MCBs can interrupt the current in either direction and use IGCTs to enhance circuit-breaking capability at low cost. Two types of MCBs are presented: one based on a pre-charged capacitor and the other on an improved bidirectional topology based on the magnetic induction current commutation module (MICCM). Both topologies can break fault current up to 15kA within 3ms as mentioned in [39, 50]. Active MCBs have faster interruption speed and more stable interruption capability compared to passive types. However, they have limited conduction losses and slower operational speed due to arc exhaustion between contactors. Careful design of the commutation capacitor is necessary for obtaining large current commutation capability under fault current interruption.

2.6.2 Solid-State Circuit Breakers

Solid-state circuit breakers include electronic devices such as IGBT, IGCT, and GTO which are used for the current interruption as depicted in Fig. 2.6. Voltage surge is controlled by a metal oxide varistor that dissipates the stored energy of network inductances. The disadvantages of SSCB are increased conduction losses and lack of galvanic separation as mentioned in several articles [51–53].In these articles, SSCB was

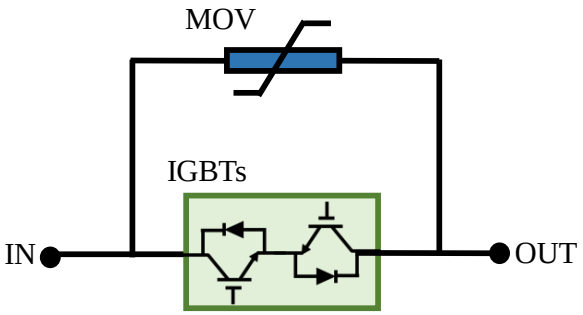

FIGURE 2.6: Diagram of a solid-state circuit breaker.

preferred due to fast switching, fewer losses, and voltage and current bearing capacity. That is phenomenal for HVDC transmission. The modifications in SSCB from the literature are discussed below:

2.6.2.1 A Fast Current Releasing SSCB

is a design that provides rapid protection by disconnecting static switches in short-circuits, limiting short-circuit current to safe levels and enhancing system stability. It minimizes power losses during normal operation, optimizing energy efficiency and making it suitable for power conservation applications. However, it cannot handle bidirectional power flow, making it less suitable for renewable energy systems or advanced electrical grids as mentioned in [40–42]. Additionally, the topology has high costs due to its sophisticated design and high-speed operation, making it less economically viable for widespread use, especially in smaller or cost-sensitive applications.

2.6.2.2 An SSCB With Self-Adaptive Fault Current Limiting

provides advanced fault protection by automatically limiting fault current based on fault magnitude, enhancing system safety and stability without manual intervention. This system can respond to various fault conditions, providing robust protection for electrical networks. However, it lacks bidirectional power. However, it lacks bidirectional power flow capability, restricting its flexibility, especially in modern energy systems where bidirectional flow is often required. As a result, its application is limited to scenarios where unidirectional power flow is sufficient as discussed in [43, 44].

2.6.2.3 A Self-Powered SSCB Using SiC JFET

is a self-powered circuit breaker that operates without external power, making it highly reliable in remote or off-grid locations. It also features an automatic self-adaptive fault current limiting feature, allowing the system to adjust automatically to different fault conditions without human intervention. However, this topology is not yet commercially available due to its prototype or experimental stage, making it less widely adopted or tested in real-world scenarios. Its complex internal structure makes it more challenging to manufacture and maintain, potentially leading to higher operational costs or technical difficulties. Additionally, it lacks bidirectional power flow capability, further limiting its potential applications as explained in [45].

2.6.2.4 A Coupled-Inductor SSCB

is a fast operation method suitable for applications requiring rapid circuit disconnection to protect against fault conditions. Its self-triggering capability reduces manual oversight and enhances reliability. However, the SISCB topology faces challenges in commercialization due to its lack of widespread adoption and its inability to handle bidirectional power flow, which limits its use in complex electrical systems. Despite its potential, these limitations need to be addressed before it can be considered a viable solution for widespread use. The topology's self-triggering capability also contributes to its reliability.

2.6.3 Hybrid Circuit Breakers

Hybrid circuit breakers (HCBs) are a combination of mechanical and solid-state circuit breakers designed to have low losses during normal operation and fast interruption performance. They interrupt current in an auxiliary branch parallel to the main current conduction path, similar to SSCBs. The performance of HCBs is significantly influenced by voltage and current stresses, on-state voltage drop, failure characteristics, series voltage equalization effect, and parallel current sharing impact of power electronic devices.

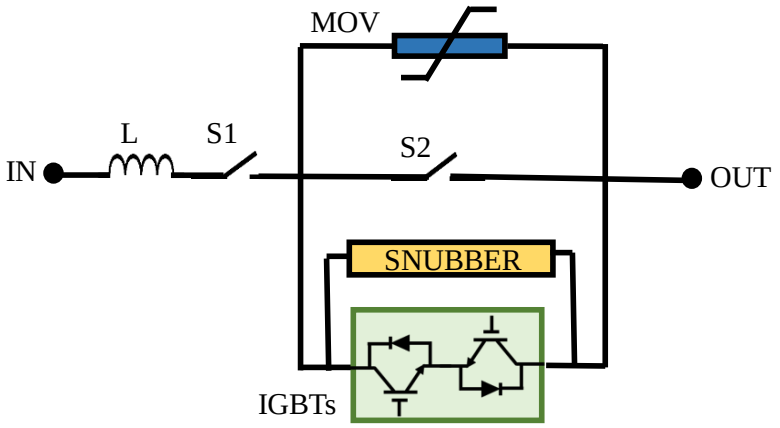

FIGURE 2.7: Diagram of a hybrid circuit breaker.

IGBT and IEGT are more suitable for high current interruption, while IGCT is better for low voltage high current HCBs due to its low on-state voltage and high surge current conduction ability as discussed in [23]. HCBs can be classified into two major categories discussed below:

2.6.3.1 Hybrid DCCB for Single-Terminal Protection

The first category is hybrid DCCB for single-terminal protection. The single terminal can be anywhere, it can be HVDC source, transmission lines, or load. As in the case of HVDC, all the components are very expensive thus protection is required everywhere. The prototype of HDCC comprised a mechanical switch and a solid-state switch. The mechanical switch carries the load current, but in a short circuit, it redirects the current to the solid state switch due to a voltage drop difference. The solid-state switch stops when the mechanical switch can handle the transient recovery voltage, interrupting the fault current. Energy is dissipated by a metal oxide varistor present in the main branch of the breaker. The schematic of HDCCB is depicted in Fig. 2.7. HCBs enhance cost and performance by combining load commutation switches (LCS) with ultra-fast disconnectors (UFD), IGBts, main breakers, and metal oxide varistors (MOVs). These components allow current to commutate to the main breaker branch. These components allow current to commutate to the main breaker branch, resulting in a 2ms breaking time. Innovations like liquid metal LCS and two-stage commutation circuits provide arc-less switching and improved fault current interruption as explained in [38, 41, 54].

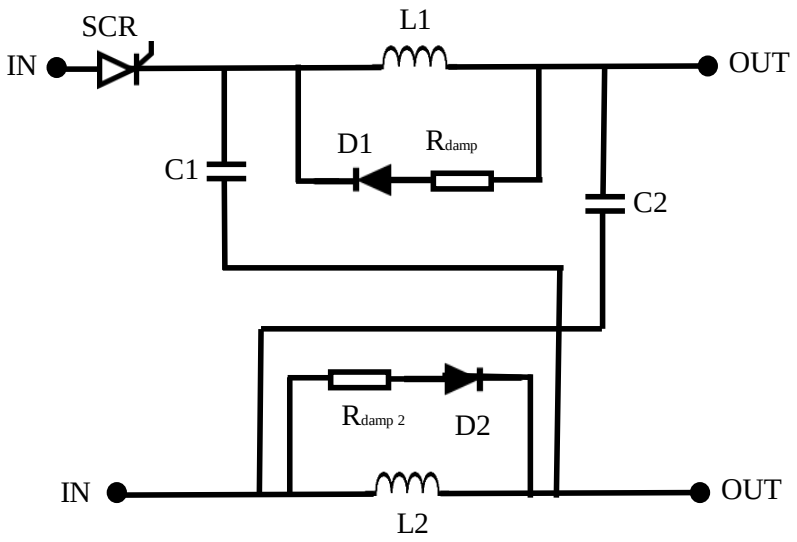

FIGURE 2.8: Diagram of Z-source circuit breaker.

2.6.3.2 Multi-Port Hybrid HVDC Circuit Breakers

Multi-port hybrid HVDC circuit breakers are attractive for their technical and economic benefits, as they can protect multiple transmission lines, sources, or loads, reducing construction costs and power losses. A novel multi-port HCB for offshore multi-terminal HVDC applications has n-ports that interrupt fault current independently, reducing surge arrester size and costs [13]. Two bridge-type integrated HCBs are developed to reduce controllable semiconductor devices and protect HVDC grids from faults [55]. A new multi-port HCB with soft reclosing capability is also developed. [56]. Thus, in HVDC, the interest of industry and researchers has shifted toward the improvement and development of multi-port circuit breakers, so that economically solutions viable solutions can be presented in the future.

2.6.4 Z-Source Circuit Breakers

The Modified Z-source circuit breaker topologies are innovative designs that enhance DC circuit breaker performance by utilizing unique inductor configurations, improving current flow management, reducing stress on switching components, and ensuring cost-effectiveness, as discussed in [41]. The general schematic of ZSCB is represented in Fig. 2.8. Below is a comprehensive explanation of the various modified ZSCB topologies:

2.6.4.1 A Crossed-Connected Inductor Topology

is used in ZSCB to reduce stress on switching devices and make the circuit simpler and more cost-effective. This design minimizes the need for heavy-duty components for handling high currents, prolonging the lifespan of components. However, the topology lacks voltage gain control, limiting flexibility in dynamic voltage regulation applications, and does not offer overcurrent protection, making it less suitable for systems prone to unpredictable power surges. Despite these drawbacks, the crossed-connected inductors provide an efficient, basic circuit configuration, best suited for applications prioritizing cost and simplicity over advanced control features [42].

2.6.4.2 A Parallel Connected Inductor Topology

employs a crossed-connected inductor topology in ZSCB to simplify and cost-effectively reduce stress on switching devices. This design minimizes the need for heavy-duty components and prolongs component lifespan. However, it lacks voltage gain control and overcurrent protection, making it less suitable for dynamic voltage regulation applications. Despite these drawbacks, the ZSCB is an efficient, basic circuit configuration suitable for cost and simplicity applications as written in [43].

2.6.4.3 A Series Connected Inductor Topology

is used in ZSCB to control voltage gain, making it ideal for dynamic voltage regulation applications. However, it lacks built-in overcurrent protection and adds complexity to the circuit design, making it less straightforward to implement. and reduces current stress on switches, improving system efficiency and longevity. However, it lacks built-in overcurrent protection and adds complexity to the circuit design, making it less straightforward to implement. However, it lacks built-in overcurrent protection and adds complexity to the circuit design, making it less straightforward to implement. Despite these challenges, the ZSCB's ability to handle higher voltages and control current makes it a valuable solution for demanding electrical systems. The topology's adaptability to complex and variable power requirements is its primary advantage as mentioned in [44].

2.6.4.4 A Bi-Directional ZSCB Uses Cross-Coupled Inductors

to enable bi-directional power flow, making it ideal for reversible power applications. This topology reduces current stress on switches, improving their durability and efficiency. It is suitable for advanced electrical systems with critical reversible power operation. However, the design presents challenges due to the complexity of the cross-coupled inductor arrangement and its lack of widespread commercialization. Despite these challenges, the ZSCB offers a robust solution for bidirectional power control, albeit at a higher cost. Despite these challenges, the ZSCB offers a robust solution for reversible power control in advanced electrical systems [45].

2.6.4.5 A Bi-Directional ZSCB Topology Utilizes Parallel Inductors

to facilitate bi-directional current flow and minimize current stress on switches. This design offers low current stress and versatile bidirectional power flow, making it suitable for various applications. However, it has drawbacks such as a complex structure, high design cost, and not yet reaching commercial viability. The diagram illustrates two parallel inductors allowing current flow in both directions, with additional switches for control.

2.7 A Comprehensive Review of Single-terminal Hybrid HVDC Circuit Breakers

A comprehensive review of single-terminal hybrid HVDC circuit breakers is provided in this section. In Table 2.4 various hybrid HVDC circuit breaker topologies and their limitations are discussed. It analyzes critical issues such as longer fault current interruption times, large fault energy dissipation, and extended breaker reset times. Studies show that fault current interruption times are significant, making them unsuitable for many HVDC applications. For instance, the topology in [57] has a fault current interruption time of 47ms, which is unsuitable for many applications. Additionally, the study in [58]

highlights the complexity of precise switching, which increases fault current interruption times. The study in [59] notes a fault current interruption time of 3ms, which is critical for high-voltage applications.

Fault energy dissipation is a common issue in many designs, including the integration of modular multi-level converters with hybrid DC breakers. Studies by [60] and [61] highlight thermal stress and energy dissipation as limiting factors, especially when scaling breakers to handle higher voltages. The work of [12] identifies energy dissipation during fault clearing as a vulnerability, impacting surge-arresting mechanisms' performance. The study in [62] also notes challenges in energy absorption during fault current limiting stages.

Longer breaker reset times can reduce system efficiency and impact the ability to handle successive faults. Research papers emphasize the need for quicker reset times to maintain grid stability, especially in multi-terminal HVDC systems, as noted by [61] and [63]. This issue is particularly noticeable in hybrid-type superconducting circuit breaker designs. The existing HVDC circuit breaker, that necessitate the need for novel solutions that reduce response times, improve energy efficiency, and enhance system reliability, with future research focusing on optimizing breaker topologies.

TABLE 2.4: A summary of recent hybrid HVDC circuit breakers.

Authors	**Year**	**Highlights**	**Limitations**
Xue *et al.* [59]	2022	(i) Allows switching between primary and backup states (ii) Two stages	(i) Requires precise coordination. (ii) Modular nature complicates system installation (iii) Interruption time 3ms
Hasan *et al.* [57]	2024	(i) Regenerative current breaking capabilities (ii) Focused current interruption	(i) Regeneration for LVDC (ii) Interruption time 47ms (iii) Missing comparative study
Mehdi *et al.* [64]	2024	(i) Literature review of hybrid AC/DC networks' protection and fault characteristics	(i) Lack of Original Research (ii) Unexplained transient fault behaviors

Continued on next page

Table 2.4 – continued from previous page

Authors	**Year**	**Highlights**	**Limitations**
Ludin *et al.* [65]	2023	(i) Fault Current Limiter and Resonant topology (ii) Passive and active components for fault disconnection	(i) Fault Detection and Coordination Challenges (ii) FCL and a HRB increase energy losses (iii) Complex topology
Li *et al.* [66]	2018	(i) Shares main breaker branch (ii) Unidirectional and bidirectional interruption	(i) Increased Maintenance Costs (ii) Interruption is larger than 5ms (iii) Complexity and integration issues
Xu *et al.* [67]	2023	(i) A aging-dependent failure rates in CB discussed	(i) Aging prediction faces inherent complexity (ii) Integration difficulties, limited data available (iii) Limited for sudden failures
Kamalinejad *et al.* [68]	2023	(i) Thyristor-based hybrid DCCB. (ii) Injects active pulses with controllable amplitude and width	(i) Slow turn-Off characteristics (ii) Face challenges in coordinating with the MMC (iii) Complexity of fault identification and auto-reclosing mechanism
Liu*et al.* [69]	2023	(i) Two coupled inductors (ii) Adaptive reclosing	(i) Complexity of dual-coupled inductor design (ii) Aging and degradation of inductors (iii) More space required
Zhang *et al.* [70]	2023	(i) Uses thyristor commutation module (ii) 3kV/6kA prototype experiment	(i) Interruption time 3.5ms (ii) Fault current regeneration ignored (iii) Slow turn-off of thyristors
Luo *et al.* [71]	2024	(i) Based on flying capacitor multilevel injector (FCM-SHCB) (ii) Multilevel characteristic studied	(i) Adding complexity for precise voltage balancing (ii) Suitable for LVDC (iii) Increased size, cost

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Table 2.4 – continued from previous page

Authors	**Year**	**Highlights**	**Limitations**
He *et al.* [72]	2023	(i) Dual-core-CPU architecture is utilized (ii) Controller hardware-in-the-loop (CHIL) model of EDISON breaker	(i) For LVDC applications (ii) Dependence on CHIL simulations (iii) Full-scale high-power tests ignored
Alashi *et al.* [73]	2024	(i) Optimization of high-temperature superconducting air-core pulse transformer (ii) Prototype at 600V/30A and 5kV/150A	(i) Larger and heavier than iron-core transformers (ii) Lack of magnetic core increases coil sizes (iii) Increased size (iv) Complex integration (v) More energy loss
Yan *et al.* [74]	2023	(i) Transformer and metric meta-learning model for quick diagnosis (ii) Hybrid transformer-convolutional neural network for fault feature extraction	(i) Limited high-quality data availability (ii) Sensitivity to data imbalance (iii) Complexity and scalability issues
Moghbeli *et al.* [12]	2024	(i) Harnesses voltage rise due to fault (ii) Surge arrestor and freewheeling diodes utilized	(i) Increased size (ii) Complex design and control (iii) High cost (iv) Thermal and electrical stress (v) Energy dissipation issues
Xue *et al.* [61]	2024	(i) Addresses current limiting and interruption (ii) Bi-directional interruption	(i) High cost (ii) Fast interruption ignored (iii) Energy dissipation, thermal stress, component degradation (iv) Over-voltage risk
Khan *et al.* [75]	2021	(i) Vaccum circuit breaker (VCB) plus SiC-MESFET topology	(i) Zero crossing challenge (ii) Interruption after 3.8ms (iii) Thermal management issues (iv) Energy dissipation losses

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Table 2.4 – continued from previous page

Authors	**Year**	**Highlights**	**Limitations**
Zhang *et al.* [76]	2021	(i) Thyristor and IGBT half-bridge submodules (ii) IGBT half-bridges for negative voltage to thyristors	(i) Complex circuit design, with multiple branches (ii) Performance variability (iii) Limited scalability (iv) Impact on switching speed and dynamics (v) Cost considerations
Khan *et al.* [63]	2015	(i) Superconducting DCCB model (ii) FCL + IGBTs h	(i) Interruption time compromised (ii) Energy dissipation ignored (iii) Reset time larger
Wang *et al.* [60]	2019	(i) Half-bridge MMCs. (ii) Fault detection and discrimination algorithm	(i) Integration is complex and costly (ii) Increased maintenance demands (iii) Thermal stress (iv) System stability risks (v) Communication and data handling issues (vi) Energy dissipation challenges (vii) System coordination difficulties
Feng *et al.* [77]	2020	(i) Repositioned current commutation module (CCM) and redesigned high-voltage solid-state switches (HVSS)	(i) High voltage and current stress (ii) Fault interruption complexity (iii) Slow response time limitations (iv) Complex control (v) Time constraints in energy absorption
Mei *et al.* [58]	2021	(i) An energy absorption branch (EAB), and a freewheeling branch (FB) achieve fault current absorption	(i) Complex topology (ii) Precise switching required (iii) Control system (iv) Energy dissipation challenges (v) 5ms interruption time.

Continued on next page

Table 2.4 – continued from previous page

Authors	Year	Highlights	Limitations
Yu *et al.* [78]	2023	(i) Two types of power electronics for interruption (ii) A 10kV/60kA breaking test	(i) Complexity of mixed switches (ii) Limited current handling (iii) Complex control
Miyara *et al.* [79]	2020	(i) Resonant CB with soft switching	(i) Increased system size and weight due to large inductors and capacitors (ii) Ignored fault current regeneration (iii) Complexity of resonant circuit design
Li*et al.* [62]	2019	(i) Topology for current limiting DCCB (ii) Inductor branches can be increased	(i) Energy Dissipation Challenges (ii) Control System Complexity (iii) Interruption time is 5ms
Lumen *et al.* [80]	2022	(i) Regenerative capabilities (ii) Capacitor to store energy	(i) Bi-directional power flow ignored (ii) Higher component requirements (iii) Interruption time 38ms (iv) Reset time 47ms

2.8 A Critical Review of Multi-port Hybrid HVDC Circuit Breakers

This section provides a critical review of multi-port hybrid HVDC circuit breakers by analysing important issues about fault current interruption time, fault energy dissipation, and breaker reset time, summarized in Table 2.5. Shorter interruption times are crucial for maintaining system stability in multi-terminal HVDC grids. However, several circuit breakers exhibit delays in fault clearance, such as a study in [81] has fault current interruption time exceeding 3ms, the study in [82] suffers with interruption times greater than 9.8ms, and a design that replaces the work in [83] with fault interruption

times over 4ms. Extended interruption times in HVDC systems hinder fault isolation, dissipating fault energy, and addressing breaker reset time. These limitations need to be addressed through innovations in control logic and component design for improved protection in multi-terminal HVDC grids.

Efficient fault energy dissipation is crucial for protecting system components from damage during fault events. Current designs face challenges in managing high-energy dissipation, leading to increased component stress and potential failure as discussed in [84]. Metal-oxide varistors (MOVs) and large surge arresters are used in [85], for energy dissipation, but these methods are inefficient and costly, particularly in large-scale systems. They do not scale well for higher voltages and larger grids. Alternative technologies for energy dissipation, focusing on performance and compact design, are needed to address these issues. Examples include metal-oxide varistors, surge arresters, separate branches and shared breaker branches.

The critical issue of longer breaker reset times, inefficient fault energy dissipation, and longer fault current interruption times is essential for the protection of multi-terminal transmission systems. Current topologies either fail to address this aspect or have complex designs that result in longer reset times, reducing system efficiency. Examples include the 8.3ms fault interruption time in [86] and the slow reclosing times in [87]. Future designs should focus on faster and more efficient reclosing mechanisms to minimize system downtime after faults are cleared. To meet the demands of future HVDC grids, particularly those involving multi-terminal configurations, these gaps need to be closed through innovations in control logic and component design.

TABLE 2.5: A critical overview of multi-terminal hybrid HVDC circuit breakers topologies.

Authors	**Year**	**Highlights**	**Limitations**
Zhang *et al.* [88]	2022	(i) Features current limiting inductors, diode, thyristor, load commutation, and semiconductor switches	(i) Coordination risk between CLIs, MB & IBB branches (ii) Complex control (iii) Bidirectional current interruption is ignored (iv) High costs

Continued on next page

Table 2.5 – continued from previous page

Authors	**Year**	**Highlights**	**Limitations**
Tu *et al.* [89]	2022	(i) DC bus fault conditions analyzed (ii) For single, multi-line, & two consecutive faults	(i) Bus fault affects healthy lines (ii) Interruption time 1000ms (iii) Complex topology due to diode and thyristor stacks
Pu *et al.* [90]	2024	(i) Self-charging, current-passing, transfer, current-limiting, current-cutting, and ground bypass branches (ii) Capacitors for polarity reversal loops	(i) Excessive branches add complexity (ii) Maintenance is more challenging (iii) Delayed interruption
Dai *et al.* [91]	2024	(i) Property identification of fault, temporary or permanent fault (ii) Multiple stages are involved	(i) Integration complexities with fault current limiting, soft reclosing, and fault-property identification (ii) fault zone, property, and protection identification cause delay (iii) Large surge arresters increase cost
Zou *et al.* [92]	2023	(i) Overview of existing multiport topologies	(i) Limited review. (ii) Interruption not discussed. (ii) Quick fault energy dissipation ignored.
Ravi *et al.* [93]	2023	(i) Type-I module – MOV (ii) Type-II module, with a MOV-resistor capacitor Network	(i)Thermal stress from hard switching. (ii) Higher turnoff currents require enhanced thermal capabilities (iii) Combined soft switching and hard switching circuit issues
Gan *et al.* [94]	2023	(i) Experimental validation is performed at the 15kV/15kA level	(i) Actual grid conditions with higher voltages ignored (ii) Interruption time 3ms (iii) Complex topology with solid-state,and diode stacks.

Continued on next page

Table 2.5 – continued from previous page

Authors	**Year**	**Highlights**	**Limitations**
Zhu *et al.* [83]	2023	(i) Load the current switch (LCS) and replace it with a simple bridge arm circuit	(i) Replacement of LCS with bridge arm circuit introduces complexities (ii) Capacitor pre-charging and discharge issues (iii) Timing and reliability issues (iv) Interruption time 4ms
Shuo *et al.* [86]	2022	(i) Distinguish temporary & permanent faults (ii) Offers soft reclosing	(i) Interruption time is 8.3ms (ii) Temporary and permanent fault differentiation challenge (iii) Breaker reclosure time is ignored
Liu *et al.* [85]	2019	(i) Main selector (MS) at each port (ii) Commutation branches	(i) Large size due to various branches and stages (ii) Complex controls algorithm (iii) Interruption time is 9.3ms (iv) Precise switching required (v) Huge arresters.
Chen *et al.* [95]	2023	(i) Double-pole DC grids (ii) LCSs, thyristor, CLIs, resistor, capacitor, and diodes to suppress over-current & voltages	(i) Adaptive reclosing causes delays in fault detection (ii) Complicated energy management at fault (iii) Capacitor charging and discharging issues (iv) Interruption time 6.35ms
Zhang *et al.* [81]	2021	(i) Unidirectional conductivity of switches (ii) Control procedure for UFD failure	(i) Interruption time 3ms (ii) Complex arrangement of UFDs, RCBs, and diodes (iii) Maintenance costs (iv) Quick energy dissipation issues
Ding *et al.* [82]	2023	(i) Working principle and controls explained (ii) Fault isolation process discussed	(i) Higher costs. (ii) Interruption time 9.8ms (iii) Large circuitry for energy dissipation

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Table 2.5 – continued from previous page

Authors	Year	Highlights	Limitations
Pei *et al.* [96]	2023	(i) Four terminal HVDC system (ii) Controllable oscillation circuit	(i) Precise resonance circuit required (ii) Quick fault energy dissipation issues
Xue *et al.* [87]	2021	(i) Thyristors (ii) CLIs for current suppression	(i) Thyristor groups control challenge (ii) Slow reclosing (iii) Both IGBTs & thyristors required (iv) Increased volume & cost

2.9 Research Gaps

A gap analysis of key challenges in multi-terminal HVDC transmission system protection is given below:

- Fault energy in MTDC systems is large, making it impractical to install a large surge arrester for fault clearance even after the fault has been interrupted. Large surge arresters and other energy absorption mechanisms are used to manage fault energy, but they increase the size, cost, and complexity of circuit breaker designs as discussed in studies [62, 87, 93]. This makes fault energy management difficult, especially in high-power and space-constrained environments. A potential solution is to regenerate some dissipated energy after fault current is interrupted, reducing reliance on surge arresters, decreasing the size and cost of circuit breaker designs, and enhancing the performance and reliability of HVDC transmission networks.

- Longer fault current interruption time is a major limitation in HVDC transmission networks, primarily due to the low transmission line impedance in HVDC systems, which causes fault currents to rise rapidly. Unlike AC systems, HVDC networks experience significantly longer fault current rise that can damage the transmission network within milliseconds, which poses a threat to both single-terminal and

multi-terminal configurations. This extended interruption time delays the isolation of faulted sections, increasing the risk of widespread system instability and equipment failure. Although advanced technologies like [65] and [57] have been developed, they still exhibit interruption times between 3.8ms and 47ms, which are inadequate for the rapid fault clearance needed in HVDC systems to protect against system failure. Thus, reducing fault current interruption time is crucial for enhancing the reliability and safety of HVDC networks.

- The development of HVDC hybrid circuit breakers faces a research gap in reducing the breaker reset time. This process, which involves managing system currents and executing precise steps, is crucial for restoring normal operation after a fault. However, the extended reset times required by modern circuit breaker designs present significant challenges, such as delayed system recovery, network instability, and cascading failures. Addressing this delay is essential for enhancing the scalability and reliability of multi-terminal HVDC systems, making minimization of breaker reset times an essential area of further research as highlighted in numerous studies [26, 38, 87].

2.10 Problem Statement

The implementation of hybrid HVDC circuit breakers faces two major challenges in single-terminal and multi-terminal HVDC transmission systems. First, slow fault interruption and delayed breaker reset times, reduce system performance. Second, a large amount of fault energy needs to be dissipated after interruption, requiring bulky energy-dissipating devices that make practical implementation difficult. Solving these problems is crucial for the development of multi-terminal HVDC networks.

2.11 Proposed Methodology

To address the stated challenges, this research proposes the following methodologies:

- The research proposes two hybrid DCCB topologies to address large fault energy dissipation in MTDC systems: modular hybrid DCCB with fault current self-adaptive control and protective coordination (MHDCCB) and improved hybrid DCCB with battery banks for energy storage (HDCCB). The MHDCCB features a two-stage current limiting mechanism that extends the current limiting duration and adapts to primary and backup protection. The improved HDCCB topology uses a resistor-inductor-capacitor resonance to create current zero-crossings and store inductive energy from network faults in battery banks for future use. Both topologies integrate battery banks to store the breaker's energy during fault events. However, the major setback is increased system cost due to occasional faults and battery degradation or unused usage.

- A novel regenerative hybrid high-voltage direct current circuit breaker (HDCCB) topology is proposed to address the limitations of installing battery banks for breakers' energy storage after interruption. This approach introduces fault current regeneration, regenerating fault energy during fault occurrence and sending it back to the grid for future use. The topology minimizes fault current interruption and breaker reset time, allowing fault interruptions under 2ms and restoration to normal operation within 5ms. It features a current-limiting branch to reduce peak fault currents and a compact topology with reduced component count, simplifying control schemes and improving integration with HVDC systems. The regeneration feature enables the recovery and reuse of 1.5MJ of fault energy, surpassing the traditional topology 17.07kJ.

- A novel hybrid multi-port direct current circuit breaker (HMPDCCB) topology is proposed for protecting multiple transmission lines using a single HMPDCCB. This design reduces the breaker's size and cost by using a common main breaker branch for all transmission lines during fault events. The breaker efficiently protects high-voltage direct current systems, reducing current interruption time to under 1.8ms and resetting within 3ms. It also incorporates a fault current regeneration feature, retrieving 0.35MJ of energy, and employs current-limiting inductors to prevent sudden surges. A simplified controller monitors the voltage across

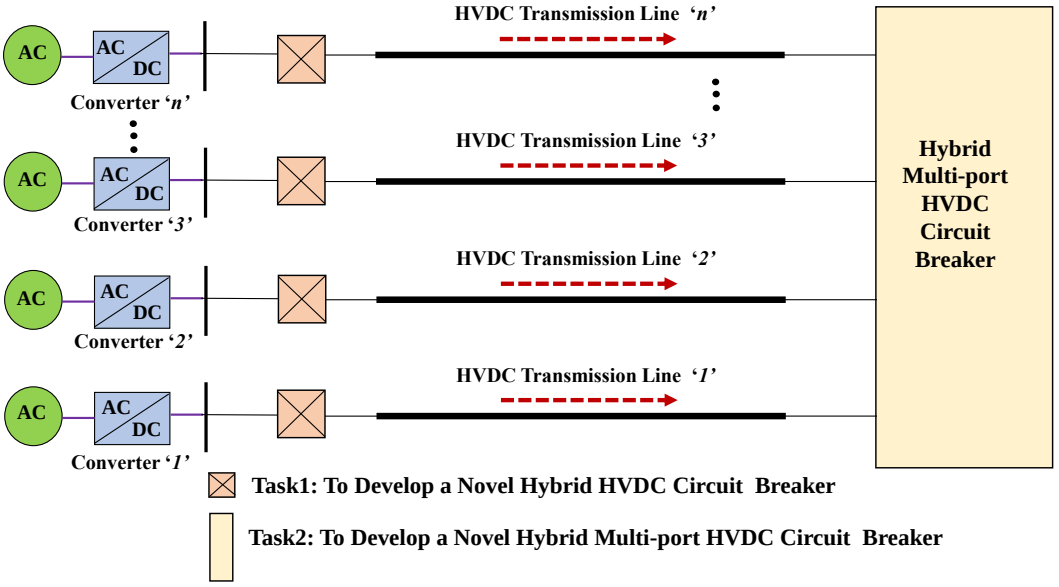


FIGURE 2.9: The proposed area of research.

CLIs to identify fault lines, selecting the port with the minimum voltage as the receiving port for regenerated energy.

- A new compact design simplifies control schemes and is also compatible with n-terminal HVDC systems.
- The performance of the HMPDCCB is thoroughly analyzed and validated against existing circuit breaker topologies.
- Fig. 2.9 depicts protection for single terminals as a first task, while multi-terminal protection extends the first task.

2.12 Chatper Summary

This chapter explores high-voltage direct current circuit breaker topologies, highlighting their crucial role in integrating large-scale renewable energy sources into modern electrical grids. The growing demand for HVDC systems, driven by the need to connect remote renewable energy generation sites, presents unique technical challenges, particularly against fault protection. The chapter compares alternating current circuit

breakers (ACCBs) and direct current circuit breakers (DCCBs), highlighting the differences in handling fault currents. It also reviews traditional circuit breaker topologies, including mechanical circuit breakers (MCBs), solid-state circuit breakers (SSCBs), hybrid circuit breakers (HCBs), and z-source circuit breakers (ZSCBs). The chapter identifies research gaps and challenges, formulates a problem statement, proposes a methodology, and establishes the foundation for further investigation and development of HVDC circuit breaker topologies.

Chapter 3

Harnessing Inductor Energy in Hybrid HVDC Circuit Breaker

This chapter highlights the need for an efficient direct current circuit breaker (DCCB) to support the expansion of multi-terminal direct current (MTDC) transmission systems. The literature review reveals that one of the key challenges in developing novel DCCB topologies is the substantial energy dissipation during fault clearance, particularly in high-voltage direct current systems. This chapter presents two topologies of DCCBs, each integrating battery banks to store fault energy after fault current interruptions. This enhances fault management efficiency by harnessing energy dissipated during fault events. The topologies, specifically hybrid HVDC circuit breakers, represent innovative advancements in HVDC protection systems, ensuring reliable and efficient operation during fault conditions. Conventional DCCB topologies typically rely on large surge arresters, but this approach leads to increased breaker size and cost. The proposed topologies aim to mitigate these issues by exploring alternative energy storage solutions. The ultimate goal is to enable energy regeneration during fault clearing. The ultimate goal is to enable energy regeneration during fault clearing allowing fault energy to be redirected back to the grid for future use, and improving the efficiency and sustainability of DCCB systems. The analysis and implementation of these topologies will be discussed in Sections 3.3 and 3.4, exploring their design, energy storage mechanisms, fault-handling capabilities, and results discussion in detail.

3.1 Introduction

This research proposes a novel direct current circuit breaker topology to address fault energy dissipation during fault clearance. The topology focuses on the reuses of breaker inductor energy. The system initially consists of a simple HVDC test, with normal current and voltage observed from the source to load HVDC transmission. A fault is created, and results are observed—the novel topology stores breaker inductor energy in battery banks, allowing better utilization for future applications. The main aim is to reduce fault current interruption and breaker reset times. Still, initially, large fault energy dissipation issues are resolved by storing energy in battery banks for future reuse. The results have been published in various conferences, with titles; improved hybrid DC circuit breaker for HVDC systems topology and modular hybrid DC circuit breaker with effective fault clearing and energy storing capability. Resistor-inductor-capacitor oscillations create zero crossing, and by dumping fault energy in the main breaker branch respectively, and after the interruption, some breaker inductor energy is stored in battery banks. The battery's state of charge indicates that the energy is stored in the battery.

3.2 A Simple HVDC Transmission Test-bed in Simulink®/Simpowersystems

A high-voltage direct current (HVDC) transmission system that converts alternating current (AC) into direct current (DC) for efficient long-distance transmission and back to AC for distribution is shown in Fig. 3.1. The AC source is connected to a transformer, which steps up the voltage for better transmission. The AC source is connected to a transformer, which steps up the voltage for better transmission. The stepped-up AC is fed into a rectifier, which converts AC into DC using MMC. This system offers higher efficiency, reduced line losses, and lower infrastructure costs compared to AC systems. Due to its superior efficiency and reduced transmission losses, it is widely used for long-distance power transmission, especially in renewable energy integration MTDC.

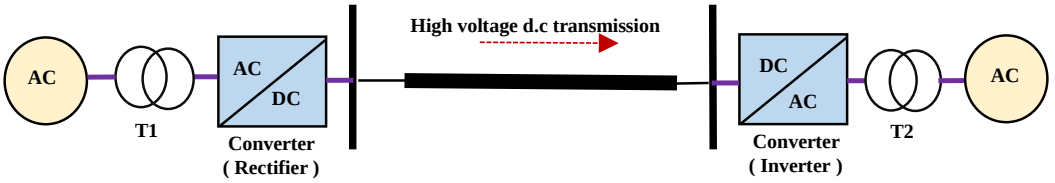


FIGURE 3.1: A typical HVDC transmission system.

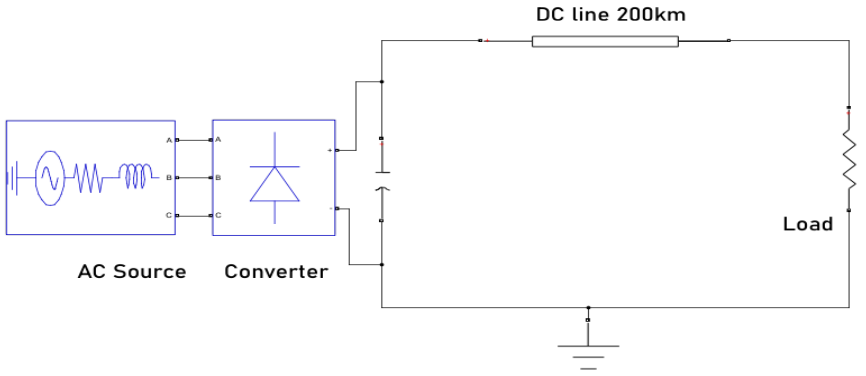


FIGURE 3.2: A 400kV HVDC transmission system serves as a test-bed for performance evaluation.

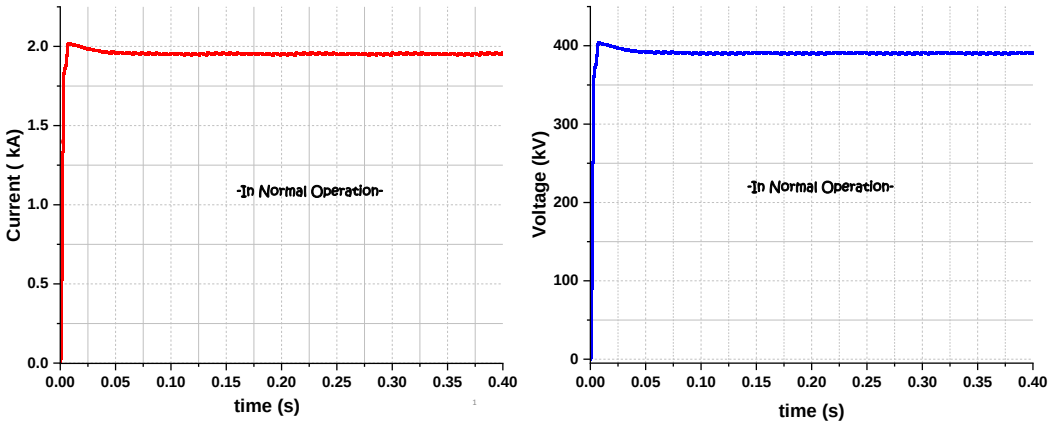
3.2.1 A 400kV HVDC Transmission System

A MATLAB test-bed for HVDC transmission is developed to validate the effectiveness of a proposed circuit breaker within the HVDC network, as shown in Fig. 3.2. The system starts with an AC source, derived from renewable sources like wind turbines, hydroelectric power, or biomass. A step-up transformer is used to increase voltage, followed by a rectifier that converts AC to DC. The rectifier is implemented using a modular multi-level converter (MMC), which efficiently converts HVAC generated at the source into HVDC. The HVDC is transmitted over long distances through an HVDC transmission line to minimize power losses. At the receiving end, another MMC acts as an inverter, converting the transmitted HVDC back into AC for distribution to the load.

A comprehensive test setup was modelled using Simulink®/Simpowersystems to analyze the working principles and fault current interruption performance of an HVDC circuit breaker. The test-bed consists of a VSC-HVDC converter station connected to a mono-polar HVDC transmission network, operating at 400kV DC voltage and 2kA load

TABLE 3.1: Parameter values of the HVDC test-bed model.

Parameter	**Specification**
VSC HVDC type	Mono-polar/multi-level
MTDC grid voltage	400kV
Normal load current	2kA
AC system X/R	7
HVDC line length	200km



(a) Normal current (b) Normal voltage

FIGURE 3.3: Current and voltage of a normal HVDC transmission system.

current. The HVDC transmission line spans 200km, allowing for long-distance transmission efficiency assessment. These parameters accurately reflect real-world conditions, making it a valuable tool for evaluating the functionality and effectiveness of the HVDC circuit breaker under various fault scenarios. To analyze the working principles and fault current interruption performance of the HVDC circuit breaker, a testing set-up was modelled in Simulink®/Simpowersystems. Table 3.1 below summarizes the general features of the test-bed model. The test-bed contains a two-level VSC-HVDC converter station with a mono-polar HVDC transmission network. Test-bed voltage = 400kV, normal current = 2kA, as depicted in Fig. 3.2. The HVDC transmission line length = 200km. As we know, $\frac{X}{R} = \frac{2\pi fL}{R}$. In Ac side as frequency, inductance and resistance are 50Hz, 2.23mH, and O.1Ω respectively, thus $\frac{X}{R}$ found as 7.

Furthermore, the table provides key specifications for the HVDC test-bed system. It features a Mono-polar/two-level VSC HVDC type for efficient long-distance power transmission, with a 400kV DC MTDC grid voltage to minimize transmission losses over 200km. The system operates with a 2kA normal load current and an AC system X/R

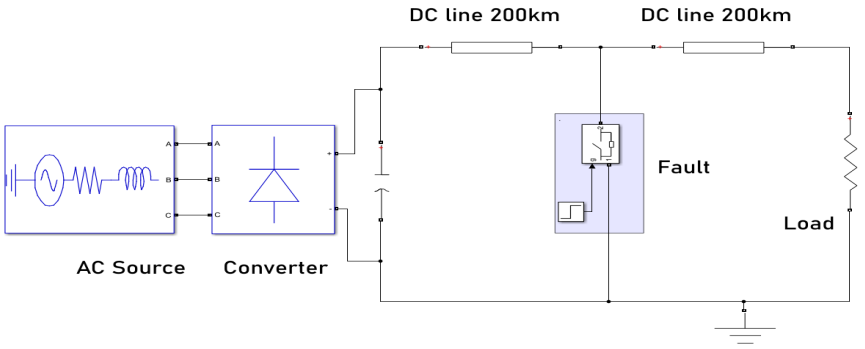


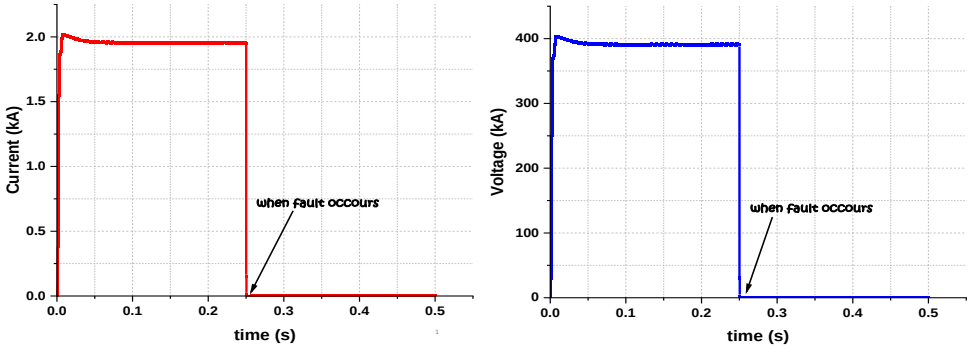
FIGURE 3.4: The HVDC transmission system with a fault.

ratio of 7, affecting converter performance and ensuring accurate simulation and testing of the HVDC model. Moreover, the graphs in Fig. 3.3 show the normal current and voltage behaviour of an HVDC transmission system during normal operation. The first graph shows a normal current of 2kA, while the second graph shows a normal system voltage of 400kV, indicating normal functioning. These graphs provide a clear understanding of the system's performance.

3.2.2 The HVDC System During a Fault

An HVDC transmission system with a fault scenario is depicted in Fig. 3.4. The system begins with an AC source. This AC is converted into DC using a rectifier, reducing power losses over long distances. The power is then transmitted over long distances through two 200km long DC transmission lines. A fault may occur on one of these lines due to issues like ground faults, disrupting power flow. A hybrid circuit breaker is likely the highlighted component, designed to protect the system during a fault. It detects the fault and isolates the faulty section from the rest of the system to prevent damage or outages. The load at the end of the system represents the power demand, such as an industrial plant or city drawing power from the HVDC transmission line. The system is designed with protective elements, such as a hybrid circuit breaker, to handle such situations.

The results of system voltages and currents in Simulink®/Simpower systems are shown in Fig. 3.5. It explains that when a fault occurs in the system, the normal currents and the voltages of the system go down. For instance, in normal cases, the system current



(a) Current (b) Voltage

FIGURE 3.5: Current and voltage of the HVDC transmission system from normal to fault occurrence.

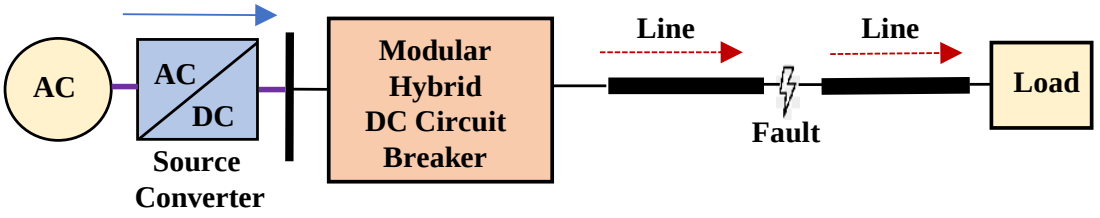


FIGURE 3.6: The modular hybrid DCCB installed in the HVDC transmission system.

was 2kA and voltages were 400kV but when a fault occurs at 0.25s the system currents and voltages go down to zero at that time.

3.3 The Proposed Modular Hybrid DCCB Topology with Fault Current Self-adaptive Control and Protective Coordination

A modular hybrid DCCB in an HVDC transmission system is proposed here, as shown in the diagram in Fig. 3.6. It has an AC source, an AC/DC converter, a DCCB, a transmission line, a fault, and a load. The DCCB protects the system duringtransmission line, a fault, and a load. The DCCB protects the system during fault conditions by breaking the circuit, while the load draws power from the HVDC network, ensuring system stability. A modular hybrid direct current circuit breaker (MHDCCB), takes

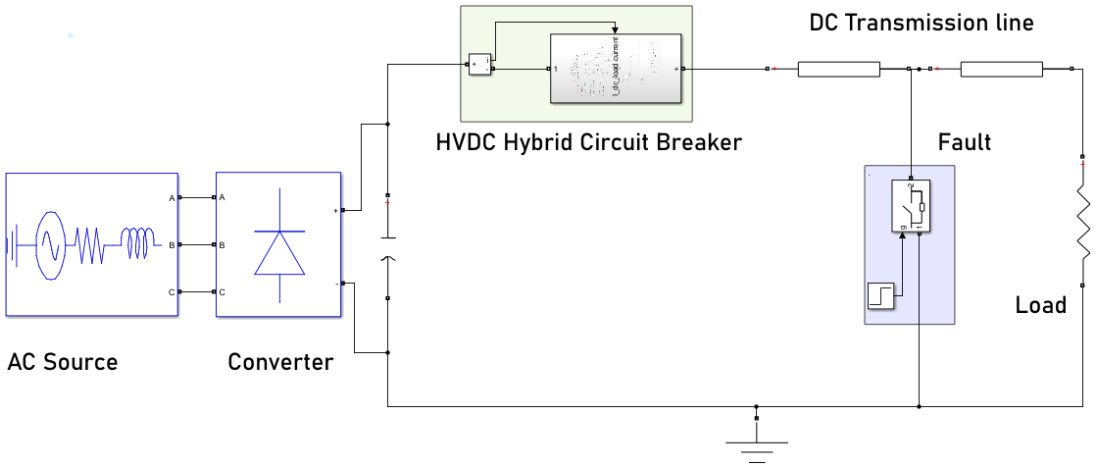


FIGURE 3.7: The modular hybrid DCCB installed in the HVDC transmission system.

advantage of both mechanical and solid-state breakers, the low-loss and fast-breaking characteristics are suitable for the HVDC system. The new topology can be switched to the primary current-limiting state and backup current-limiting state, which reserves enough time for fault detection and location. Recent studies rarely link fault control with main and backup protection. Before backup, the converter station is blocked. The MHDCCB as illustrated in Fig. 3.7 use self-adaptive fault control. Fault-control and protection combination inspired by this MHDCCB has three major benefits:

- The topology two-stage current limiting stage can significantly increase the current limiting duration and self-adapt to primary and backup protection.
- The converter station can be prevented from being blocked in the event of a transmission line accident.
- Following the protection trip signal, the current-limiting reactor speeds fault current cleaning bypasses.

3.3.1 Operation Stages of the MHDCCB

The operation states of the proposed MHDCCB with a progression of states are illustrated in Fig. 3.8. The breaker operates in five states: normal operation, which is the standard state without faults; commutation, which prepares for a transition; primary

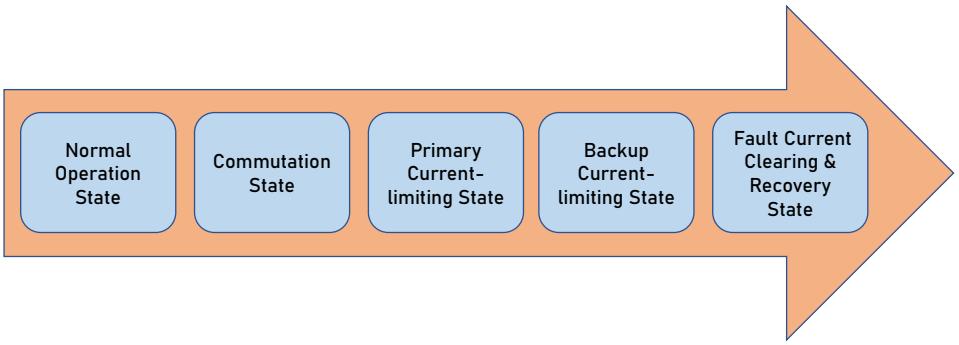


FIGURE 3.8: The operation states of the MHDCCB.

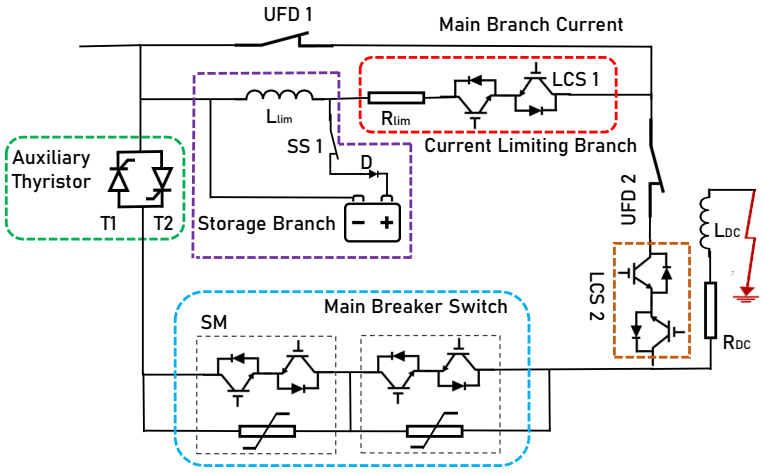


FIGURE 3.9: The topology of the modular hybrid DC circuit breaker.

current-limiting, which limits current due to overload or fault; backup Current-limiting, which reduces current if the primary system fails; and fault Current Clearing and recovery, which clears fault current and restores the system to a stable state.

3.3.2 The Proposed Topology of the MHDCCB

The Schematic of the proposed MHDCCB is shown in Fig. 3.9 which is a combination of the solid-state and mechanical switch for fast current breaking. The topology consists of several key branches, including:

- Main branch comprises load commutation switches (LCS) and ultra-fast disconnectors to efficiently supply MHDCCB with a stable, low-loss, and reliable current path (UFD) for enhanced performance and protection during normal operation.

TABLE 3.2: The system parameters for testing the MHDCCB.

System parameter	**Value**
Voltage rated	$U_{dc} = 400$kV
Current rated	$I_{dc} = 2$kA
Parameters of MHDCCB	$L_{lim} = 300$mH; $R_{lim} = 15\Omega$

- Current-limiting branch's current-limiting inductor (L), resistance (R), and LCS control fault current growth and maximum value through an inductor, ensuring the system remains stable and efficient.
- Main breaker branch combines current commutation and energy-consuming branches into sub-modules (SM) for transfer and energy consumption functions. Each SM consists of an IGBT and MOV. The IGBT control signals transfer, restrict, and clear fault currents. This manages fault commutation and energy dissipation.
- Storage branch after a fault current interruption, some of the energy stored in the breakers inductor is redirected to battery banks instead of dissipating.

The system parameters for testing the proposed MHDCCB are given in Table 3.2. The voltage and current ratings are 400kV and 2kA respectively, indicating the maximum HVDC system can handle. The current-limiting reactor's inductance value is 300mH, while the current-limiting resistor's resistance is 15Ω. These parameters are crucial for ensuring the MHDCCB's effective operation during testing and fault conditions.

3.3.3 Working Principle of the MHDCCB

The working principle of the proposed MHDCCB is comprised of five states elaborated below:

3.3.3.1 Normal operation stage (before t_0):

UFDs are kept closed during normal operation, and only the line commutated switch (LCS1) is triggered, as depicted in Fig. 3.10. When the transmission line is not faulted, the MHDCCB can continue to operate for a long time in a low-loss condition.

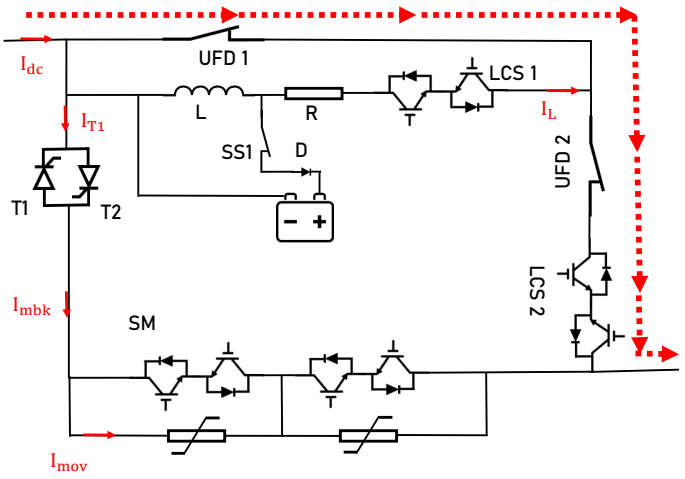


FIGURE 3.10: The normal current path before t_0.

3.3.3.2 Commutation Stage (t_1 to t_2)

The commutation stage, which is a transitional stage, is created to serve two functions: (a) to provide a fault current path before UFD1 has tripped, and (b) to give decision-making time to decide whether to choose a current-limiting stage or a current-clearing stage. The MHDCCB sequentially performs the following actions when the protection system detects over-current and reaches the protection system start-up threshold then trigger all sub-modules of the main breaker branch, continue to trigger the gate pole of the thyristor T1, and block LCS1. UFD1 trips and T1 stops being triggered when all of the I_{dc} has been transferred to the main breaker branch. The present course is depicted in Fig. 3.11. is triggered, blocking all sub-modules on the main breaker branch. Fig. 3.12 depicts the fault current transfer process. red solid lines represent that I_{dc} flows from the branch of the main breaker, which separates into two parts green dotted lines and orange lines. In this process, the current in the

3.3.3.3 Current Limiting Stage (t_2 to t_3)

After the commutation stage, the primary current limiting stage begins to control the rate of rise of the fault current before the arrival of the fault protection trip signal. The following is the MHDCCB's method of control: LCS1 and LCS2 main breaker branches gradually decrease to zero whereas, the current in the current-limiting branch

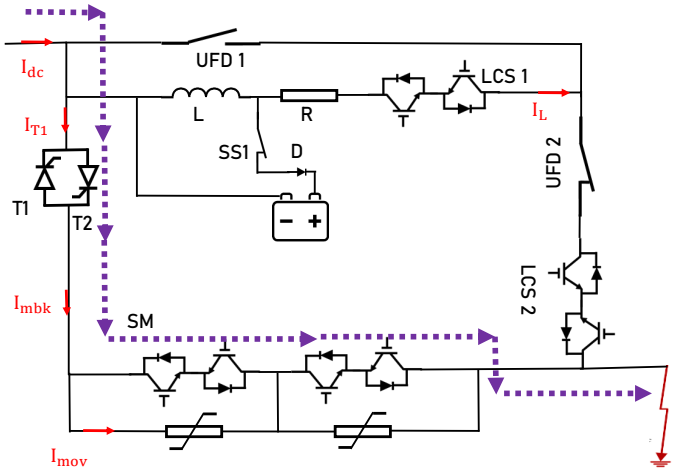


FIGURE 3.11: The commutation path during t_1 to t_2.

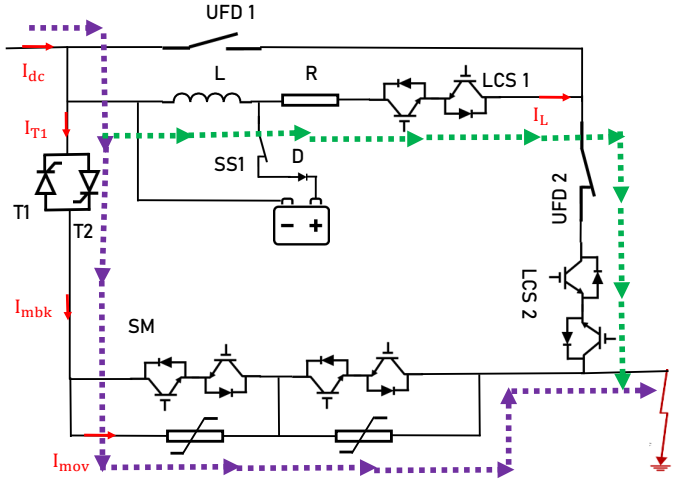


FIGURE 3.12: The primary current limiting paths during t_2 to t_3.

has started rising to $I_L = I_{dc}$. The thyristor T1 will automatically turn off after the commutation is completed.

3.3.3.4 Backup Current-Limiting Stage (t_4 to t_5)

After the primary current-limiting stage is complete, the backup current-limiting stage is meant to stop the secondary rise of the fault current from going beyond the converter's tolerable threshold. This stage ensures enhanced system protection by effectively suppressing excessive current surges and mitigating potential damage. The method is shown in Fig. 3.13. It turns on T2 and all SMs, while disabling LCS1, thereby optimizing fault management and ensuring stable operation under transient conditions.

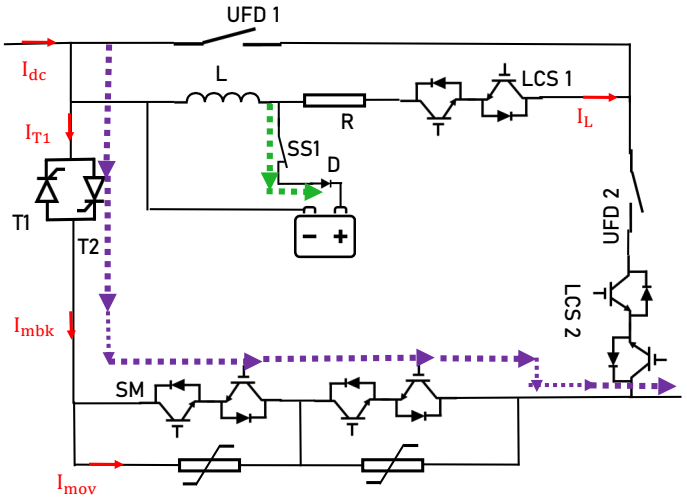


FIGURE 3.13: The backup current-limiting path during t_4 to t_5.

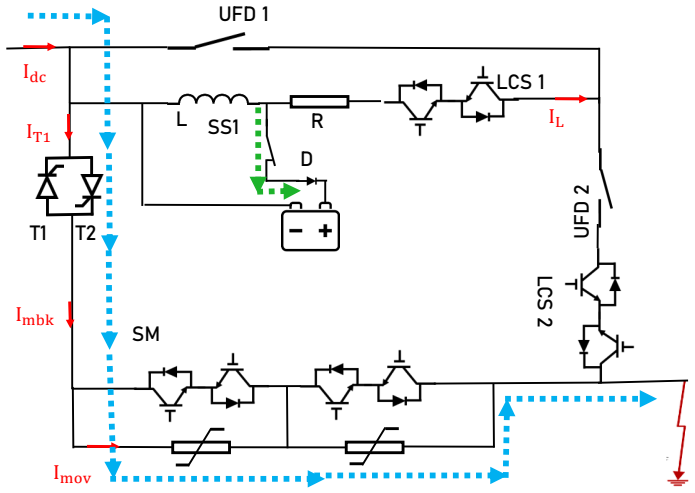


FIGURE 3.14: Fault clearing and recovery path of current during t_5 to t_6.

3.3.3.5 Fault Clearing and Recovery Stage of Current (t_5 to t_6)

As shown in Fig. 3.14, the hybrid circuit breaker operates in response to a protection trip signal. T1 triggers and blocks all SMs, ensuring rapid isolation. All MOVs immediately reduce current to zero, effectively eliminating the fault and preventing excessive overvoltage stress. The recovery condition takes place between fault elimination and normal operation, facilitating seamless system restoration. All semiconductor components except LCS1 are shown to be triggered, maintaining control over current flow. Without initial current I_L, system current recovers rapidly with minimal transient effects. As soon as I_L approaches zero, the MHDCCB closes all UFDs, activates LCS1, and blocks all SMs, restoring primary branch functionality without excessive delay.

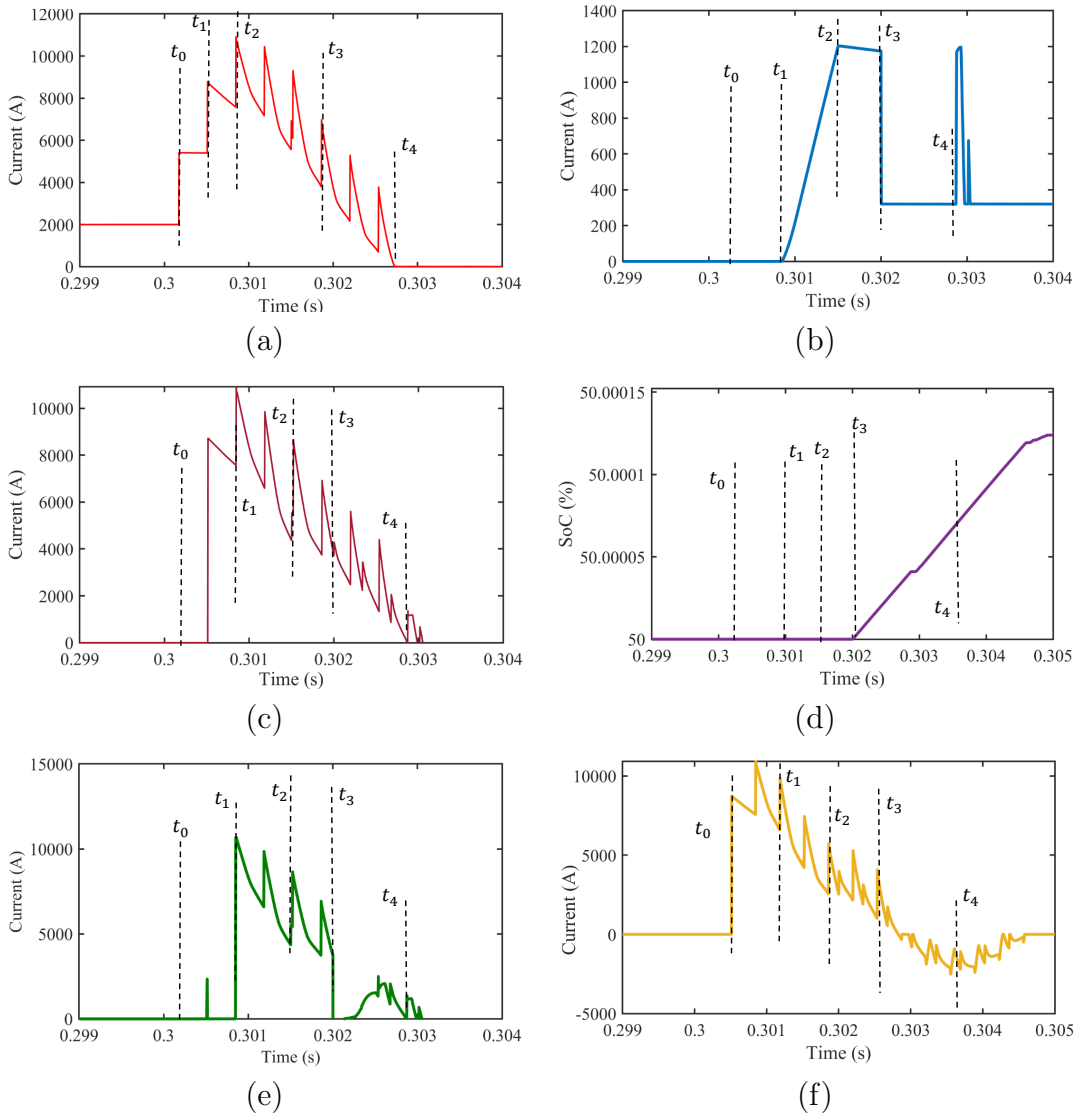


FIGURE 3.15: The simulation results of the proposed modular hybrid high-voltage direct current circuit breaker. (a) Current across the breaker, (b) limiting branch current, fault current limiting state, (c) main breaker branch current, (d) battery charging, (e) current across sub-modules, and (f) current flowing through thyristor T1.

3.3.4 Results and Discussion of the MHDCCB

This section discusses the MHDCCB system, designed and implemented in MATLAB's Simulink®/Simpowersystems. It covers key aspects like current breaking, fault clearing, and inductor energy storage. The simulation results are illustrated in Fig. 3.15, showing the behaviour of parameters during different operational stages, including fault current limiting and battery charging. Each graph provides detailed insights into the system's performance, demonstrating how it manages fault currents and energy.

3.3.4.1 Effective Fault Clearing in the MHDCCB

The MHDCCB is to manage fault conditions in HVDC power systems efficiently. It involves several stages, where different components work together to divert and mitigate fault current. Under normal operating conditions, the current flowing through the system is 2kA as shown in Fig. 3.15(a). When a fault occurs, the current starts to rise rapidly, triggering the fault detection stage. The MHDCCB waits until the current reaches a certain threshold before taking action. By the time t_1, the fault current is diverted from the main branch to the sub-modules. However, the sub-modules are not sufficient to limit the fault entirely, so additional protection mechanisms are needed. When the fault current reaches its peak value of 11kA, the system activates its primary protection stage to limit the fault current and prevent further rise as depicted in Fig. 3.15(b).

The MHDCCB combines solid-state components with mechanical switches to provide rapid response times and efficient energy dissipation during fault events. Its main breaker branch engages and diverts the fault current, ensuring it is fully interrupted and the system can return to normal operation as shown in Fig. 3.15(c). After the fault current is fully diverted and reduced, the system starts charging the battery after complete clearance of fault energy the system will return to normal operation, reconnecting the main breaker branch to the normal current path and disengaging the sub-modules.

3.3.4.2 The MHDCCB's Inductor Energy Stored in the Battery

In the proposed MHDCCB, after the primary fault current has been limited and partially cleared, several processes are initiated to dissipate excess energy, charge the battery, and return the system to normal operation. The battery plays a crucial role in the MHDCCB design by capturing energy that would otherwise be wasted as heat. During fault events, a significant amount of energy is stored in the breaker inductance, specifically in the current-limiting reactor L_{lim} and other inductive components. As the fault current is reduced, this stored energy is transferred to the battery, allowing for efficient energy recovery. This not only prevents energy wastage but also enhances the overall system's

energy efficiency by storing the recovered energy for future use or as a backup during other fault events.

After the battery has begun to charge, the current behaviour across sub-modules and surge arresters is illustrated in Fig. 3.15(d). During the fault-clearing phase, a substantial portion of the fault current is diverted to the sub-modules, which consist of IGBTs and MOVs. These components work together to dissipate the fault current and protect the system from electrical stress as illustrated in Fig. 3.15(e). Surge arresters are essential in protecting the system from transient over-voltages that can occur during the rapid reduction of fault current.

Its current flow through thyristor T1 is almost identical to the DC current under normal conditions, ensuring a seamless transition from fault conditions back to normal operation. Thyristor T2 also plays a significant role in controlling the flow of current during the fault-clearing process. Similar to T1, T2 helps divert current from the main breaker branch to the sub-modules and limiting branch. As the fault current dissipates, the current through T2 gradually decreases, reflecting the successful clearance of the fault. Once the fault has been fully cleared and the system returns to normal operation, the current through T2 approaches zero as shown in Fig. 3.15(f), indicating that it is no longer required to manage fault current.

3.4 The Proposed Improved Hybrid DC Circuit Breaker with Battery Banks for Energy Storage

The section presents a new topology for DC circuit breakers called the improved hybrid DC circuit breaker (HDCCB), which incorporates battery banks to store regenerative energy from network inductance. This approach improves energy efficiency and reduces losses by storing the energy for future use. The proposed topology is tested within an HVDC grid, where power is generated by an AC source and converted to DC through a rectifier for transmission. The system was applied and tested in a 400kV HVDC

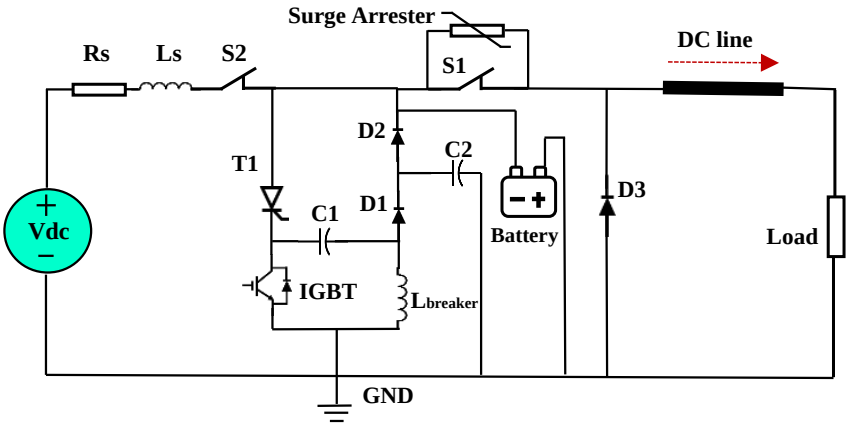


FIGURE 3.16: The schematic of the proposed hybrid DC circuit breaker.

transmission system, demonstrating improved grid performance. The system involves detailed mathematical modelling to explain its operational principles, including the inclusion of battery banks. The working principle involves capturing the energy generated by network inductance during the breaking event and directing it into the battery banks for future use. This innovative approach avoids significant energy losses found in conventional designs and enhances the overall efficiency and performance of the HVDC grid. The success of this topology in a 400kV HVDC system highlights its potential for broader application in modern energy systems.

3.4.1 Construction of the Proposed Improved HDCCB

The schematic of the proposed improved hybrid DC breaker, as shown in Fig. 3.16, combines both solid-state and mechanical switches to enable fast current interruption. The primary branch, referred to as the main branch, consists of two mechanical switches, S1 and S2, where S1 is a fast-operating switch designed for rapid response, and S2 functions as the normal switch. A secondary branch is integrated with a capacitor (C1), a thyristor (T1), and an inductor (L) to effectively commutate the fault current away from the primary branch. Additionally, a regenerative circuit is formed by a combination of IGBT, capacitors C1 and C2, inductor L, and diodes D1 and D2, which work together to manage energy recovery. Furthermore, diode D3 provides a path for free-wheeling, ensuring the current leakage is directed safely towards the load. This innovative design enhances the breaker's speed and efficiency in fault current interruption.

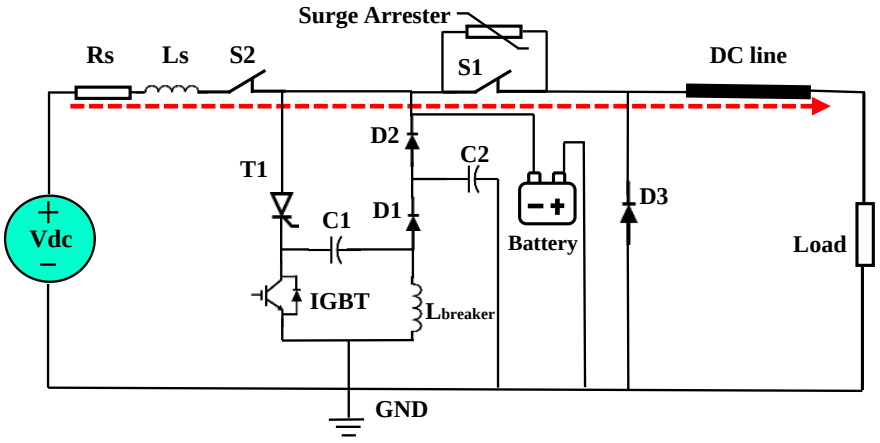


FIGURE 3.17: The current path of the source before tripping.

3.4.2 Working Principal of the Improved HDCCB

3.4.2.1 Normal Operation

Initially, both mechanical switches S2 and S1 are closed as in normal operation, and the current flow through them is calculated using (3.1) as,

$$i_s(t) = i_{LOAD}(t) = I_o. \tag{3.1}$$

In this case system is behaving normally as shown in Fig. 3.17.

3.4.2.2 Fault Occurrence

When the system crosses a certain threshold and is detected as faulty the thyristor T1 will be turned ON and start storing the charge in the capacitor. When switch S1 turns off, it energizes LS due to current breaking, and a secondary path is provided to the fault current. Meanwhile, a turn-on signal is sent to the thyristor T1, to get ON and a path is provided to the capacitor to get charged as shown in Fig. 3.18. Whereas, inductor charging is done in the next step when the signal is given to IGBT, and IGBT is turned ON after the thyristor has performed its operation. Moreover, the current flow is represented in (3.1). At this time current oscillations are generated, resulting in zero-crossing, and the thyristor is turned off at the first point of zero-crossing. However, as given in (3.2), a series resonance circuit is responsible for controlling current oscillation,

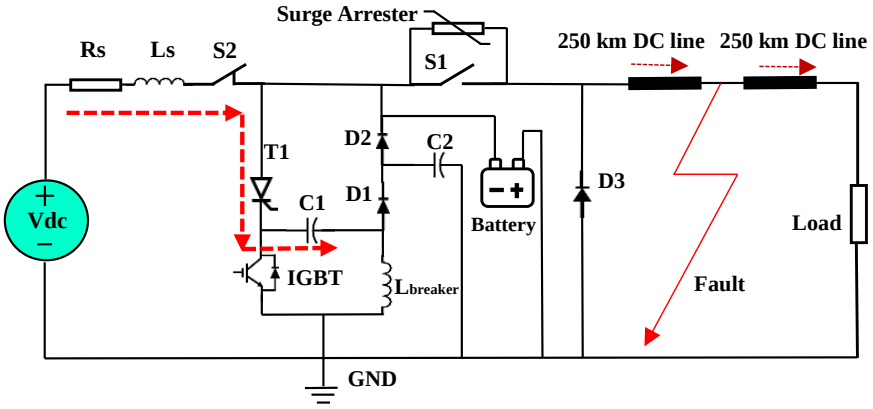


FIGURE 3.18: The current path of the source when a fault occurs.

$$L^{*}\frac{di_{s}\left(t\right)}{dt}+R_{s}i_{s}\left(t\right)+\frac{1}{C1}\int i_{s}\left(t\right)dt=V_{dc},i_{s}\left(t=t_{o}\right)=I_{o}, \tag{3.2}$$

where, V_{dc} is the DC source voltage, L_s is the source inductance, R_s represents the source resistance, $i_s(t)$ is the source current, I_o is the source current before tripping starts, and $L^{*}=L_{s}+L$. By rearranging (3.2) we get:

$$V_{dc}-L^{*}\frac{di_{s}\left(t\right)}{dt}-R_{s}i_{s}\left(t\right)-\frac{1}{C1}\int i_{s}\left(t\right)dt=0. \tag{3.3}$$

The roots of our systems are obtained by solving 3.3 as,

$$D_{1},D_{2}=\frac{-R}{2L}\pm\sqrt{\left(\frac{R}{2L}\right)^{2}-\frac{1}{LC}}. \tag{3.4}$$

From (3.4), we have three cases: the system may be under-damped, critically damped, or over-damped. When the roots of D_1 and D_2 are complex, the solution of the system from (3.4) would be:

$$i\left(t\right)=e^{-\alpha t}\left(x\cos\beta t+y\sin\beta t\right), \tag{3.5}$$

$$\begin{aligned} &i_{s}(t)=e^{-\alpha t}c\cos(\beta t-\phi),\\ &c=\sqrt{x^{2}+y^{2}}\text{ and }\phi=\tan^{-1}\left(\frac{y}{x}\right). \end{aligned} \tag{3.6}$$

(3.5) shows that the system is under-damped. In our case, we use an under-damped system, because, at the first zero-crossing point of this oscillating current, the thyristor T1 turns off by natural commutation, accomplishing the successful current breaking.

Here, $\alpha = \frac{R_s}{2L^*}$ is the damping frequency, $\omega_r = \sqrt{\frac{1}{L^*C1}}$ is the resonance frequency, and $\beta = \sqrt{\omega_r^2 - \alpha^2}$ is the ringing frequency, provided by the condition that the ringing frequency should be greater than the damping factor.

Moreover, the capacitor and inductance in the oscillation loop have a significant impact on the ringing frequency. The apparent current breaking time T_{trip} can be found by solving (3.6) as,

$$i_s(t = T'_{trip}) = 0. \tag{3.7}$$

The switching delay T_{off} is added as,

$$\begin{aligned} T_{trip} &= T'_{trip} + T_{off}, \\ T_{trip} &= \frac{1}{\beta}\left(\frac{\pi}{2} + \phi\right) + T_{off}. \end{aligned} \tag{3.8}$$

After putting the values of the T'_{trip}, (3.8) reveals that the higher the value of β, the faster would be the current breaking. On the other hand, when the source current flows through the capacitor C1, it will be charged. Now the capacitor voltage can be derived from (3.6). Thus, the capacitor will be charged up to the voltage $V_{c1}(t)$ is computed as,

$$V_{c1}(t) = \frac{1}{c_1}\int (e^{-\alpha t} c\cos(\beta t - \phi))dt, \tag{3.9}$$

$$V_{co} = V_{c1}(t = T'_{trip}). \tag{3.10}$$

Comparing (3.9) with (3.10) results in,

$$V_{co} = \frac{1}{c_1}\int (e^{-\alpha T'_{trip}} c\cos(\beta(T'_{trip} - \phi))dT'_{trip}. \tag{3.11}$$

Now, the energy in the capacitor will be stored as the combination of load energy subtracted by the source energy as a result of the energy transfer process.

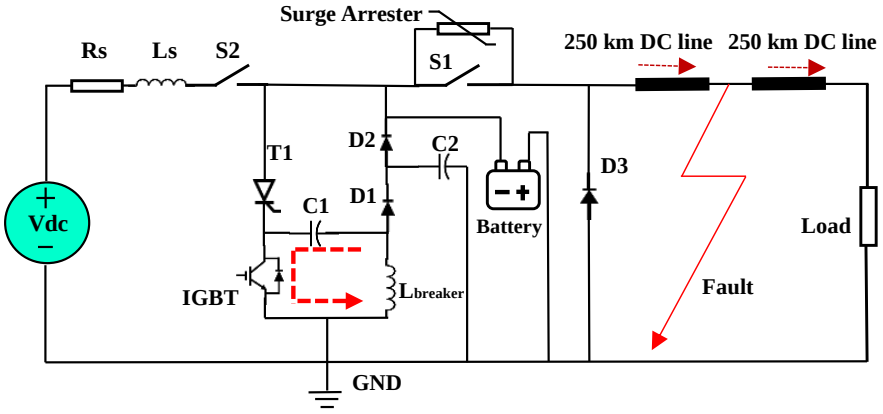


FIGURE 3.19: The energy is transferred from the capacitor to the inductor.

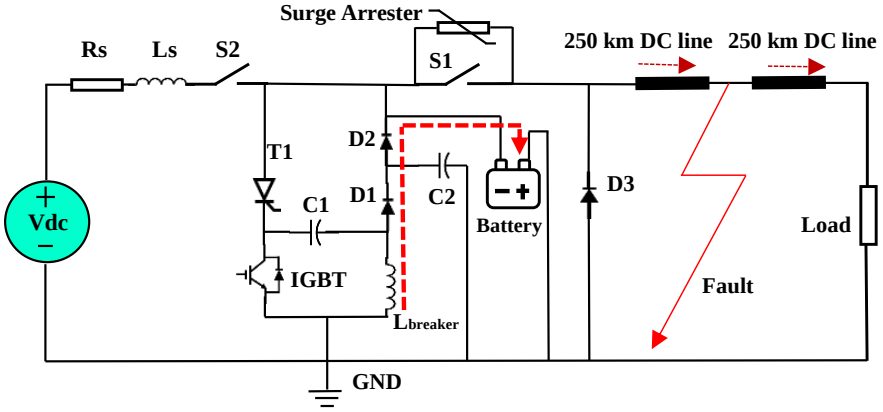


FIGURE 3.20: The breaker's inductor current starts charging the battery.

$$E_{c1} \approx E_s - E_{Load}. \tag{3.12}$$

Inductor charging: The charging process of the inductor by the capacitor is given in Fig. 3.19.

3.4.2.3 Regeneration of Current

The regeneration sequence will commence as soon as the source current approaches zero. C1 will discharge through L, and the IGBT will turn on a fixed duty cycle of 20% and a switching frequency of 20kHz as depicted in Fig. 3.20. Slow discharge is required because the source does not accept the fast change. (3.13) gives the capacitor discharging through the inductor as, and the process stabilizes gradually during operation.

$$L\frac{di_r(t)}{dt} + \frac{1}{c_1}\int i_s(t)dt = 0. \tag{3.13}$$

Given the resonant frequency $\omega_r' = \frac{1}{\sqrt{Lc_1}}$, (3.13) is further solved for regenerated current as,

$$i_r(t) = V_{co}\sqrt{\frac{C_1}{L}}\sin\omega_r' t \tag{3.14}$$

The regenerated current is smoothed out by C_2 as,

$$C_2 = \frac{I_R(avg)d}{\Delta V c_2 f}, \tag{3.15}$$

and the energy stored in the inductor is given as,

$$L = \frac{V_{c1}d}{\Delta I_r f}. \tag{3.16}$$

The transferred energy from the inductor to the battery bank is governed by,

$$V_{dc} = (L_s + L)\frac{di_s(t)}{dt} + R_s i_s(t). \tag{3.17}$$

The average regenerated current is,

$$I_R(average) = \frac{1}{T_R}\int_0^{T_R} i_R(t)dt. \tag{3.18}$$

3.4.3 System Design of the Improved HDCCB

Fig. 3.21 represents the simulation set-up of the designed regenerated hybrid DC breaker which is connected to the HVDC grid and the transmission line. Parameters of the

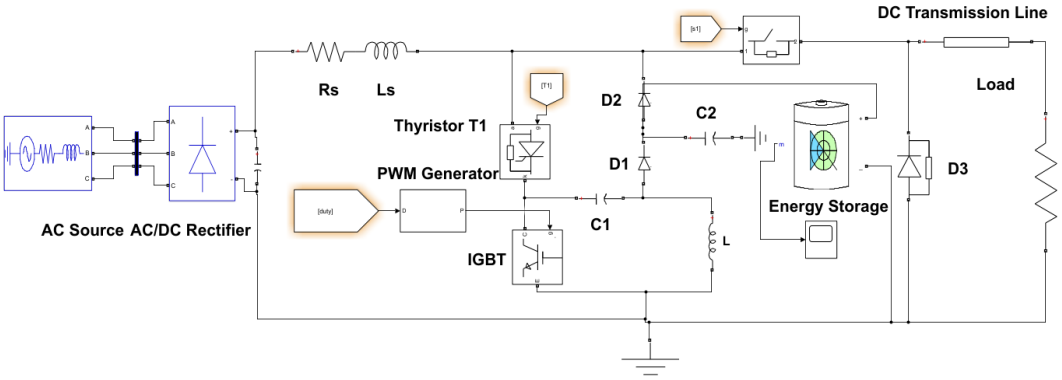


FIGURE 3.21: The simulation set-up of the proposed improved hybrid DC breaker with the energy storage element.

network, battery, load, Transmission Line.

3.4.4 Results and Discussion of the Improved HDCCB

This section gives a brief review of the designed system's simulation results in MATLAB's Simulink®/Simpowersystems environment. The system's outputs are distributed over the input block, CB, C1, battery banks, and load. In addition, hybrid CB performance, for instance, time of current breaking, voltage across breaker, and battery banks charging are also investigated and evaluated based on the results.

3.4.4.1 Current Breaking

CB receives a trip signal at time t=0.02s and remains ON until the thyristor turns ON. After that, main contacts will open, and the thyristor will provide a secondary path for the fault current and the circuit breaker current reduces to zero as depicted in Fig. 3.22(a). This current breaking energy will be stored in C1 for 0.02s to 0.04s as shown in Fig. 3.22(d). During this period, the current is broken and the source current is diverted to the secondary branch. Meanwhile, the series resonance circuit is established and necessary oscillations are generated. As a result, when the source current is diverted, the load is disconnected. The load was initially receiving a voltage of 400kV as illustrated in Fig. 3.22(e) and a current of 2kA in normal operation as shown in Fig. 3.22(f) however, after the trip signal is received, the load disconnects

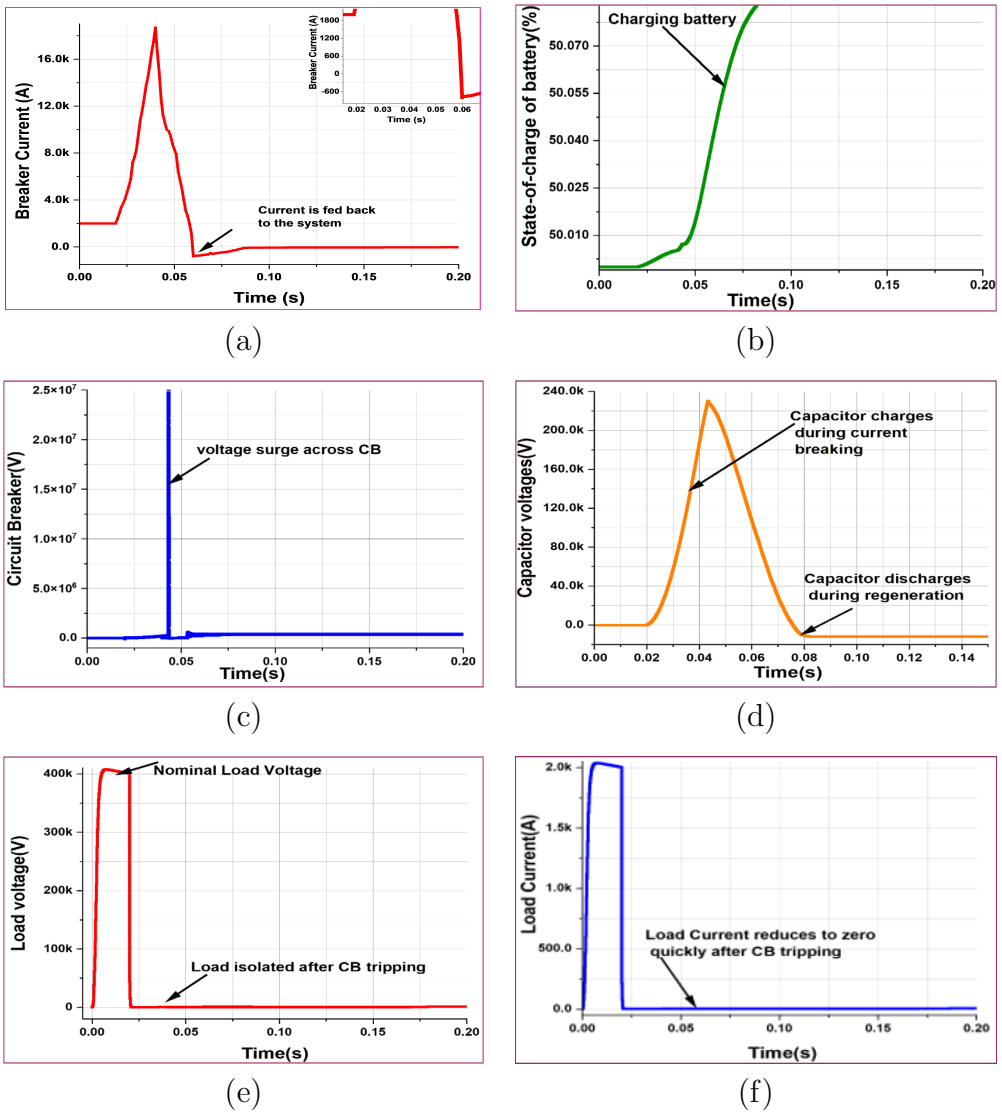


FIGURE 3.22: The simulation results of the proposed improved hybrid high-voltage direct current circuit breaker. (a) Current across the breaker, (b) the battery is charging, (c) voltage across the switch S11, (d) voltage across the switch S1, (e) voltage at the receiving end of the load, and (f) current at the receiving end of the load.

and the voltage becomes zero which isolated the load, as shown in Fig. 3.22(e). When current oscillations begin and cross the first zero-crossing point, the current is broken and the thyristor turns off automatically.

When current travels through the capacitor C1, it charges. Fig. 3.22(c) depicts the voltage stress across the breaker, as the source is inductive so a large voltage surge when the breaker opens. Whereas, Fig. 3.22(d) depicts the voltage appearing on the capacitor, which reveals the capacitor has been charged up to 240kV. Fig. 3.22(a)

depicts the current of the circuit breaker which was wasted in the traditional topologies. Whereas, IGBT works at a fixed duty cycle of 20% duty cycle and 2kHz PWM signal adjusted of IGBT.

3.4.4.2 Current Regeneration

The circuit breaker will be ready for regeneration when the source current approaches zero and the thyristors (T1) turn off. Capacitor C2 smooths the regenerated current. IGBT helps the capacitor to convert its stored energy into the pulsed current at 20% duty cycle and 2kHz PWM signal adjusted of IGBT. The duty cycle of IGBT decides the speed and quality of the regenerated current while the Inductor current shows the discharging current. Control is established to coordinate between CB, thyristor and IGBT. Whenever the IGBT is turned ON, the inductor will force the current towards the battery banks. The smoothed regenerated current is 75kA. PWM cycle decides the regenerated current magnitude and it will continue to forward the regenerated current to the battery banks. The regeneration process continues till the capacitor holds the charge, after when the capacitor discharges, the regeneration process is complete. PWM signals stop once regeneration is complete, and the breaker controls the residual current to zero, allowing battery banks to charge from a higher level of charge. The battery's initial level of charge was 50%, and it has since begun to increase, as depicted in Fig. 3.22(b), indicating that the battery is charging.

3.4.4.3 Regeneration and Supercapacitors

Supercapacitors offer exceptional charge and discharge capabilities, making them ideal for high-voltage DC applications requiring rapid energy delivery. Their high capacitance and low internal resistance enable efficient energy transfer with minimal losses. Unlike conventional batteries, supercapacitors can endure millions of charge-discharge cycles without significant degradation, ensuring long-term reliability and durability. Additionally, they operate efficiently across a wide temperature range, making them suitable for demanding industrial and automotive environments. With their ability to store and

release energy almost instantaneously, supercapacitors provide high power density, supporting applications that require quick bursts of energy. Their electrostatic double-layer capacitance (EDLC) and pseudocapacitance mechanisms allow for superior energy retention and rapid response times. Furthermore, advancements in materials, such as graphene-based electrodes, have enhanced their energy density and performance. Supercapacitors also require minimal maintenance, as they do not rely on toxic or rare materials, making them a sustainable energy storage solution.

Several high-performance supercapacitors are available in the market, designed to meet the demands of industrial, automotive, and renewable energy applications. Maxwell Technologies (now part of Tesla) produces ultracapacitors widely used in power grids and transportation systems. Skeleton Technologies offers graphene-enhanced supercapacitors with superior energy density, making them ideal for high-power applications. Eaton's XLR Series provides reliable energy storage solutions for electric buses and renewable energy systems, while LS Mtron and Nippon Chemi-Con manufacture supercapacitors tailored for industrial power stabilization and automotive applications. These commercially available supercapacitors are revolutionizing energy storage, offering a sustainable, high-efficiency alternative for modern electrical systems.

3.5 Chapter Summary

The chapter discusses the development of a modular hybrid DC circuit breaker (MHDCCB) that enhances energy efficiency and fault clearance in High Voltage Direct Current (HVDC) systems. The MHDCCB captures and stores fault energy after interruption, improving system sustainability and performance. Its innovative topology design allows for energy reuse from the breaker's inductor, reducing waste and improving efficiency. The MHDCCB can self-adaptively switch between current limiting and current clearing stages, offering flexibility in protection strategies. It also stores fault energy during fault occurrences, preventing significant energy dissipation in HVDC systems with large inductors. The MHDCCB reduces breaker size and cost, making it more compact and cost-effective, this work is published in [25].

Another contribution discussed in this chapter is the development of an improved hybrid Direct Current Circuit Breaker (HDCCB) topology to capture and store wasted energy from network inductance. The DCCB was tested in a High Voltage Direct Current (HVDC) grid to validate its performance and successfully stored the wasted energy in battery banks for future use. HDCCB conserves, regenerates, and transfers energy during each current break. This topology is particularly beneficial for large inductive networks. A control algorithm was developed to adjust the duty cycle, ensuring efficient current breaking with minimal energy loss. The hybrid DCCB was rigorously tested within an HVDC grid, showcasing its effectiveness this work is published in [26].

Chapter 4

A Regenerative Hybrid HVDC Circuit Breaker Topology

This chapter introduces an efficient regenerative hybrid high voltage direct current circuit breaker (HDCCB) topology for HVDC system protection. The topology consists of four stages: normal operation, current commutation, primary current limiting, and current regeneration. The insulated gate bipolar transistors (IGBTs) and thyristors used in the breaker are efficient, with nanosecond and microseconds turn-on times. The proposed topology has a reduced number of components and a simplified control scheme, achieving quick current interruption time and reducing energy dissipation pressure on surge arresters. The circuit breaker is modelled and simulated in MATLAB Simulink®/Simpowersystems, providing a fault current interruption time of less than 2ms and a reset time of less than 5ms, outperforming some of the state-of-the-art circuit breakers.

4.1 Introduction

High-voltage direct current systems are beneficial for long-distance bulk power transmission. Still, their formation remains a challenge due to the lack of efficient breakers as discussed in studies [97–99]. HVDC grids have low active and reactive power conduction

losses, but short circuit faults pose a challenge due to faster penetration mentioned in [100, 101]. Fast and reliable breakers are needed to isolate faults and prevent grid collapse as per research in [102–104].

Direct current is more challenging to break than alternating current due to its lack of a natural zero crossing point. Therefore, HVDC circuit breakers are crucial as discussed in [105]. The rapid rise of fault current in HVDC makes it difficult to isolate faults and develop protection systems. China tested the first bipolar hybrid high-voltage direct current circuit breaker (HDCCB) for a 500kV multi-terminal direct current (MTDC) transmission system on the Zhangbei-Beijing overhead line as mentioned in [106]. A DC fault in MTDC transmission can damage semiconductor equipment and potentially propagate converter failure throughout the HVDC network as frequently discussed in studies [107–109].

The MTDC system requires an efficient HDCCB with a simplified control scheme, fewer breaker components, reduced energy dissipation pressure on surge arresters, and current limiting capability to minimize cascaded failure as per studies [110–112]. HDCCBs isolate DC-faulted lines from the grid, preventing fault propagation. Fast mechanical switches are used for normal operational current, while solid-state power electronics interrupt short circuit current. These HDCCBs combine ultra-fast disconnectors and solid-state switches for minimal on-state losses and speedy breaking capabilities.

Installing DC reactors at transmission line ends can limit fault currents but prolong the fault-clearing time in the HVDC grid as mentioned in[113, 114]. Large DC reactors can slow down DC circuit breaker isolation speed, leading to system instability. A study proposed a solution for quick tripping through fault current limiters (FCLs), which provide significant inductance during failure and low inductance for normal operation, as indicated in [115, 116]. However, their research lacks larger fault energy dissipation pressure and longer current interruption time.

Conventional HDCCB topologies use absorber components like snubber networks or nonlinear resistors to absorb and dissipate surplus energy as heat, aiding in fault current reduction like [117, 118]. This current-breaking mechanism is similar to dynamic breaking in electrical drives, which converts kinetic energy into electrical energy and

releases it as heat in a resistor [119]. However, in modern HDCCB topologies, this energy waste is unnecessary as it increases the size and expense of the circuit breaker and prolongs its current interruption duration. Regenerative braking is used to recycle and return this energy to the source.

In the recent studies on the HDCCB, the longer fault current interruption time has been reduced to less than <5.2ms in [120] and <3ms in[121, 122], <4ms in [123], <10ms in [124, 125]. However, this reduction in interruption time is insufficient due to large fault currents in high-voltage systems, which can cause immediate damage to the transmission system and converter stations. Moreover, the HDCCB's fault-clearing process requires large energy dissipation, making it challenging for the breaker to reset to normal operation after interrupting the fault current. Some researchers have reduced this time to 8ms in [120], 30ms in [122], 40ms in [121], 60ms in [124] and 14ms in [125]. However, there is still room for improving the current interruption time and breaker reset time of the HDCCB to make it compatible with the MTDC system.

The concept of regeneration has rarely been addressed in the literature. Usually, large energy-dissipating devices are deployed in the breaker to clear fault energy. This method has not only increased the cost and size of the breaker but also compromised the current interruption time of the breaker. In [122], the primary current interruption time of the breaker is reduced to 3ms but the breaker reset time is 40ms as a large amount of time is consumed for energy clearing. Whereas, in [123, 125] concept of energy regeneration was introduced in which some energy was reused. However, this circuit breaker topology was tested for low-voltage direct current systems. Moreover, the concept of the current limiting branch was ignored, which is essential for limiting the sudden rise of fault current. Summarizing the above arguments, longer fault current interruption time, breaker reset time and larger energy-dissipating devices are impeding the implementation of HDCCBs in HVDC systems. This work proposes an efficient regenerative HDCCB topology with minimized fault current interruption and reset time. The primary current interruption time is reduced to less than 2ms and the breaker reset time is reduced to less than 5ms along with the reuse of some of the fault energy after interruption of fault. Moreover,

a simplified control scheme due to a lesser number of components, and, fault current

limiting capability are the additional features of the proposed topology. These characteristics make our regenerative HDCCB topology unique as compared to the earlier studies [120–125].

4.1.1 Major Contributions of the Regenerative HDCCB

The major contributions of the proposed regenerative HDCCB are following:

- A novel and efficient regenerative hybrid high-voltage direct current circuit breaker topology is proposed to protect HVDC systems from faults within milliseconds. The current interruption of the proposed HDCCB is significantly reduced to less than 2ms and the breaker reset to normal operation achieved within 5ms. The circuit breaker features a current limiting branch to limit fault current from reaching its peak value, preventing system damage within milliseconds.
- A compact topology is developed with fewer components as compared to the studies [122, 125]. Less number of switches leads to a simplified control scheme, making the proposed circuit breaker compatible with the HVDC system applications.
- The proposed HDCCB has a fault current regeneration feature. Conventionally, after the interruption of the fault current, the remaining fault current is freewheeled through diodes or thyristors to bring the system back to normal operation. However, after the main fault current is interrupted, the proposed HDCCB reuses that fault energy and sends it back to the source, saving 1.5MJ of fault energy compared to the existing work's 17.07kJ [125].

4.2 The Proposed Regenerative Hybrid High-voltage Direct Current Circuit Breaker

This section provides a detailed description of the proposed regenerative HDCCB topology. Firstly, the schematic of the circuit breaker is presented and explained. Later on,

different operation stages of the breaker are described, including the normal operation, current commutation, primary current limiting, and current regeneration stage.

4.2.1 Topology

The schematic of the proposed high-voltage direct current circuit breaker is given in Fig. 4.1. It consists of four branches: the main branch, the regeneration branch, the current-limiting branch, and the main breaker branch.

- The **main branch** has ultra-fast disconnectors (UFD1 and UFD2) which are fast mechanical switches capable of withstanding high voltages, interrupting large currents, and having minimal conduction losses. Moreover, they have an interruption time of less than 2ms [126]. The switch S isolates the source from the transmission line during a fault. A load commutation switch (LCS2) offers high resistance during the fault and forces the current to flow in the other branches. The source equivalents are represented in Fig. 4.1, as capacitor C_{eq}, voltage source U_{eq}, resistor R_{eq}, and inductor L_{eq} along with the transmission line equivalents R_{dc} and L_{dc}.

- The **regeneration branch** of the proposed circuit breaker consists of regeneration switches (RGS1 and RGS2) to control the regeneration mechanism of the breaker, a diode D to maintain the flow of current in a single direction, and a ground switch (GS1) to support regeneration.

- The **The current limiting branch**, consisting of a load commutation switch (LCS1), an inductor L, and resistor R, is designed to prevent sudden changes in current and limit fault current from peak values, thereby saving HVDC from large DC fault current.

- The **main breaker branch** features sub-modules (SM) with IGBTs and surge arresters as arch extinguishing chambers to snub voltage and current changes due to faults, protecting expensive components like UFD1, UFD2, LCS1, and LCS2 by dumping maximum fault energy in surge arresters.

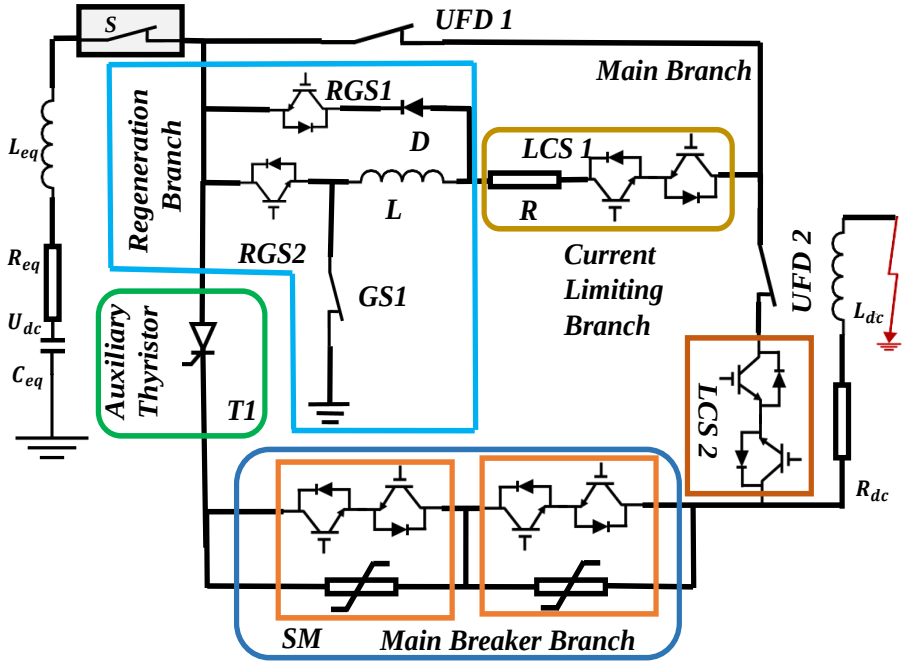


FIGURE 4.1: The proposed regenerative hybrid high-voltage direct current circuit breaker schematic.

The details of the above-mentioned four branches are given in the following Section 4.2.2 of the proposed topology.

4.2.2 Operation Stages

This section provides a comprehensive explanation of the four operation stages, starting from the normal operation stage of the regenerative HDCCB topology.

4.2.2.1 Normal Operation Stage (Before t_0)

The normal operation of HDCCB is represented as a red dotted line in Fig. 4.2. Here, both ultra-fast disconnectors (UFD1 and UFD2) and load commutation switch LCS1 continue to maintain their ON position, and the rest of the switches will be OFF to ensure fewer on-state operation losses. This stage continues to operate until a fault occurs. The equivalent circuit of this stage is represented in Fig. 4.3. During normal operation, when a load is sinking power from the source the voltage drop against UFDs, LCSs have been calculated from (4.1) as,

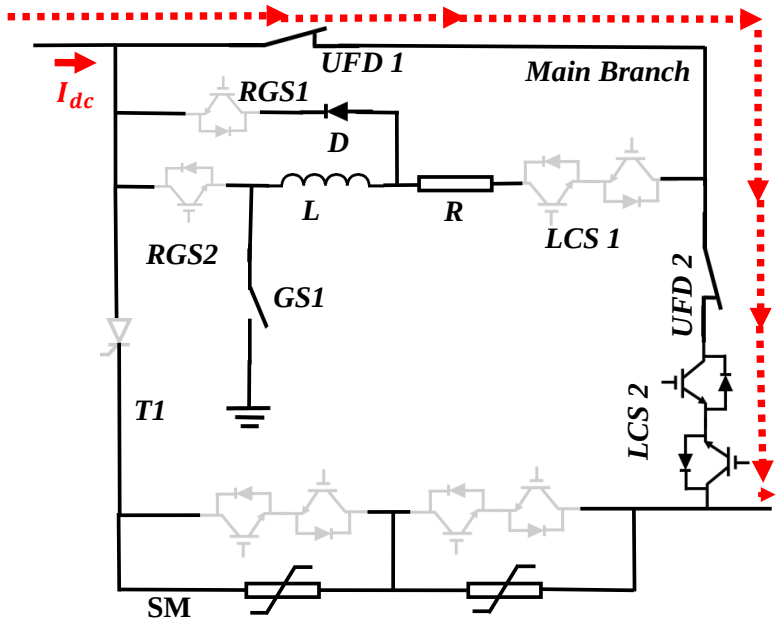


FIGURE 4.2: Before t_0: Normal operation stage of the proposed hybrid direct current circuit breaker.

$$\begin{aligned} &V_{\text{source}} - V_{\text{UFD-1}} - V_{\text{UFD-2}} \\ &\quad - V_{\text{LCS-2}} - V_{\text{TL}} - V_{\text{load}} = 0, \end{aligned} \tag{4.1}$$

$$V_{\text{UFD-1}} \approx 0, \quad \text{(mechanical switching)}$$

$$V_{\text{UFD-2}} \approx 0, \quad \text{(mechanical switching)}$$

$$V_{\text{LCS-2}} \approx 0, \quad \text{(electronic switching)}$$

which shows that assuming the ideal switch's voltage drop is approximately zero. Considering the above equation, the voltage sent from the source will be approximately equal to the voltage received by the load as shown in (4.2),

$$V_{\text{source}} \approx V_{\text{load}}. \tag{4.2}$$

The ideal response occurs when a circuit breaker acts as a conductor, with the load current limited by the load resistor R_L, as shown in (4.3), and the system operates efficiently under these conditions.

$$I_{\text{load}} = \frac{v_{\text{load}}}{R_{\text{load}}} \approx \frac{v_{\text{source}}}{R_{\text{load}}}. \tag{4.3}$$

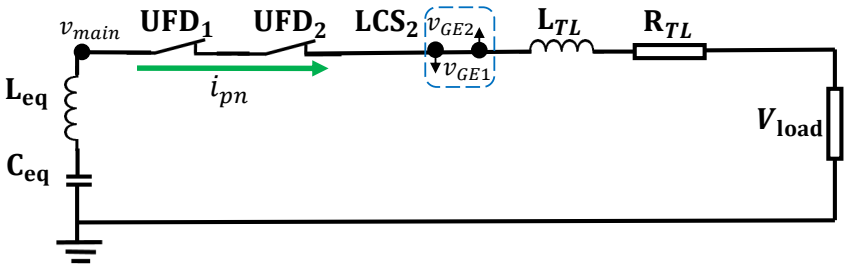


FIGURE 4.3: Equivalent circuit during normal operation of the regenerative hybrid high-voltage direct current circuit breaker(HDCCB).

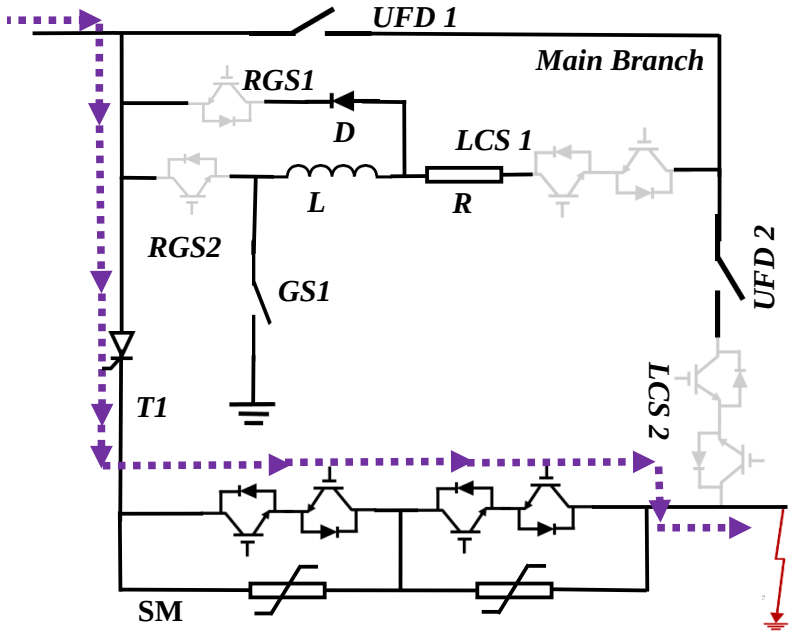


FIGURE 4.4: t_1 to t_2: Current commutation stage of the proposed regenerative hybrid direct current circuit breaker.

From (4.2), it is found that both voltages are equal, resulting in (4.4), where I_{load} is calculated. The lower the voltage drop across switches, the higher the load current,

$$I_{\text{load}} = \frac{v_{\text{UFD-1}} + v_{\text{UFD-2}} + v_{\text{LCS-2}} + v_{\text{TL}} + v_{\text{load}}}{R_{\text{load}}}. \tag{4.4}$$

4.2.2.2 Fault Current Commutation Stage (t_1 to t_2)

The main purpose of this stage is to divert the direction of fault current towards the arc extinguishing chamber's branch to protect expensive UFDs. The proposed topology of regenerative HDCCB initiates fault commutation when the breaker detects an overcurrent exceeding its threshold, ensuring the safety and efficiency of the system.

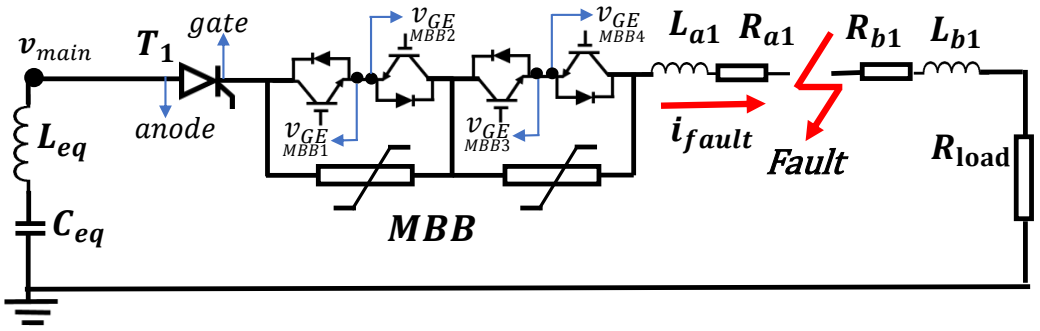


FIGURE 4.5: Current commutation stage's equivalent circuit when fault current diverted towards energy dissipation branch of regenerative HDCCB.

In this stage, the fault current is directed towards the main breaker branch IGBTs.The HDCCB activates all main breaker branch sub-modules. This can be done by triggering thyristor T1, by increasing its gate voltage from its threshold value, like 3V, using the suggested thyristor from the product ID: K0900ME650 datasheet. Then IGBTs of LCS are triggered by increasing its gate voltage from its threshold value, like 7.3V, using the suggested IGBT from the product ID: 5SNA3000K452300 datasheet, depicted in (4.5) as,

$$V_{\text{GS - LCS}} \gg V_{\text{TH - IGBT - LCS}}. \tag{4.5}$$

As the turn-on time of this thyristor and IGBT is in micro and nanoseconds respectively, this will help to protect the expensive UFDs from the 'inductive kickback effect' of the transmission line within milliseconds. The purple dotted line in Fig. 4.4 indicates the current commutation stage of the proposed HDCCB. At this stage, the series current path from LCS2 is truncated by reducing the $V_{Gate-Emitter-LCS2}$ to less than its threshold magnitude as of (4.6),

$$V_{\text{Gate-Emitter(LCS-2)}} < V_{\text{th}}. \tag{4.6}$$

In this way, the LCS2 switch will be open and truncate the main current flow to the transmission line. Thus, UFD1 and UFD2 would be protected. The voltage drop during the current commutation stage has been found from (4.7),

$$\begin{aligned} &V_{\text{main}} - V_{\text{anx.thyristor}} - V_{\text{CC12}} \\ &- V_{\text{CC34}} - V_{\text{TTL}} - V_{\text{Ground}} = 0, \end{aligned} \tag{4.7}$$

where, V_{CC12} is voltage between collectors of IGBT1 and IGBT2, V_{CC34} is voltage be-

-tween collectors of IGBT3 and IGBT4, V_{TTL} is voltage drop over the terminated transmission line, and V_{ground} is ground potential of the sub-modules switches.

The fault current is directed towards the auxiliary thyristor branch, necessitating instant activation of the thyristor and main breaker branch to meet the conditions in (4.8),

$$\begin{aligned} V_{\text{aux.thyristor}} &\approx 0|_{V_{\text{Gate-Anode}}>V_{\text{th}}}, \\ V_{\text{CC12}} &\approx 0\Big|_{\substack{V_{\text{Gate-EmitterMBB1}} \\ V_{\text{Gate-EmitterMBB2}}\end{aligned}\Big\}>V_{\text{th}}}, \\ V_{\text{CC23}} &\approx 0\Big|_{\substack{V_{\text{Gate-EmitterMBB3}} \\ V_{\text{Gate-EmitterMBB4}}\end{aligned}\Big\}>V_{\text{th}}}. \end{aligned} \tag{4.8}$$

Thus, the fault current during the 'current commutation stage' is mainly dependent on the resistance of auxiliary thyristor $R_{aux.thyristor.ON}$ and main breaker branch resistance R_{cc}, as given in (4.9),

$$\begin{aligned} I_{\text{fault}_{t-1}} = & \frac{V_{\text{main}}}{R_{\text{aux.thyristor-ON}} + R_{\text{CC12-ON}}} \\ & \overline{+R_{\text{CC32-ON}} + R_{\text{TTL}}}. \end{aligned} \tag{4.9}$$

Assuming ideal switches, zero resistance will be offered from all the switches is almost negligible so the fault current can reach infinity, as in (4.10),

$$I_{\text{fault}_{(t-1)}} \approx \infty. \tag{4.10}$$

Above, are the main reasons that we need to protect expensive parts of our circuit breaker (UFD1 and UFD2) but the source is still at risk. Thus to protect the source and breaker's expensive components the fault current would be directed in the parallel path so that our breaker can handle the $I_{fault(t-1)}$ efficiently.

4.2.2.3 Primary Current Limiting Stage (t_2 to t_3)

The proposed regenerative HDCCB offers a primary current-limiting stage to gradually decrease fault current magnitude, directing fault current I_{fault} towards the current limiting branch I_L and main breaker branch's surge arresters I_{SA}, ensuring efficient fault

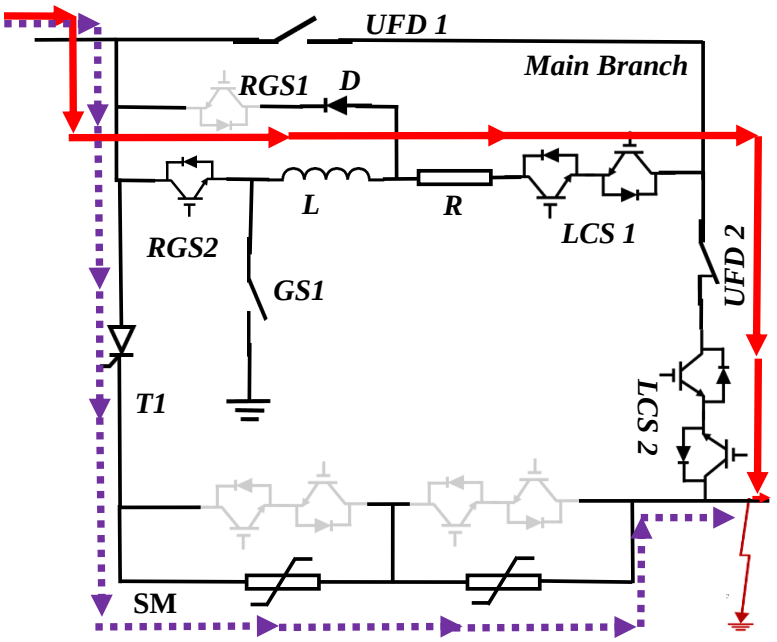


FIGURE 4.6: t_2 to t_3: Primary current limiting stage of the proposed regenerative hybrid direct current circuit breaker.

current management, and protecting costly breaker components. I_{fault} is given as (4.11),

$$I_{\text{fault}} = I_{\text{Limit}} - I_{\text{SA}}, \tag{4.11}$$

where, I_{Limit} and I_{SA} are inductor and surge arrester currents, respectively.

The control method involves triggering LCS1 and LCS2, and dividing the fault current into two parts red solid line as I_L and a purple dotted line as I_{SA} as depicted in Fig. 4.6. Parallel paths help to reduce voltage transients due to fault current with the help of surge arresters of the main breaker branch. The surge arresters show less resistance during a fault, dumping maximum fault energy. Later, the surge arresters show high resistance, shifting fault current to the current-limiting branch. surge arresters serve three main functions: connecting fault circuits, clamping over-voltage to save semiconductor equipment, and absorbing short circuit energy.

The current flowing through the current limiting branch I_L could be calculated as (4.12),

$$I_{\text{Limit}} = \frac{V_{\text{main}} - V_{\text{Breaker}}}{R_{\text{CE . IGBT}_{(\text{RGS2})\text{ON}}} + R_{\text{L}} + R_{\text{Limit}} + R_{\text{LCS1}_{ON}} + R_{\text{LCS2}_{ON}}}. \tag{4.12}$$

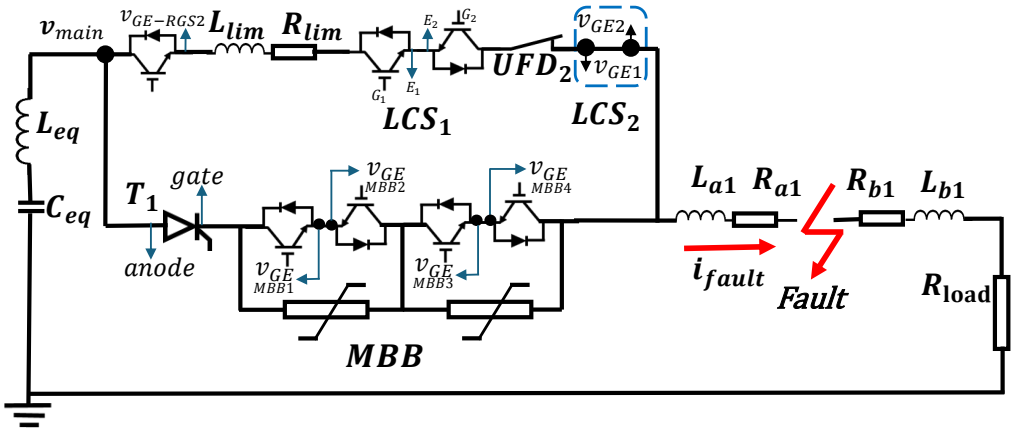


FIGURE 4.7: Equivalent circuit of the regenerative HDCCBs primary current limiting stage, including current limiting and main breaker branch.

The conditions in (4.13),

$$\begin{aligned} R_{\text{CE . IGBT}_{(\text{RGS2})\text{ON}}} &\approx 0|_{V_{\text{GE.RGS2}}>V_{\text{th}}}, \\ R_{\text{LCS1}_{\text{ON}}} &\approx 0|_{V_{\text{GE}}>V_{\text{th}}}, \\ R_{\text{LCS2}_{\text{ON}}} &\approx 0|_{V_{\text{GE}}>V_{\text{th}}}, \end{aligned} \tag{4.13}$$

are satisfied while calculating current during the current limiting stage. However, in (4.12), R is the series resistance. Thus, I_L is limited by the limiting resistor R. For instance, a higher value of R lowers the I_L and vice versa. In the main breaker branch, the surge arrester current should be limited by the value of the on-state resistance of surge arresters as mentioned in Fig. 4.7. The value of surge arrester resistance will determine the I_{SA} as (4.14),

$$I_{\text{SA}} = \frac{V_{\text{main}} - V_{\text{Breaker}}}{R_{\text{AC}_{\text{ON}}} + 2R_{\text{SA}_{\text{ON}}}}, \tag{4.14}$$

where R_{AC-ON} is the anode-cathode resistance of the thyristor, its value is mainly dependent on gate-to-anode voltage biasing, i.e.,

$$\begin{aligned} \text{for } V_{\text{Gate-Anode}} > V_{\text{th}} &\Rightarrow R_{\text{AC}_{\text{ON}}} \approx 0, \\ \text{for } V_{\text{Gate-Anode}} > V_{\text{th}} &\Rightarrow R_{\text{AC}_{\text{OFF}}} \approx \infty. \end{aligned} \tag{4.15}$$

Thus, the application of the principles outlined in (4.11) leads to the derived expression in (4.16), which further refines the system's behavior and performance characteristics.

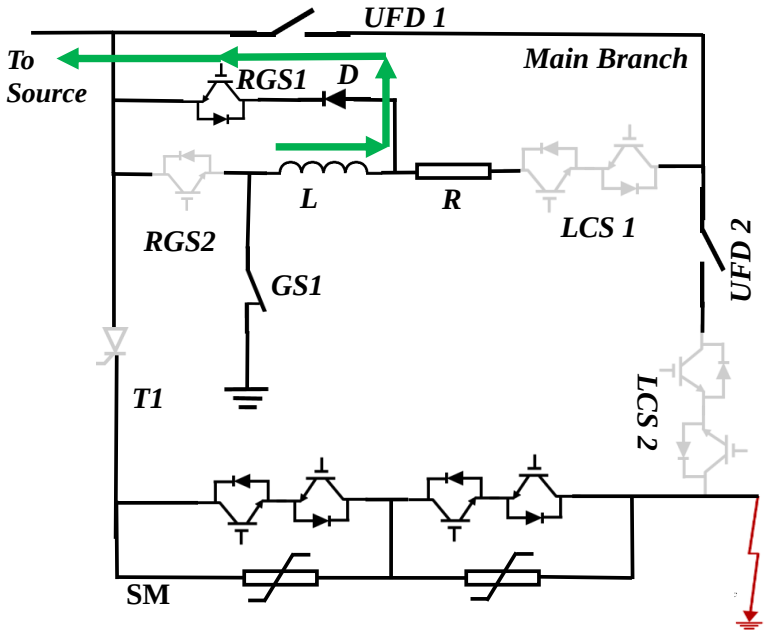


FIGURE 4.8: t_3 to t_4: Current regeneration stage of the proposed regenerative hybrid direct current circuit breaker.

$$I_{\text{fault}_{t2}} = (V_{\text{main}} - V_{\text{Breaker}})\left[\frac{1}{R_{\text{limit}}} + \frac{1}{2R_{\text{SA(ON)}}}\right]$$
$$\therefore R_{\text{limit}} < 2R_{\text{SA}}. \tag{4.16}$$

4.2.2.4 Current Regeneration Stage (t_3 to t_4)

The inductor energy of the breaker reaches its highest value during the primary current limiting stage. This inductor L must disperse its energy as soon as feasible to clear the fault, as energy loss is a key issue with HVDC breakers. In conventional topologies, this fault current is freewheeled and through energy dissipation circuitry, which ultimately increases the size of the breaker [127]. The proposed breaker topology includes the ability to regenerate/reuse the breaker's inductor energy after interruption of the main fault current. In the case of HVDC transmission, a large inductor, such as 300mH, is used. The RGS1 switch will be turned ON to regenerate and clear the energy as quickly as possible. The capacitor of sub-modules facilitates thyristor T1 to self-shutdown. The path of the current regeneration is represented in Fig. 4.8 as a green solid line. In the current regeneration stage, only the 'RGS1' IGBT shown in its equivalent circuit in Fig. 4.9 will be activated because in this stage the energy stored in inductor L will be sent

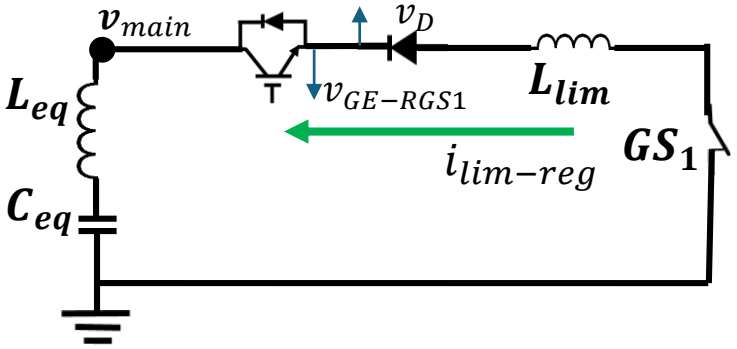


FIGURE 4.9: The equivalent circuit of fault current regeneration state helps reuse some of the fault energy.

back to the source, and the rest of the switches will be OFF during this operation. At this moment, I_L (as written in (4.18) will be routed to the V_{main} terminal until both of the terminals maintain their respective potential this stage will continue to operate. The energy stored in the breaker's inductor is represented by (4.17) as,

$$E = \frac{1}{2}\, L\, (I_L)^2, \tag{4.17}$$

$$I_{\mathrm{L}} = \frac{1}{L} \int (V_{\mathrm{main}} - V_{\mathrm{Ground}}) dt. \tag{4.18}$$

Moreover, in the proposed topology of the HDCCB, the current flow from the inductor at this time will be calculated from the resistance on the way as well as the voltage difference as given in (4.19),

$$\begin{aligned} I_{\mathrm{L}} &= \frac{V_{\mathrm{L}} - V_{\mathrm{main}}}{R_{\mathrm{FB}} + R_{\mathrm{CE_{(ON)}}}}, \\ I_{\mathrm{L}} &\approx (V_{\mathrm{L}} - V_{\mathrm{main}}). \end{aligned} \tag{4.19}$$

The energy sent back from the breaker's inductor can be calculated using (4.20), which takes into account the inductor's current, voltage, and the time duration of the energy transfer during the regenerative process.

$$\begin{aligned} E_{\mathrm{L}} &= \frac{1}{2}\, L \left(\frac{V_{\mathrm{L}} - V_{\mathrm{main}}}{R_{\mathrm{FB}} + R_{\mathrm{CE_{(ON)}}}} \right)^2, \\ E_{\mathrm{L}} &\approx (V_{\mathrm{L}} - V_{\mathrm{main}})^2. \end{aligned} \tag{4.20}$$

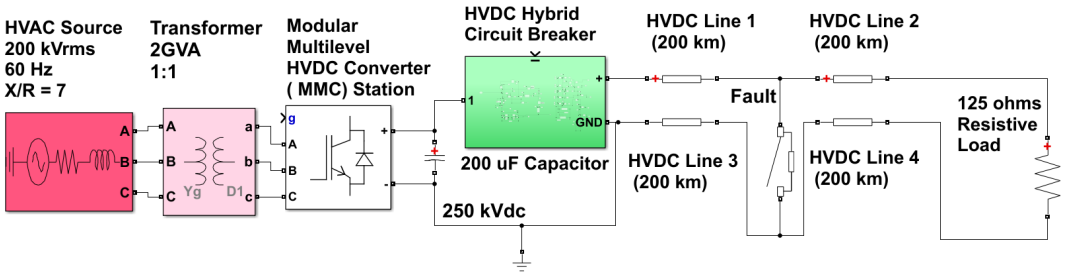


FIGURE 4.10: The simulation test-bed model of the proposed regenerative hybrid high-voltage direct current circuit breaker.

4.3 Simulation Setup

In this section, the simulation test-bed of the proposed regenerative hybrid high-voltage direct current circuit breaker is presented along with the design parameters of the system that are used. In addition, a simplified control algorithm for the controller module of the proposed circuit breaker is also discussed here.

4.3.1 The Test-Bed Model

The MATLAB simulation test-bed model of the proposed regenerative hybrid high-voltage direct current circuit breaker is presented in Fig. 4.10. It includes a high-voltage alternating current (HVAC) source of rating 200kV$_{rms}$, then a transformer to step up the voltage, and after that a multilevel modular converter voltage source converter (MMC-VSC) based mono-polar converter station. The capacitor banks are installed after the VSC to reduce the ripples of the voltage. A hybrid HVDC breaker is installed at the start of the HVDC transmission line and then a resistive load. In this case, a line-to-ground fault is created. The proposed simulation helps to verify the results of the proposed HDCCB. The design parameters of the HVDC network, load, transmission line, and the HVDC breaker are presented in Table 4.1. The design parameters for the VSC HVDC system are chosen to ensure efficiency, reliability, and suitability for the intended application. A mono-polar, 2-level VSC HVDC topology is adopted for its simplicity and cost-effectiveness, with a grid voltage of 250kV is to minimize transmission losses over long distances. The normal current of 2kA and power rating of 500MW align with the load demand, while an AC system voltage of 200kVrms and X/R ratio of 7 ensure

TABLE 4.1: The design parameters of the system.

Device	**Parameter**	**Value**
HVDC network	VSC HVDC type	Mono-polar/2-level
	HVDC grid voltage	250kV
	Normal current	2kA
	Power consumption	500MW
	AC system voltage	200kVrms
	AC system X/R	7
Load	Resistive load	125Ω
	Load current (I_{load})	2kA
Transmission line	Length of each line	200km
	Resistance of line	0.015Ω
	Inductance of line	0.792mH
	Capacitance of line	14.4nF
HVDC breaker	Rated voltage	250kV
	Rated current	2kA
	Current interruption capacity	30kA
	Primary current interruption	2ms
	Breaker reset time	5ms
	Breaker inductance (L)	300mH
	Breaker resistance (R)	15Ω

proper network integration and stability. The resistive load of 125Ω corresponds to a load current of 2kA, matching the system's capacity. Transmission line parameters, including a length of 200km and with its resistance, inductance, and capacitance values. The HVDC breaker, rated for 250kV and 2kA with a current interruption capacity of 30kA, is designed for fast fault clearing, with a 2ms interruption time and 5ms reset time and incorporates specific inductance 300mH and resistance 15Ω for effective fault current management. These parameters collectively ensure the system's robust operation under varying conditions.

4.3.2 Control Algorithm

The control algorithm for the controller module of the proposed regenerative hybrid high-voltage direct current circuit breaker is presented in this subsection. The flow of the proposed circuit breaker is illustrated step-wise in Fig. 4.11. In HVDC circuit breakers, various fault sensing methods are employed, including overcurrent sensing, rate of change of current, voltage sensing, and power differential protection. In our

proposed hybrid HVDC circuit breaker topology, we have opted for overcurrent sensing. In this method, a controller continuously monitors the current, and if it exceeds a predefined threshold, it identifies a fault and activates the breaker. The topology then sends an initial signal to the commutation and later to the trip signal. While various fault sensing methods are available, the overcurrent detection method is preferred in this scenario. In practical applications, a Hall effect sensor is often used to detect faults in high voltage DC circuit breakers. Initially, the fault is continuously sensed as soon as a fault is detected, and the current is diverted towards the current commutation stage, through thyristor T1. The fault current will pass through the IGBTs of the main breaker branch at this time. As these IGBTs have turn-ON time in nanoseconds they will trigger instantaneously. However, switches of the main branch UFD1, LCS1, LCS2, and RGS2 will be opened at this time. This control scheme will help to prevent arc formation across the UFD1 which can damage the whole HVDC transmission within milliseconds. The current is interrupted and the primary current limiting stage begins to limit the rise of fault current. After that regeneration stage begins the fault is cleared and the breaker returns to the normal operation stage.

4.4 Model Validation

The multiple stages of protection make it feasible to deal with HVDC fault currents. The logic sequence of protection can present a better picture of the timing diagram of the working regenerative HDCCB.

4.4.1 Logic Sequence for Protection

Primary protection is sensitive to interrupting fault current quickly [122, 126]. However, clearing faults requires energy dissipation, causing delays in completely clearing the fault and bringing the system back to a normal operation state. Our proposed topology reuses energy after interrupting the main fault current and sends it back to the grid. The primary protection stage of a breaker starts within 2ms, allowing the commutation stage to continue. Fig. 5.13 represents, that after a delay of pico-seconds, the ionization

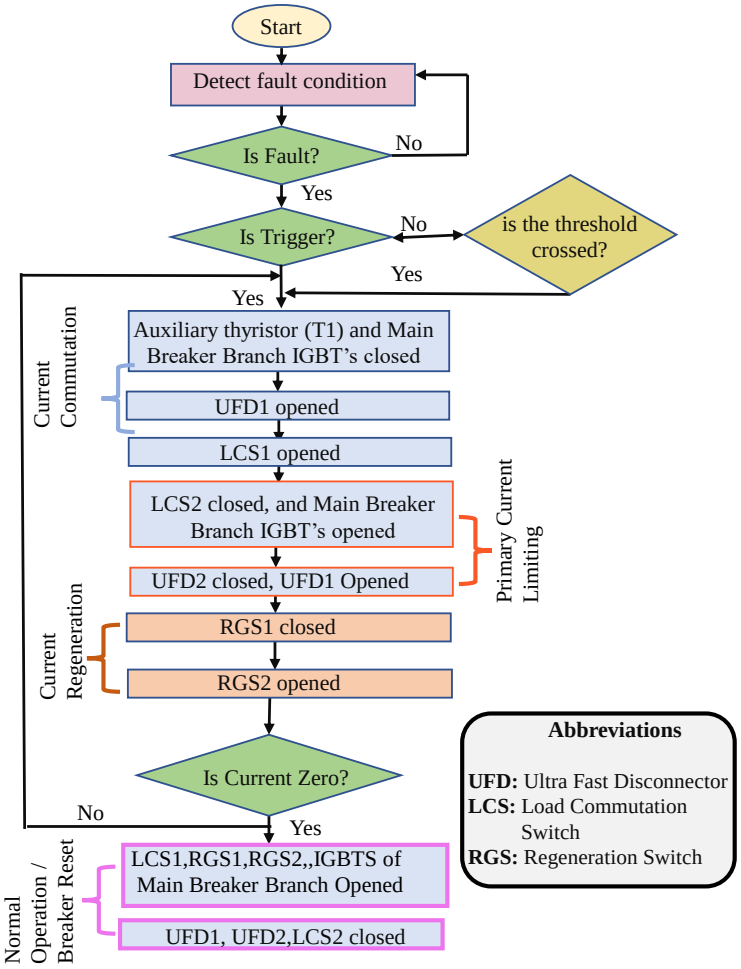


FIGURE 4.11: The control algorithm for the controller module of the proposed regenerative hybrid direct current circuit breaker.

stage begins, lasting 1ms, and the breaker switches to the primary current limiting stage to limit fault current rise. The fault current path is diverted towards surge arresters, causing fault energy to dissipate. In less than 1ms, the fault's maximum energy is cleared, and regeneration begins. Switch UFD2 is opened to regenerate energy left for fault isolation. This process takes less than 2ms, and the fault is completely cleared within 5ms.

4.4.2 Components and Design Analysis

The main breaker branch's sub-modules are exposed to various electrical stresses during different stages of regenerative HDCCB, necessitating series and parallel connections to prevent damage. The maximum current and voltage stress directly impacts the breaker's

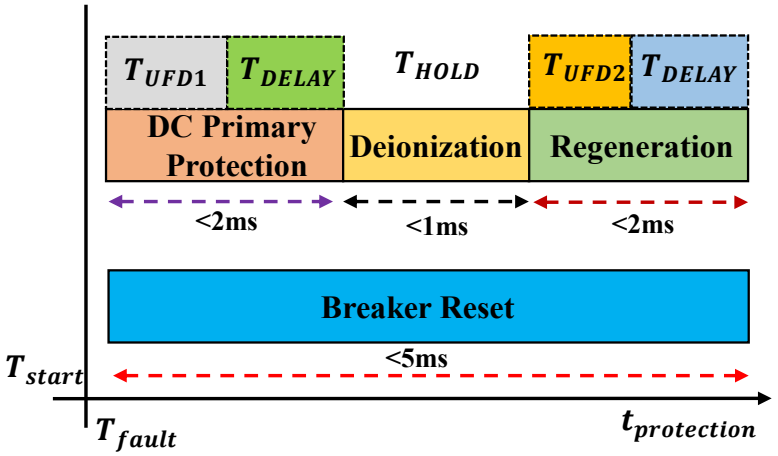


FIGURE 4.12: Logic sequence representation of protection.

proposed topology. Table 4.2 displays the required power electronic components for a 250kV DC system, along with their modules and costs. The solution uses IGBTs, thyristors, and diodes with minimal operational time, achieving a breaker current interruption time of less than 2ms.

The analysis in Section 4.2 reveals that the maximum current stress in the main breaker branch at the primary current limit state t_2 and maximum voltage stress at metal oxide varistors or surge arresters can be calculated from (4.21),

$$\begin{cases} N_{SM-IGBT} \geqslant k_v i\left(t_2\right) / \left(I_{IGBT\_N}\right) \\ M_{SM-IGBT} \geqslant 2k_v \frac{U_{mov}}{n_{SM}} / \left(U_{IGBT\_N}\right) \end{cases}. \tag{4.21}$$

The current limiting method in the circuit breaker opposes the sudden change of fault current. The number of sub-module groups (nSM) is determined by the number of parallel branches ($N_{SM-IGBT}$) and the number of IGBTs ($M_{SM-IGBT}$) in each branch of each SM. The larger the n, the fewer IGBTs in each group and the more steady the current as illustrated in (4.21).

Following the main breaker branch, the auxiliary thyristor is designed with the current-limiting branch's total voltage stress and maximum current stress on the thyristor at time t_2, as given in (4.22),

$$u_{T_1 \max} = U_{dc} - \mathrm{Leq}\frac{di_{dc}}{dt}. \tag{4.22}$$

TABLE 4.2: The required power electronic parts and their specifications of a 250kV DC system for the single regenerative HDCCB.

Component	**Value**	**Operation time**	**Module (prod ID)**	**Cost**
Single IGBT	4.5kV	$t_d(on)$ = 705ns	5SNA3000K452300 [109]	4,961 USD
Single Thyristor	6.5kV	$t(gt)$= 2.5μs	K0900ME650 [109]	400.5 USD
Single Diode	2kV	Fast	SD1100C20C [109]	72.3 USD
Main Breaker Branch	n=2, kv=1 $N_{SM-IGBT}$=1, $M_{SM-IGBT}$=25, N_{T1}=3, M_{T1}=40	–	10D511K [109]	0.07 USD

Table 4.2 shows the number of parallel branches and series thyristors required to make the proposed topology of the regenerative HDCCB, denoted by N_T and M_T, respectively,

$$\begin{cases} N_T \geqslant 2k_v i_{T\max} / \left(I_{T\_N}\right) \\ M_T \geqslant k_v u_{T\max} / \left(U_{T\_N}\right) \end{cases}. \tag{4.23}$$

The rated current and voltage of a single thyristor are denoted by I_{T_N} and U_{T_N}, respectively, as written in (4.23).

4.5 Results and Discussion

This section discusses the results of the proposed topology of the regenerative HDCCB, including its currents, voltages, and energy.

4.5.1 Electrical Current Analysis

In the case of the HVDC circuit breaker, the amount of current flowing from each branch and component holds a significant value. In the main branch of the breaker, UFD1 is connected, which is made up of a Thomson-coil actuator with a very fast action speed and a typical opening time of less than 2ms [126]. This mechanical switch can handle and interrupt the maximum current. In our case, before time t_0, normal operation is

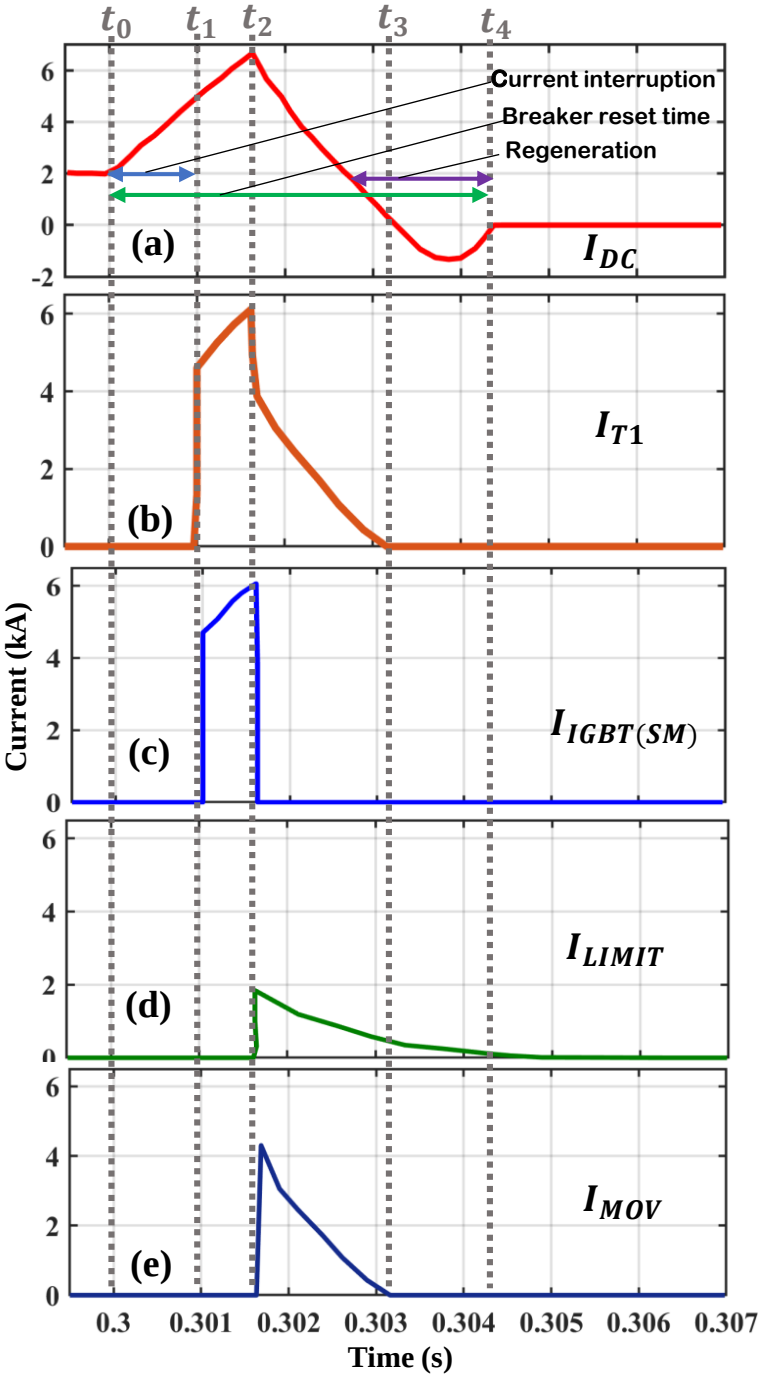


FIGURE 4.13: Current waveforms of the proposed circuit breaker for its different operation stages during t_0 to t_4.

running in the system with a system current of 2kA. At 0.3s, the 'line-ground' fault occurs, and the fault current starts increasing. The proposed topology of RHDCCB interrupts I_{fault} at 6.3kV within 2ms as shown in Fig. 4.13(a) represented as I_{dc}. In contrast to the proposed breaker, reference [122] breaker takes 3ms to interrupt when its fault current reaches 12kA. The interruption process is facilitated by the current

commutation stage when the system. This stage is activated when the current crosses a certain threshold level and the breaker detects it as a fault current. It will trigger the thyristor, T_1 and fault current will be routed with the help of this thyristor as shown in Fig. 4.13(b) represented as I_{T1} during time t_1 to t_2. As this is a very fast-acting thyristor having a turn-on time in microseconds, all the current will be routed towards the main branch. However, the next stage is the current limiting stage; during this time, the IGBTs of the main branch will be open, high voltage will develop across it, and fault current will be moved toward the MOVs of the main branch. The current at this stage can be observed during t_2 to t_3.

During the current commutation stage, the thyristor is triggered, and the fault current is routed toward the IGBTs of the main branch. During this stage, the path of the fault current is diverted, but it keeps on increasing through time t_1 until the trip signal is received at time t_2, which is named as the primary protection in studies[120, 121]. The current flowing through the IGBTs could be observed in Fig. 4.13(c) represented as $I_{l_{IGBT(SM)}}$ which is almost the same current flowing through the thyristor during time t_1 to t_2. This is because the IGBTs have a turn-on time in nanoseconds.

The next stage of the breaker is the current-limiting stage, where the fault current is divided into two branches: the primary current-limiting branch and the main breaker branch for efficient fault management. During this stage, two paths are provided for I_{fault}, passing through the inductor L and resistor R of the current-limiting branch and the surge arresters of the main breaker branch, causing the current to start decreasing after this stage. As the maximum current flows through the main branch, closing the switches of the primary limiting branch results in a temporary increase in current att_2, as illustrated in Fig. 4.13(d) represented as I_{lim}. However, during this time, as most of the fault energy will start dissipating, the fault current will start decreasing, and from t_3 to t_4, the process of regeneration will begin, and that stored energy in the breaker inductor will start sending back to the grid. The regeneration process starts at time t_3, and the energy stored in the inductor is regenerated, which is delivered back to the source during the feedback stage from t_3 to t_4. Around 1.8kA current is regenerated when the RGS2 switch is OFF and the GS1 switch is ON during energy regeneration from the breaker's inductor to reuse some of the fault energy. Compared to [123], the proposed

breaker shows a better result in terms of regenerated energy and less interruption time as compared to [122, 123]. The above results differentiate the proposed regenerative HDCCB from the existing literature.

Moving further the current flowing through the MoVs of the main branch could be observed during the current limiting stage time,t_2 to t_3 shown in Fig. 4.13(e) represented as I_{MOV}. This shows that the proposed RHDCCB needs to absorb less energy as compared to existing DCCB topologies discussed in [120, 121]

4.5.2 Voltage Analysis

The proposed circuit breaker's effectiveness is evaluated by measuring voltage stress across its components. In Fig. 4.14(a), the voltage stress is initially zero before the primary current interruption stage (t_2), indicating that the system is operating normally.

However, when a fault occurs and the breaker is triggered, the voltage stress gradually starts to decrease as the current passes through the thyristor T1 and is directed towards the main breaker branch, as illustrated in Fig. 4.14(c). This indicates that the proposed regenerative hybrid high-voltage direct current circuit breaker is capable of interrupting fault current with minimal voltage stress.

Similarly, in Fig. 4.14(b), the voltage stress across the limiting branch is shown as U_{lim}. It can be observed that the voltage stress across the limiting branch starts increasing during the current commutation stage (t_1 to t_2) and is interrupted at the primary current interruption stage (t_2). This is because the limiting branch is responsible for limiting the fault current and has to handle high voltage stress during the fault interruption. However, the voltage stress across the limiting branch is well within the safe limits and does not cause any damage to the components. The voltage stress across the surge arresters branch, i.e., U_{MOV}, is given in Fig. 4.14(d), which is the voltage flowing through surge arresters. The plot shows that the voltage stress absorbed by the surge arresters is higher than that of the existing hybrid circuit breaker topologies [120]. Despite the higher voltage stress, the surge arresters have effectively protected the circuit breaker components from voltage surges.

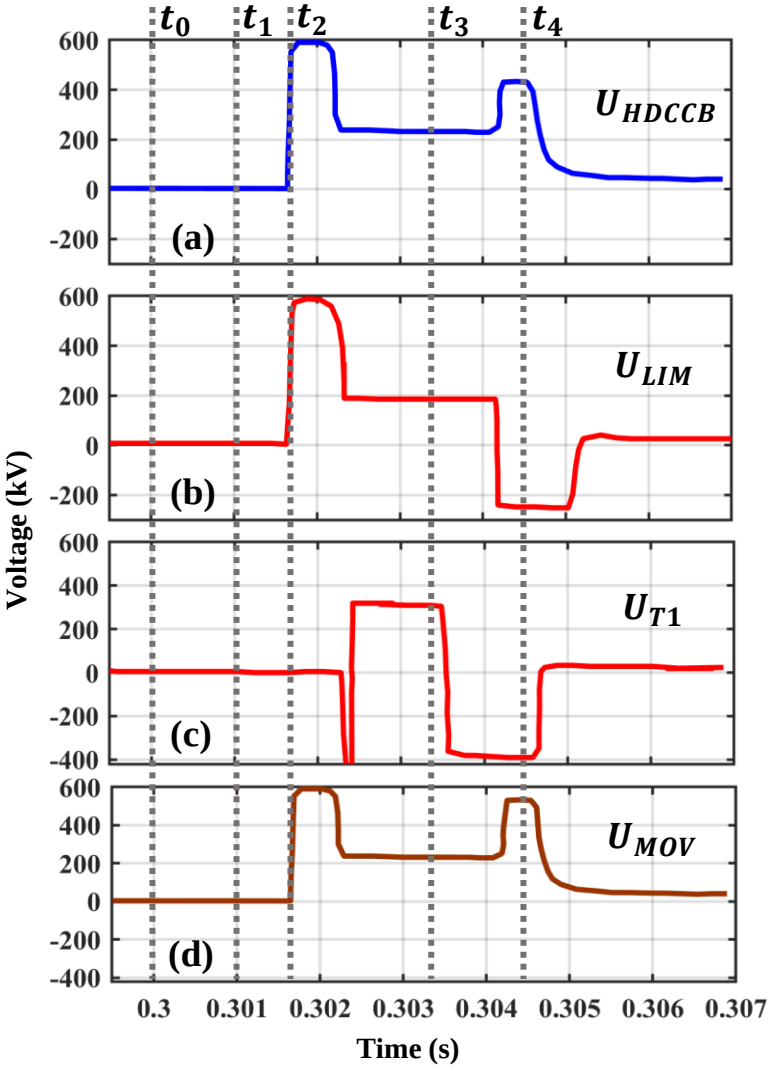


FIGURE 4.14: Voltage waveforms of the proposed circuit breaker for its different operation stages during t_0 to t_4.

Summarizing above, the voltage stress analysis of the proposed regenerative hybrid high-voltage direct current circuit breaker indicates that it is capable of interrupting fault currents with minimal voltage stress and can effectively protect the components from voltage surges.

4.5.3 Energy Analysis

The energy analysis of the proposed regenerative HVDC circuit breaker topology is presented in Fig. 4.15. The proposed HDCCB is designed for 250kV, and 2kA system parameters. Thus, the normal power flowing through the system is 500MW before the

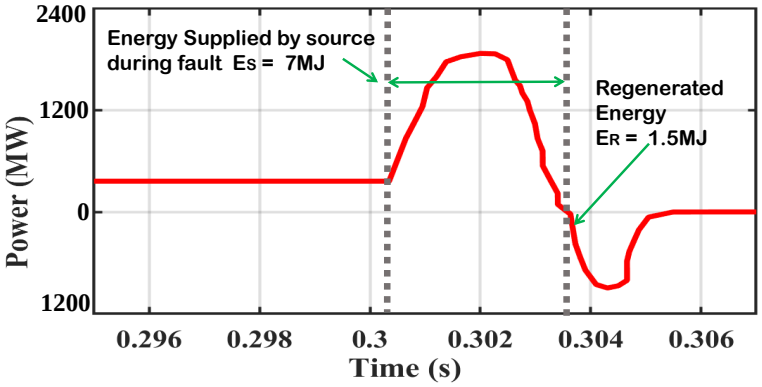


FIGURE 4.15: Power waveform of the system from normal operation to current breaking and regeneration operations.

time 0.3s. However, the 'line-ground' fault occurred at 0.3s, and the fault current and voltage across the breaker increased. As a result, power also starts increasing as it is the product of voltage and current. The power of the system reaches the maximum value of 2000MW. Whereas, energy is the product of time and power. This source of energy at this time is around 7MJ.

Later on, the breaker current reverses its direction when a major fault current is interrupted. At 0.303s the negative direction of the current shows that, the energy of the breaker is feeding back to the grid, through the converter, which will act as an inverter in this case converting direct current back to alternating current. Around 1.5MJ of energy is regenerated and reused for future purposes from the proposed topology of the regenerative hybrid HVDC breaker. This highlights the severity of fault conditions and the need for a fast and efficient breaker topology.

Overall, the energy analysis reveals that the proposed HDCCB breaker topology effectively handles high fault currents while minimizing energy losses, ensuring stability and reliability in power systems, particularly in high power level applications. This highlights its potential for various power system applications.

4.5.4 Performance Comparison

In this section, the proposed regenerative HDCCB is compared with some of the existing high-performance circuit breakers. The comparison is given in Table 4.3. The analysis

TABLE 4.3: Comparison of the proposed regenerative hybrid high-voltage direct current circuit breaker with other circuit breakers. The comparison is performed in terms of interruption time, breaker reset/recovery time, and regeneration capability.

Circuit breakers	**Interruption time**	**Breaker reset/recovery time**	**Regeneration**
Proposed HDCCB	**<2ms**	**<5ms**	**Yes**
Shu *et al.* [120]	<5.2ms	8ms	No
Yu *et al.* [121]	<3ms	40ms	No
Xue *et al.* [122]	<3ms	30ms	No
Lumen *et al.* [123]	<4ms	40ms	Yes
Wang *et al.* [124]	<10ms	60ms	No
Hasan *et al.* [125]	<10ms	14ms	Yes

is made on these points: fault current interruption time, breaker reset/recovery time, regeneration capability, breaker size, and control complexity.

4.5.4.1 Current Interruption Time

Faster fault current interruption is crucial for reducing damage and increasing power system reliability [128, 129]. The proposed HDCCB prevents faults from spreading to other parts, reducing damage and stress on breaker expensive components like thyristors, UFD1, UFD2, LCS1, and LCS2. This lowers maintenance costs and prolongs the breaker's lifespan. Therefore, it's essential to interrupt fault current quickly.

The proposed regenerative HDCCB breaker has a primary current interruption time of <2ms, significantly less than three famous circuit breakers [121, 122, 130], 50% less than [123] and 80% less than [124], indicating it can interrupt fault currents significantly faster than other circuit breakers, as shown in Table 4.3.

4.5.4.2 Breaker Reset Time

A short reset time is essential for power systems to quickly restore normal operations after interruption of the main fault current, reducing breaker reset time and improving the overall system's reliability. Additionally, a short reset time ensures that the system can handle subsequent faults that may occur quickly, reducing the risk of cascading failures and improving the overall system stability. The reset times of the proposed regenerative hybrid high-voltage direct current circuit breaker and other circuit breakers

are given in Table 4.3. The proposed HDCCB can clear the fault and reset it within 5ms. In comparison with other circuit breakers, this reset time is significantly lower, that is, four times less than the best circuit breaker reset time of [130], and eight, six, eight, and twelve-time lower than the circuit breakers in [121–124] respectively. It is twenty-five times less than the latest published research [131]. The proposed regenerative hybrid HDCCB topology offers a fast reset time, allowing the system to return to normal operation quickly, and minimizing potential damages and losses from system shutdowns, making it a promising solution for high-voltage DC power systems.

4.5.4.3 Regeneration Capability

The proposed regenerative HDCCB breaker topology offers a unique energy regeneration function, allowing for the recovery of stored energy in the inductor of the current limiting branch after the interruption of the main fault current during faults. This feature is particularly valuable in larger and more complex HVDC power systems. The researchers in [123, 131] have introduced the regeneration feature but it is for low-voltage direct current applications. However, our suggested regenerative HDCCB topology can deal with high-voltage direct current applications. The regenerated current and energy of the proposed hybrid HDCCB breaker are much higher than those achieved in the low-voltage DC systems investigated in [123, 131]. This is encouraging evidence that an HDCCB breaker can be utilized to increase the efficiency of HVDC systems by recycling energy that would otherwise be wasted. The proposed HDCCB breaker's energy regeneration feature distinguishes it from other existing circuit breakers in Table 4.3. Because of its ability to recycle energy stored in the inductor of the current limiting branch, the proposed HDCCB is ideal for HVDC and offers a promising chance to improve power system efficiency and sustainability.

4.5.4.4 Breaker Size

The proposed regenerative HDCCB breaker reduces the size of the breaker compared to the [105, 122, 130] topologies. Specifically [122], which uses a back-to-back thyristor

branch and large surge arresters to dissipate fault energy. This approach increases the breaker size. The proposed HDCCB breaker uses energy regeneration to recover stored energy in the inductor of the current limiting branch due to fault generation, reducing the need for large surge arresters and the overall size. The proposed topology eliminates the need for the back-to-back thyristor branch, further decreasing the breaker size. This topology offers better performance, faster fault-clearing time, and a more compact design, making it more suitable for high-voltage direct current systems where space and cost are critical factors.

Furthermore, in [131], a complex topology for current regeneration is presented which ultimately not only increased the fault current interruption time, and breaker reset time but also increased the size of the breaker as well. More importantly, this breaker topology is tested for low-voltage direct current applications. However, the proposed regenerative HDCCB topology is for HVDC applications having regeneration features and compact size as well.

Moreover, no freewheeling diodes or thyristors are required to clear fault energy after the interruption of the main fault current due to the fault current regeneration feature of the proposed topology that will result in a compact size of the proposed topology.

4.5.4.5 Control Complexity

The proposed regenerative HDCCB breaker has fewer components compared to [122, 131], which is beneficial as it leads to reduced control complexity of the system. In [122], the back-to-back thyristor-2 branch and large surge arresters were used, increasing the breaker size. More controlled switches are used in that research ultimately increasing the controls for the system. Compared to the above study, fewer components are used in the proposed regenerative HDCCB topology, decreasing the control complexity of the proposed HDCCB. The proposed HDCCB topology simplifies the control system by reducing the number of switches used, unlike the complex system in [130]. A simpler control system reduces complexity, leading to cost savings. It also reduces the risk of failure or malfunction, enhancing reliability and availability. A simpler control system improves reliability and availability.

4.6 Chapter Summary

The chapter introduces a new regenerative hybrid high-voltage direct current circuit breaker (HDCCB) topology designed to reduce fault current interruption and breaker reset times for multi-terminal high-voltage direct current (MTDC) applications. The HDCCB consists of four branches: the main branch for normal operation, the current limiting branch to prevent sudden changes due to fault, an auxiliary thyristor to divert fault current towards surge arresters, the main breaker branch to dump fault energy, and the regeneration branch to reuse fault energy after interruption. The proposed circuit breaker was put under rigorous testing using MATLAB Simulink®/Simpowersystem to ensure its effectiveness. Simplified equivalent circuits were provided for each stage to observe voltages and currents at each stage. The proposed circuit breaker reduced fault current interruption time to <2ms and breaker reset time to <5ms, saving 1.5MJ of fault energy compared to an existing work's 17.07kJ. Based on these results, the proposed HDCCB outperforms some of the state-of-the-art circuit breakers in the literature. The future work will focus on prototype development to fully evaluate the performance and feasibility of the proposed circuit breaker in practical applications.

Chapter 5

A Hybrid Multi-port HVDC Circuit Breaker Topology With Regeneration Capability

As HVDC transmission systems transition to multi-terminal configurations, the need for an efficient, cost-effective, and high-speed fault protection strategy becomes crucial. Chapter 4 introduced the Single-Terminal Hybrid HVDC Circuit Breaker, designed for individual terminal protection while enabling post-interruption energy reuse and regeneration. While effective for single-terminal applications, this approach is not scalable for multi-terminal HVDC (MTDC) networks, where multiple transmission lines require coordinated protection.

Building on this foundation, Chapter 5 presents the Hybrid Multi-Port DC Circuit Breaker (HMPDCCB)—a novel solution tailored for MTDC systems. Unlike conventional Hybrid DC Circuit Breakers (HDCCBs), which necessitate separate breakers for each terminal, the proposed HMPDCCB utilizes a single common breaker with shared energy dissipation branches. This design significantly reduces system complexity, cost, and response time while effectively managing high fault currents and voltage demands.

The HMPDCCB provides selective protection for all connected DC lines and integrates current-limiting inductors (CLIs) to limit fault current rise. Its main breaker branch,

incorporating IGBTs with parallel surge arresters, ensures rapid fault isolation with minimal energy losses. The proposed design achieves a fault current interruption time of 1.8ms and a reset time of less than 3ms, demonstrating superior performance compared to existing models.

To validate its effectiveness, the HMPDCCB has been rigorously modeled and simulated using MATLAB Simulink®/Simpowersystems,. The simulation results confirm its ability to deliver fast, reliable, and cost-efficient fault protection for MTDC transmission networks.

5.1 Introduction

The global energy market is shifting towards renewable resources, attracting attention to HVDC due to its lower corona losses, stability, and affordability as discussed in [54]. However, protecting HVDC transmission remains challenging due to sudden fault current rise and no zero-crossing. Thyristor-based breaker solutions are suggested, but turn-off is challenging [132]. The converter can experience DC-side faults, rapidly increasing the fault current tens of times from the normal system current. Thus, quick isolation is necessary to protect the entire power transmission system [133].

The direct current circuit breaker (DCCB) technology can isolate DC problems selectively while maintaining network stability. Hybrid DC circuit breaker (HDCCB) is a potential solution due to its fast action and low power losses as described in study [134]. HDCCBs consist of load current path, main breaker branch, and residual current breaker. However, due to high costs, comprehensive selective protection in the MTDC grid is challenging. HCBs can reduce peak fault current with increased CLIs and parallel MOVs, but installing them on each transmission line increases system costs as highlighted in study [135].

Numerous multi-port hybrid DCCBs have been proposed to address fault isolation issues. However, these breakers have limitations. In [38] multi-port breaker can isolate faults on transmission lines, but it has a longer current interruption time than DC cir-

-cuit breakers. In [136], the DC breaker transfers fault current to a shared main branch but doesn't guarantee selective protection for all connected lines. In [137], fast fault current interruption in a Tangjiawan ±10kV three-terminal DC distribution network requires two complete HDCCBs, making it ineffective for multi-terminal power transmission systems.

Literature suggests various solutions for the n-terminal grid, including CFC-IHCB hybrid DC circuit breaker, which reduces system costs but requires multiple hybrid circuit breakers. In [138] a hybrid converter coordinated DC fault ride-through strategy reduces full-bridge submodules but increases system costs and interruption time due to increased solid-state switches. In contrast, the work in [139] highlights the significance of multi-port DC circuit breakers compared to hybrid DC circuit breakers, which could ultimately decrease the system cost and carbon footprints.

The introduction of a diode-bridge multi-port DC breaker in [13] is complex due to the use of more components and large surge arresters. This results in larger energy losses and increased costs. The multi-port breaker in [140] consists of a bidirectional main branch and a selection branch for every port, with one breaker cell and a string of thyristors. This system is more costly and complex than the multi-port hybrid DC circuit breaker (MHCB).

Recent studies on multi-port hybrid DC circuit breakers (MHCB) have reduced fault current interruption time to less than <3ms in [141], <4ms in [142], <5ms in [143], <10.6ms in [144] and <3ms in [145] and <9.8ms in [146], which is crucial for HVDC protection. However, these reductions are insufficient due to the large fault currents in HVDC systems, which can damage both the transmission system and converter stations instantly.

The MHCB system faces challenges in quickly returning to normal operation after interrupting and clearing fault currents due to multiple lines connected to a single breaker. Researchers have reduced this time to 14ms in [141], 15ms in [142], 12ms in [143], 11ms in [144], 6ms in [145] and 19ms in [146], but to make the MHCB compatible with the MTDC system, improvements in current interruption time and breaker reset time could be made. Conventional breaker topologies use absorber components like snubber

networks and nonlinear resistors to dissipate fault current after the main fault current interruption [117]. However, some energy can be regenerated and reused, especially in high-voltage direct current (HVDC) with large fault currents [119]. Regenerative braking could be an efficient solution, reducing the size and cost of circuit breakers and recycling energy. The concept of regeneration, introduced in [123], was tested for low-voltage direct current systems but was not tested for multi-terminal power systems.

To summarize the above arguments, it is concluded that conventional protection schemes for HVDC transmission use hybrid circuit breakers and multiple energy-dissipating devices, increasing system size and cost. Multi-port breakers are suggested to address this issue, but their complex topological structure and solid-state switches compromise fault current interruption and breaker reset time. Current limiting inductors (CLIs) are ignored in multi-port breaker topology, causing potential damage to the entire HVDC network.

The proposed hybrid multi-port direct current circuit breaker topology (HMPDCCB) offers a cost-effective alternative to individual HDCBs at the end of each transmission line, offering a current interruption time of 1.8ms, breaker reset time of 3ms, and fault current regeneration feature after main fault interruption, making it unique compared to previous studies [141–146].

5.1.1 Primary Contributions of the Proposed HMPDCCB

Listed below are the primary contributions of the proposed breaker:

- A novel HMPDCCB breaker is presented for all HVDC connected lines in multi-terminal HVDC systems making the power systems more cost-effective and efficient. The common main breaker branch manages energy and fault current dissipation for all connected HVDC transmission lines, reducing costs and reducing the size of the breaker.
- A new topology is proposed that offers fault current regeneration capability after main fault current interruption, utilizing HVDC transmission's significant fault

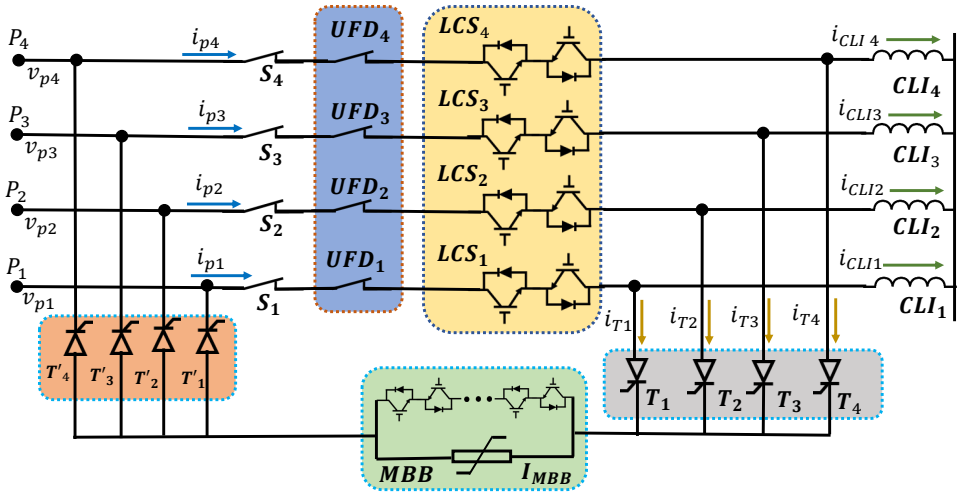


FIGURE 5.1: The proposed topology of hybrid multi-port hybrid high-voltage direct current circuit breaker (HMPDCCB).

current, a unique feature not found in most existing circuit breaker topologies.

- An efficient design is presented that protects HVDC systems from faults within milliseconds. The proposed breaker reduces current interruption to less than 1.8ms and resets the breaker to normal operation within 3ms, using current-limiting inductors to prevent sudden fault current rise.

- A compact topology with fewer components is provided, resulting in a simplified control scheme that makes the proposed circuit breaker compatible with n-terminal HVDC system applications.

- The HMPDCCB topology is thoroughly analyzed, and its effectiveness is verified through a comprehensive comparison with existing circuit breaker topologies.

5.2 The Proposed Hybrid Multi-Port HVDC Circuit Breaker

This section provides an explicit elucidation on the basic fundamental topology of the proposed hybrid multi-port direct current circuit breaker (HMDCB), its integration in the HVDC transmission network, and its operating principles, including key considerations for optimal performance.

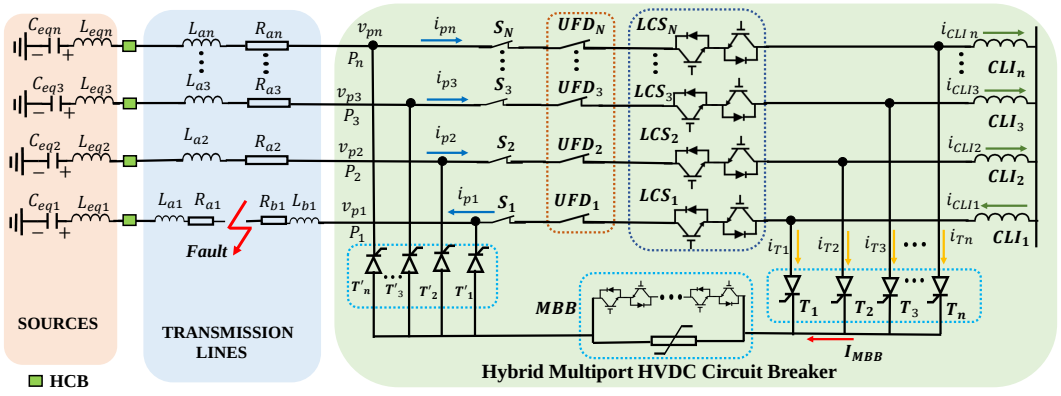


FIGURE 5.2: The generalized model of n-terminal HVDC grid showing, source, transmission lines along with the proposed HMPDCCB.

5.2.1 Fundamental Topology

The topology of the proposed HMPDCCB is illustrated in Fig. 5.1 with four ports used as a test bed model for the protection of a multi-terminal power transmission system. It will replace four typical HCBs required for the protection at the end of each transmission line. It includes CLIs which are responsible for limiting the fault current to reach its maximum threshold level, load commutation switches (LCS), and ultra-fast disconnectors (UFDs), a magnetic mechanical switch to interrupt fault current quickly when needed. These components operate with fewer on-state losses until a fault occurs. When a fault occurs, a shared main breaker branch (MBB) is used to dissipate fault energy. Thyristors are used as controlled switches to route fault current towards the MBB only in case of fault, and thyristor T' is used to route regenerated fault current towards the source. Section 5.2.3 provides the theoretical analysis of the proposed topology of the breaker.

5.2.2 HMPDCCB Integration in HVDC Transmission

A generalized model for multi-terminal high-voltage direct current transmission, as shown in Fig. 5.2, which includes n-number sources represented by (C_{eq1}, ..., C_{eqn}) equivalent capacitors, equivalent inductors (L_{eq1}, ..., L_{eqn}), then a hybrid circuit breaker (HCB) for source protection. Afterwards, HVDC transmission lines are showcased by line inductance as (L_{a1}, ..., L_{an}), and line resistances as (R_{a1}, ..., R_{an}). Moreover, at

port-1, a line-ground fault occurs which breaks the transmission line-1 into (L_{a1}, R_{a1}) and (L_{b1}, L_{b1}). Moving forward, the proposed hybrid multi-port direct current circuit breaker (HMPDCCB) is installed to protect n-transmission lines. This figure gives the complete picture of the HVDC transmission along with the (HMPDCCB) breaker as well. The basic difference between these two figures is that Fig. 5.1 is only the topology of the proposed HMPDCCB, whereas, Fig. 5.2 is the integration of the proposed HMPDCCB topology in the HVDC transmission network.

5.2.3 Operating Principles

This section provides a detailed explanation of the proposed hybrid multi-port direct current circuit breaker's (HMPDCCB) working principles. The HPMDCCB's theoretical foundation is explained using equivalent circuits for each state, consisting of four: normal operation, fault current limiting, fault current interruption, and current regeneration state, starting with the normal state.

5.2.3.1 Normal Operation State (Before t_0)

In the normal operating state, the current will flow through the load commutation switch (LCSn), ultra-fast disconnectors (UFDn), and current-limiting inductors (CLIn) of all the terminals, as shown in Fig. 5.3. This state will continue to operate with fewer on-state losses until a fault occurs, however, in case of a fault. The remaining breaker network is common for all the HVDC transmission lines. For instance, thyristors (T_1 to T_n), (T_1' to T_n'), and the main breaker branch (MBB) including IGBTs and surge arresters. This network will remain off during normal operation maintaining fewer on-state losses.

For theoretical analysis of this state, equivalent circuit of a single branch is shown in Fig. 5.4 including source equivalent capacitor C_{eqn} and inductor L_{eqn} and transmission line inductor and resistance of L_{an} and R_{an}, and the voltage equation during this state will be (5.1). Here, V_{main} is the main source voltage, $V_{aux(n)}$ is the load side voltage and

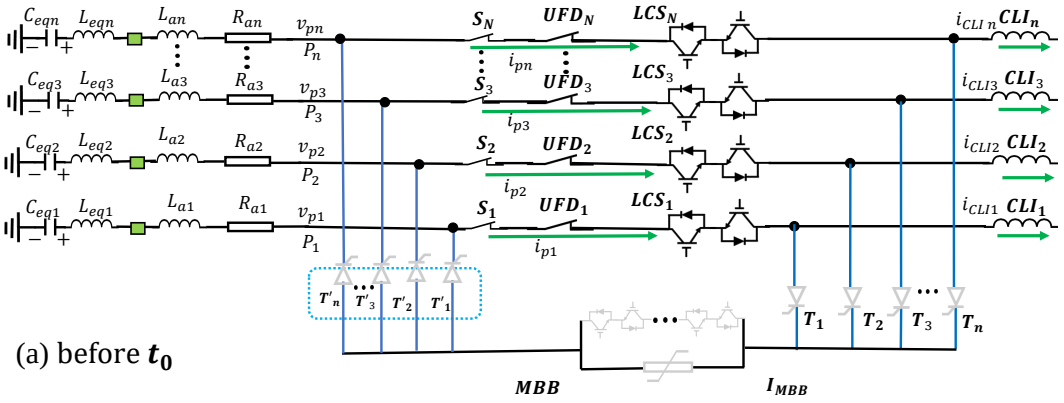


FIGURE 5.3: Before t_0: Normal operation state of the HMPDCCB.

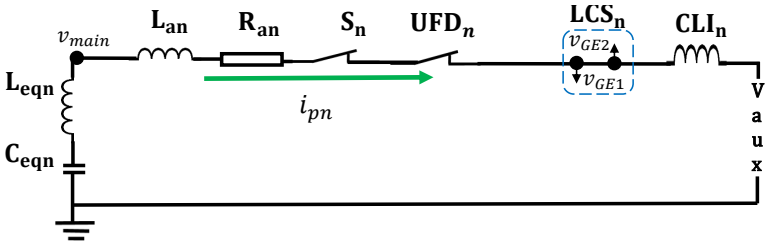


FIGURE 5.4: Equivalent circuit of the single terminal during normal operation state of HMPDCCB.

the rest is the voltage drop across the breaker as,

$$\begin{aligned} V_{\text{main(n)}} - V_{\text{T.line(n)}} - V_{\text{s(n)}} - V_{\text{UFD(n)}} - V_{\text{LCS(n) (1)}} \\ - V_{\text{LCS(n)(2)}} - V_{\text{CL1(n)}} - V_{\text{aux(n)}} = 0. \end{aligned} \tag{5.1}$$

For an ideal circuit breaker, the voltage at the source side should be equal to the voltage at the load side as elaborated in (5.2). Here, the voltage drop across the MPHDCCB breaker is assumed as negligible as an ideal circuit breaker as,

$$V_{\text{main(n)}} \approx V_{\text{aux(n)}}. \tag{5.2}$$

Thus, the current of the normal operating state could be calculated as (5.3). In this state, the breaker will continuously sense the differential voltages of the current limiting inductors (CLIs) of all the terminals, and until and unless the differential voltage of any terminal's CLI is ten times greater than any other terminal CLI, the normal operation will continue its work for a long period. Whereas, the $V_{aux(differential)}$ is the voltage at

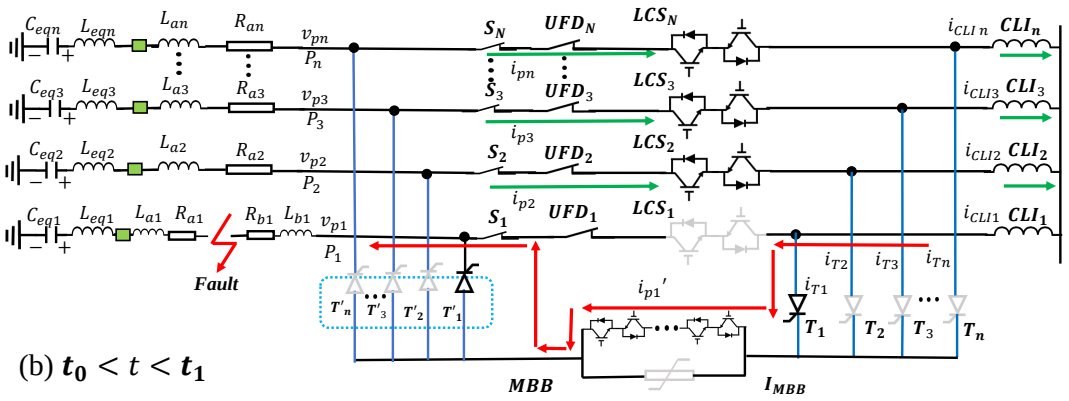


FIGURE 5.5: $t_0 < t < t_1$: Fault current limiting state of the HMPDCCB.

the load side of the CLI as,

$$i_n = \frac{\sum_1^n \Delta\delta V_{pn}}{\sum R_{\text{normal}}}, \tag{5.3}$$

where,

$$\begin{aligned}\sum R_{\text{normal}} =& R_{\text{S(n) close}} + R_{\text{UFD(n) close}} + \\ & R_{\text{CE-1(n) close}} + R_{\text{CE-2(n) close}} \\ & + \frac{V_{\text{aux (differential)}}}{\frac{1}{L}\int V_{\text{aux (differential)}}\, dt} |||[2\pi f l],\end{aligned}$$

given, X_{CLI} = AC reactance = $2\pi f l$ and R_{CLI}= DC resistance = $\frac{V_{\text{aux (differential)}}}{\frac{1}{L}\int V_{\text{aux (differential)}}\, dt}$.

5.2.3.2 Fault Current Limiting State ($t_0 < t < t_1$)

The HMPDCCB's controller constantly checks the differential voltages of all the (V_{CLI1} ... V_{CLIn}) current-limiting inductors. If $V_{\text{CLI-n}}$ is greater than $5V_{\text{CLI-n}'}$, a fault occurs at the nth terminal. In our case, a fault has occurred at port-1, because the CLI-1 has the highest voltage compared to the rest of the CLIs. To stop the HMPDCCB breaker from generating a long-time electric arc, it is necessary to first open LCS1 to interrupt the circuit because fault current will still pass through this arc and can damage the entire system within milliseconds. This could be done by commutating fault current by triggering thyristor T_1, though increasing its gate voltage from its threshold value, like 3V, using the suggested thyristor from the k0900ME650 datasheet. Then IGBTs of LCS are triggered by increasing its gate voltage from its threshold value, like 7.3V,

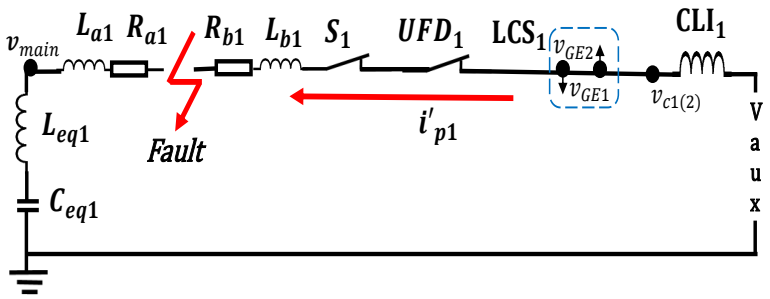


FIGURE 5.6: Equivalent circuit of branch-1 during fault detection and the current limiting the state of HMPDCCB.

using the suggested IGBT from the 5SNA3000K452300 datasheet [109], there are surge arresters in the parallel to snub the voltage spike due to fault occurrence. The main aim of this state is to commutate fault current to prevent UFD from generating long-time electric arcs. As when a fault occurs, if UFD is open instantaneously, the fault current will still pass through the electric arc, across the mechanical switch and can damage the entire system within milliseconds. Thus, the fault current needs to commutate first, as soon as the magnitude of the fault current decreases, the UFD will be open for smooth operation. The 'inductive kickback effect' increases the voltage across the breaker's inductors when the transmission line breaks, causing voltage buildup across the breaker's inductor. *Lenz's law* suggests that a change in the magnetic field across the inductor can cause the current to reverse its direction, potentially damaging the entire HVDC transmission system and potentially damaging the source. Thus, the breaker must be activated promptly to safeguard the system as depicted in Fig. 5.5.

At t_0, When a short-circuit fault occurs and the fault current rises, the HMPDCCB receives a trip signal to protect UFD-1 from electric arc generation. After evaluating the faulty port, the potentials of $V_{GE(1)1}$ and $V_{GE(1)2}$ should be turned to zero, and $R_{EC(1)1}$ should become large enough to hinder the back EMF of CLI (1).

The equivalent circuit in Fig. 5.6 demonstrates that when a fault occurs, the CLI will limit the instantaneous change of current and the rate of change. As the voltage potential across the CLI-1 increases due to the fault, the current direction changes from i_{p1} to i'_{p1}. The differential voltage of CLI of port-1 is represented as,

$$V_{\text{CLI(1)differential}} = V_{\text{(1)collector(2)}} - V_{\text{aux(1)}}, \tag{5.4}$$

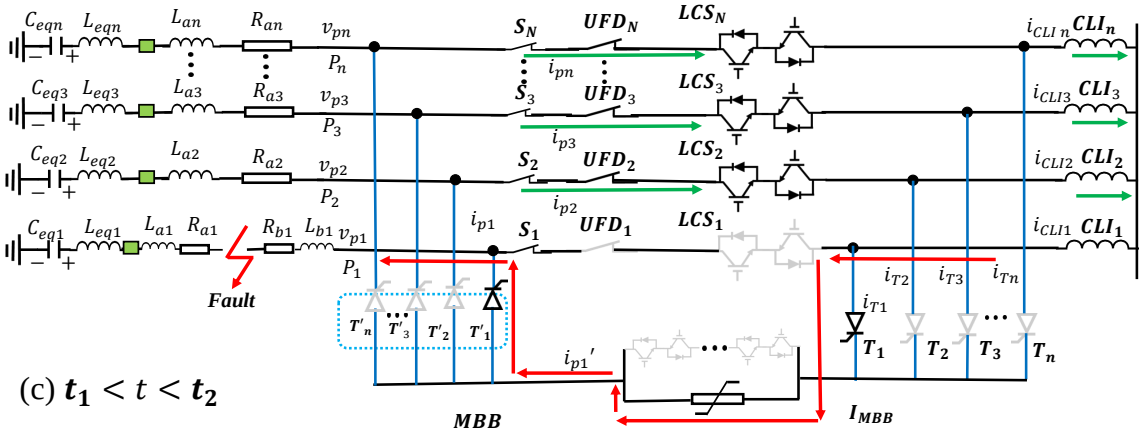


FIGURE 5.7: $t_1 < t < t_2$: Fault current interruption state of the HMPDCCB.

where, $V_{CLI(1)differential}$ is differential voltage of CLI, $V_{(1)collector(2)}$ is LCS's CLI side voltage, and $V_{aux(1)}$ is load voltage. (5.4) will ultimately satisfy the (5.5) and (5.6). For instance, the voltage of a faulty terminal will be five times higher than the voltage of all other CLIs as,

$$\lim_{t \to t_0} V_{\mathrm{CLI}(1)max} \geq |5V_{\mathrm{CLI}(1)'}|, \tag{5.5}$$

$$\left|V_{\mathrm{aux}(1)} - V_{c(1)2}\right| > \left|V'_{\mathrm{aux}(1)} - V'_{c(1)2}\right|. \tag{5.6}$$

5.2.3.3 Fault Current Interruption State ($t_1 < t < t_2$)

The fault current interruption process begins after identifying and commuting fault current to the main breaker branch for effective energy dissipation, starting with the opening of UFD-1. This could be done by turning off the IGBTs in the main breaker branch, while the parallel surge arresters offer less resistance during this time, facilitating fault current to dissipate in these arresters, as depicted in Fig. 5.7. This parallel configuration saves IGBTs from large power stresses. IGBTs in the main breaker branch are turned by increasing the gate voltage of IGBTs of the main breaker branch from its threshold value of 7.3V as given in (5.7). As a result, these IGBTs will offer high resistance, and the current will be directed to the surge arresters, as shown in Fig. 5.8, to dissipate fault energy in the form of heat, and the main fault current will start decreasing as,

$$\int_{t=0}^{t=0+} V_{\mathrm{GE(MBB)}} > V_{\mathrm{threshold}}. \tag{5.7}$$

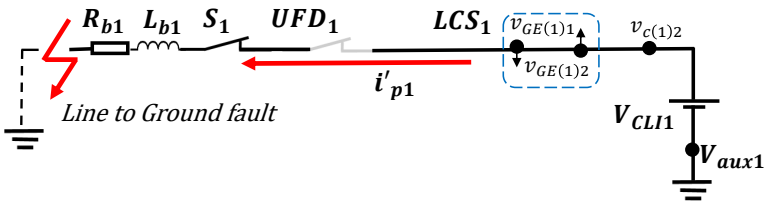


FIGURE 5.8: Multi-port hybrid DC circuit breaker's fault current interruption state's equivalent circuit when the line to ground fault occurs.

This state will last till time t_2 when the fault current is interrupted and starts decreasing. The dissipation of fault current mainly depends upon the inductive time constant of the breaker's CLI, as given in (5.8),

$$\tau_L = \frac{L}{R}. \tag{5.8}$$

The thyristor's activation mechanism is determined by the gate-to-cathode voltage of the thyristors, as given in (5.9). The same is the mechanism for the compliments of thyristors on the other side given as,

$$\begin{aligned} V_{\mathrm{GK(1)THY}} &= V_{\mathrm{G(1)THY}} - V_{\mathrm{K(1)THY}}, \\ V_{\mathrm{GK(2)THY}} &= V_{\mathrm{G(2)THY}} - V_{\mathrm{K(2)THY}}, \\ V_{\mathrm{GK(3)THY}} &= V_{\mathrm{G(3)THY}} - V_{\mathrm{K(3)THY}}, \\ V_{\mathrm{GK(}n\mathrm{)THY}} &= V_{\mathrm{G(}n\mathrm{)THY}} - V_{\mathrm{K(}n\mathrm{)THY}}. \end{aligned} \tag{5.9}$$

In our case of the selected thyristor, K0900ME650 the gate to cathode voltage is 3V. Thus to trigger thyristor V_{GK} we need to increase the voltage of the thyristor from above the $V_{GK} > 3$V. After the interruption of fault, we need to develop a proper mechanism to route the i'_{p1}, and here is regeneration state begins. Thus, in this situation, (5.10) will be satisfied to trigger T'_2 at this time as,

$$V'_{\mathrm{GK(2)THY}} > V_{\mathrm{threshold}}. \tag{5.10}$$

Whereas, the rest of the thyristor complement will remain off at this time by satisfying (5.11) below,

$$\left.\begin{aligned} &V'_{\mathrm{GK(2)THY'}} \\ &V'_{\mathrm{GK(3)THY'}} \\ &V'_{\mathrm{GK(}n\mathrm{)THY'}} \end{aligned}\right\} < V_{\mathrm{threshold}}. \tag{5.11}$$

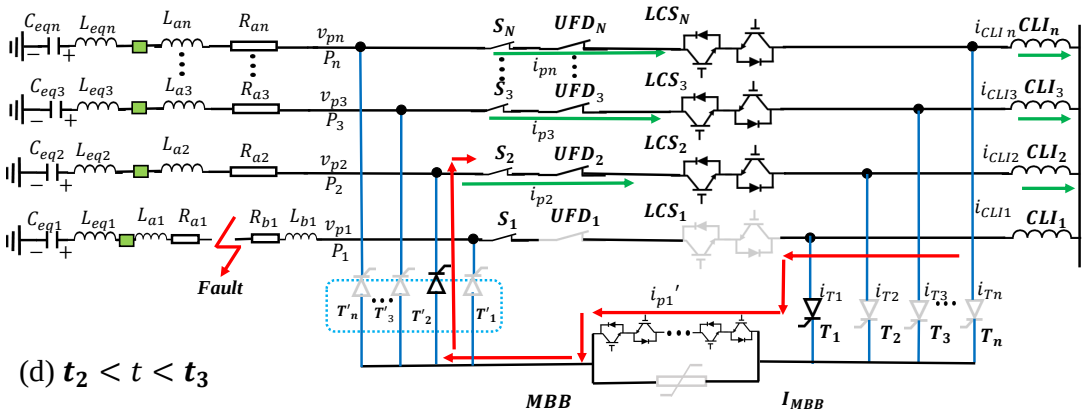


FIGURE 5.9: $t_2 < t < t_3$: Current regeneration state of the HMPDCCB.

5.2.3.4 Current Regeneration State ($t_2 < t < t_3$)

The regeneration decision is based on the port voltages of different transmission lines, with the node having minimum voltage preferred for receiving the regeneration current. As previously declared, the port with the largest CLI voltage is the faulty port, and the current is dissipated until the fault is interrupted. After the interruption of fault current, some of the energy is reused/regenerated and directed toward the minimum voltage port. As previously declared, the port with the largest CLI voltage is the faulty port, and the current is dissipated until the fault is interrupted. After the interruption of fault current, some of the energy is reused/regenerated and directed toward the minimum voltage port, as the path of the current is shown in Fig. 5.9. In our case, port-2 has the minimum voltage so the regenerated current is diverted towards port-2.

Thus, the current flow from terminal-2 will be the sum of the original current flowing through port-2 $i_{2(p)}$ and the regenerated current i'_{1p} as depicted in its equivalent circuit Fig. 5.10, as well. The enhanced current will be seen in the manner given in (5.12) to ensure that the current i'_{p1} is completely channelled towards port-2 as,

$$i'_{\mathrm{CLI}(2)} = i_{2(p)} + i'_{1p}, \tag{5.12}$$

Originally the current flowing through port-2 is given in (5.13) as,

$$i_{p(2)} = \frac{\sum_1^1 \Delta\delta V_{2p}}{\sum R_{p(2)}}, \tag{5.13}$$

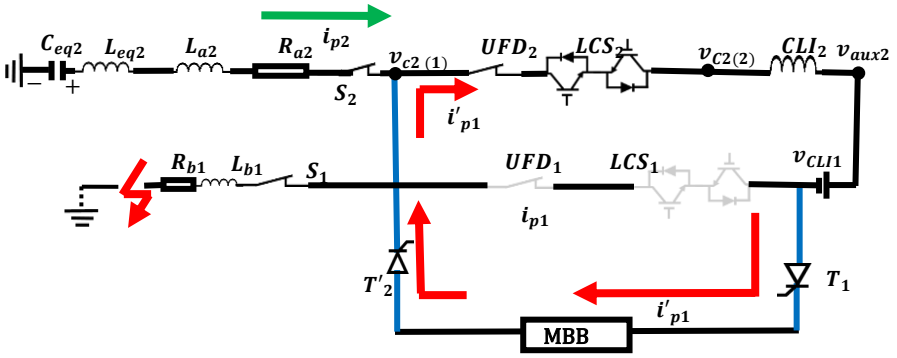


FIGURE 5.10: Fualt current reuse/regeneration path in HMPDCCB is presented here in the form of its equivalent circuit.

$$\sum R_{p(2)} = R_{S(2)close} + R_{\text{UFD(2) close}} + R_{\text{CE1(2) close}} + R_{\text{CE2(2) close}} + \frac{V_{\text{CLI(2) differential}}}{\frac{1}{L}\int V_{\text{CLI(2) differential}} dt} || [2\pi f l_{\text{CL1(2)}}].$$

However, the current flow through $V_{c1(2)}$ node will be the current in (5.14) as,

$$\begin{aligned} i'_{p(2)} &= \sum_{p1}^{p2} [i'_{p(1)}, i_{p(2)}], \\ &= i'_{p(1)} + i_{p(2)}. \end{aligned} \tag{5.14}$$

The current to be regenerated/reused will be current in (5.15) as,

$$i'_{p(1)} = \frac{\delta V_{\text{cc(1,2)}}}{\sum R_{p(1)'}}, \tag{5.15}$$

where,

$$\sum R_{p(1)'} = R_{\text{T1 (close)}} + R_{\text{S (close)}} + R_{T2(close)'}.$$

Thus, after putting (5.13) and (5.15) in (5.14) we get (5.16) as,

$$i'_{p(2)} = \frac{\delta V_{\text{cc(1,2)}}}{\sum R_{p(1)'}} + \frac{\sum_1^1 \Delta\delta V_{2p}}{\sum R_{p(2)}}. \tag{5.16}$$

Hence, (5.16) will be the new current flowing through port-2 which combines both

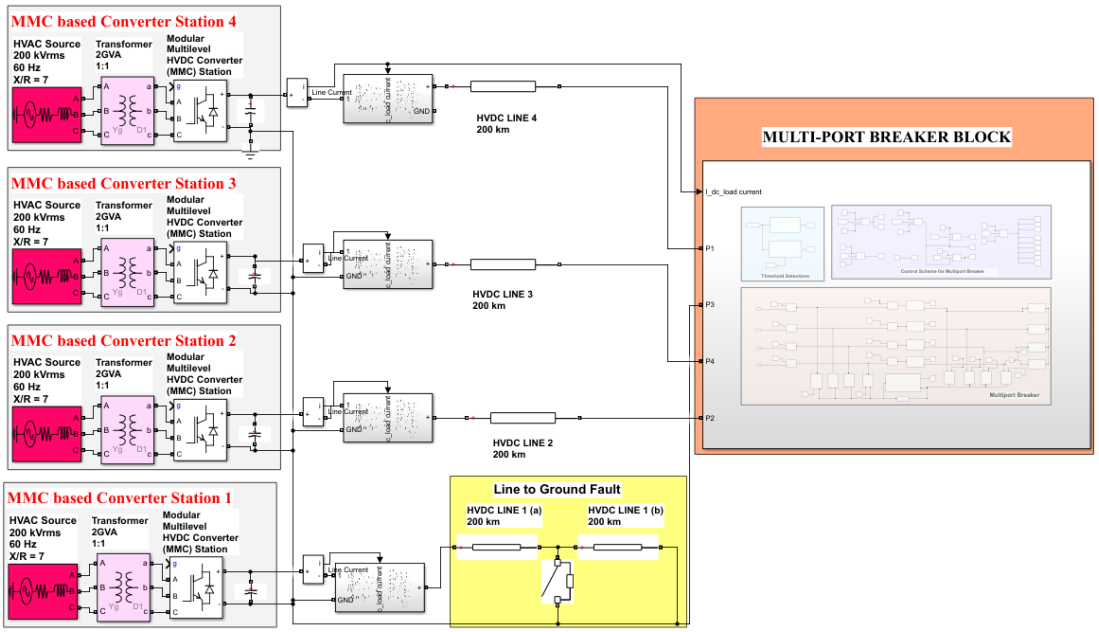


FIGURE 5.11: The simulation test-bed model of the proposed hybrid multi-port DC circuit breaker (HMPDCCB).

the original current of port-2 along with the regenerated current.

As soon as the process of regeneration is done when V_{p2} are approximately equal to V_{CLI1}. Then breaker will go to the reclosing condition by sequentially turning off the thyristor branches T_n and T'_n. After that, UFD-1 and LCS-1 will be triggered, and the system will be brought back to normal operation. At this time fault is cleared, and breaker closing will be safe and non-distinctive upon reclosing. Moreover, reclosing is crucial for restoring the system to normal operation.

5.3 Simulation Setup

MATLAB's Simulink®/Simpowersystems was used to test the performance of the proposed HMPDCCB, as shown in Fig. 5.11. The testbed, including the source, HCB, transmission lines, and HMPDCCB, has experienced a line-to-ground fault to evaluate the system's dynamic response and fault-clearing capabilities under realistic operating conditions. Table 5.1 provides a comprehensive list of essential variables used in the simulation model, including system voltages, fault impedance, breaker ratings, inductance values, and control logic parameters for an accurate and detailed analysis.

5.3.1 The Test-bed Model

The MATLAB simulation test-bed model of the HVDC transmission network is depicted in Fig. 5.11. It includes four AC source ports each of rating 200kV_{rms}, then a transformer to step up the voltage, and then multi-level modular converter-voltage source converter (MMC-VSC) based mono-polar converter stations to convert AC voltages into DC. MMC-VSC will act as a rectifier on this side, using IGBTs as a switching configuration. The capacitor banks are installed after the MMC to reduce the ripples of the receiving voltage. The proposed circuit breaker HMPDCCB is installed after the HVDC transmission lines to protect the multiple transmission lines with a single hybrid multi-port direct current circuit breaker (HMPDCCB). In this case, a line-to-ground fault is created at transmission line-1. This simulation helps to verify the results of the HMPDCCB. The design parameters of the Source, HVDC network, transmission line, converter, and HMPDCCB breaker are presented in Table 5.1. The practical voltage source of 200kV (RMS) is chosen for the proposed system because it has an internal resistance of 1.2Ω and an internal inductance of 1.658 mH. An ideal voltage source has no internal resistance or inductance, whereas, in reality, every voltage source exhibits these characteristics. It has an X/R ratio of 7, indicating that it is primarily inductive. Therefore, the chosen source aligns with real-world power system characteristics and is a practical and appropriate choice.

The parameters were chosen to reflect realistic and optimal design requirements for an HVDC transmission system, ensuring efficiency, reliability, and compatibility with typical operating conditions. The mono-polar/n-terminal VSC HVDC type with a 250kV grid voltage aligns with standard industry practices for high voltage applications, offering flexibility in configuration. The transmission line lengths (100km, 200km, and 500km) represent typical ranges for long-distance power transfer, with resistance, inductance, and capacitance values carefully selected to reflect practical line behavior. The converter design, using IGBT switches and a 1000μF capacitor, ensures efficient AC/DC conversion with stable voltage control. The HMPDCCB breaker parameters, such as its 2kA rated current, 30kA interruption capacity, and 1.8ms interruption time, support safe and fast fault isolation while minimizing system disturbances. Overall, these values

TABLE 5.1: The design parameters of the system.

Device	**Parameters**	**Values**
Source	Voltage source	200kVrms
	Source Resistance	1.2 Ω
	Source Inductance	1.6581mH
	AC system X/R	7
	Frequency	60 Hz
HVDC network	VSC HVDC type	Mono-polar/n-terminal
	MTDC grid voltage	250kV
	Normal currents MMC1, MMC2, MMC3, MMC4	0.89kA, 2kA, 0.82kA, 2kA
	Power consumption	222.5MW, 500MW, 205MW, 500MW
Converter	Type	AC/DC (Rectifier)
	Switching device	IGBT
	Capacitor	1000μF
Transmission line	Length of each line	100km, 200km, 500km
	Resistance of each line	0.015mΩ, 0.022mΩ, 0.036mΩ
	Inductance of each line	0.792mH, 0.833mH, 0.921mH
	Capacitance of each line	14.4nF
Converter	Type	AC/DC (Rectifier)
	Switching device	IGBT
	Capacitor	1000μF
HMPDCCB breaker	Rated voltage	250kV
	Rated current	2kA
	Current interruption capacity	30kA
	Current interruption time	1.8ms
	Breaker reset time	3ms
	Breaker inductance (L)	300mH
	Breaker resistance (R)	125Ω

were chosen to meet technical constraints, operational demands, and the performance requirements of a modern HVDC system.

5.3.2 Control Algorithm

This section presents the control algorithm for the proposed HMPDCCB. Various fault sensing methods are used in HVDC circuit breakers, including overcurrent sensing, rate of change of current, voltage sensing, and power differential protection. In the proposed hybrid HVDC circuit breaker topology, voltage sensing has been adopted for fault detection. The controller continuously monitors the differential voltage across the current-limiting inductors (CLIs), using it as a threshold to detect faults. If the voltage

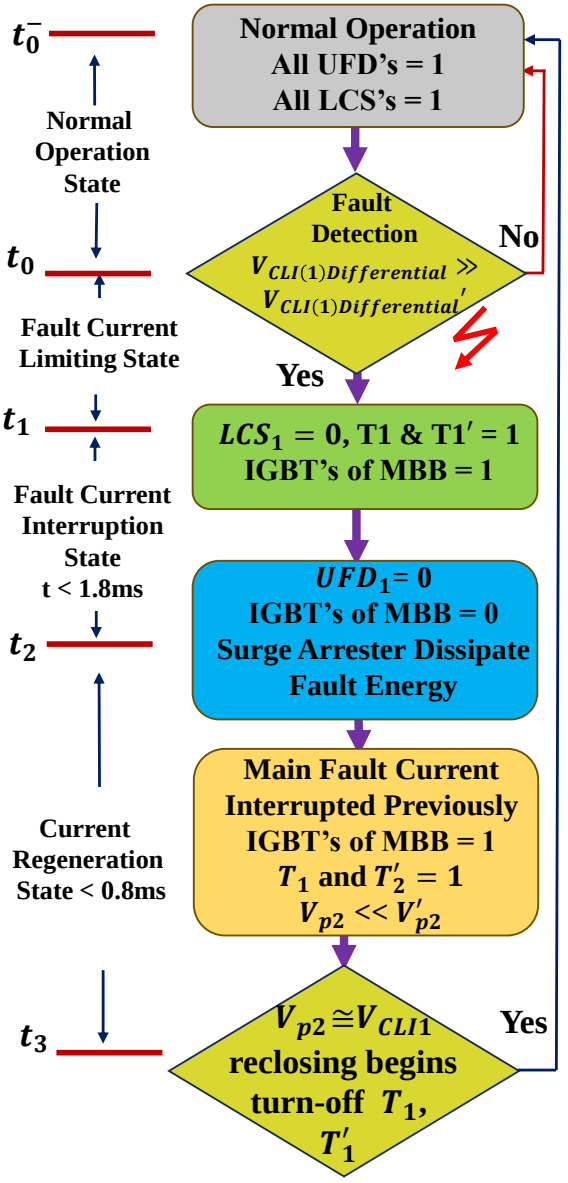


FIGURE 5.12: The control algorithm for the controller module of the hybrid multi-port DC circuit breaker (HMPDCCB).

of a particular VCLI branch exceeds that of its corresponding VCLI', the system identifies that branch as faulty and activates the breaker. Once a fault is detected, the topology first sends a commutation signal, followed by a trip signal, to isolate the fault. Voltage sensing is preferred in this scenario due to its high reliability and fast response time. In practical applications, Hall Effect sensors are commonly used for this purpose in high-voltage DC circuit breakers.

The controller module is illustrated in Fig. 5.12. Initially, the system operates normally with ultra-fast disconnectors ($UFD_1, \ldots, UFD_4$) and load commutation switches

($LCS_1, \ldots, LCS_4$) triggered on all terminals until a fault occurs. Upon fault detection, the controller moves to the next step; otherwise, it remains in its initial state. Once a fault is detected, the fault current is diverted toward the main breaker branch via thyristor T_1, and $LCS1$ is turned on at this stage. The IGBTs in the main breaker branch then pass the fault current by opening UFD1 and LCS1 switches.

Once the main fault current is interrupted, the remaining fault energy must be dissipated. The proposed topology ensures the regeneration of residual fault energy, with the decision based on terminal port voltages. Port-2 is selected for regeneration due to its minimum voltage. Gradually, the fault current decays to zero, clearing the fault and restoring the breaker to normal operation. The regeneration process continues until V_{p2} voltage becomes approximately equal to V_{CLI1} voltage. The thyristor branches T_n and T_n' are sequentially turned off to ensure breaker closure and restore normal system operation. The concept for the proposed controller was inspired by [147, 148].

5.4 Model Validation

This section outlines a protection logic sequence, detailing the time it takes for fault current interruption, regeneration, and breaker reset to restore the breaker to normal operation. Its subsection will analyze the available components and their required quantity for hardware setup deployment for the proposed HMPDCCB. The multiple states of protection enable the efficient working of various HMPDCCBs, providing a clearer understanding of the breaker's functioning.

5.4.1 Logic Sequence for Protection

Current interruption is sensitive to interrupting faults quickly [59, 126], but clearing faults requires energy dissipation, causing delays in breaker rest time [149]. Our proposed topology of HMPDCCB reuses energy and sends it back to the grid, after the interruption of the main fault current, which would be dissipated otherwise, like in the conventional topologies. The state of current interruption protection can be coordinated

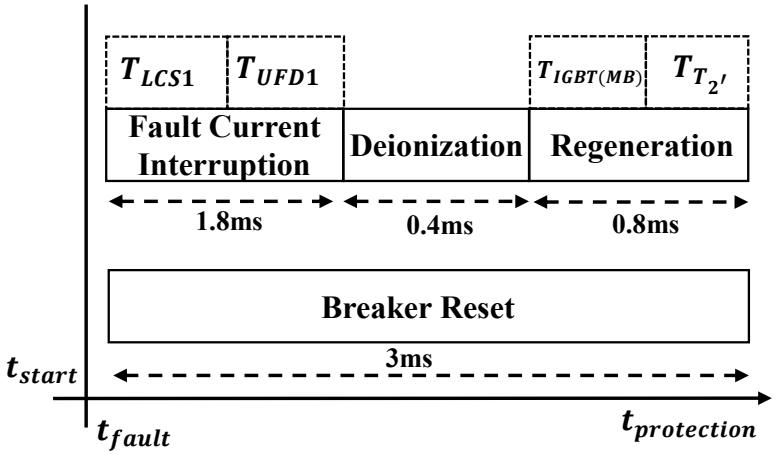


FIGURE 5.13: Logic sequence representation for the protection in hybrid multi-port DC circuit breaker (HMPDCCB).

with regeneration and breaker reset controls signal. Fig. 5.13 represents that the current interruption gets on within 1.8ms with the time of UFD1 and some delay after that is the ionization/transition state when the main fault current is interrupted. As the fault current path is diverted towards the surge arresters of the main breaker branch, the fault energy starts dissipating through them and in less than 0.4ms dissipation of the fault remains to continue. At this time, the maximum energy of the fault will be cleared and the process of regeneration will begin. This regeneration process will take less than 0.8ms and the fault will be clear within 3ms. Thus, the logic sequence presents a clear picture of fault current interruption and brings the system back to its original condition.

5.4.2 Components and Design Analysis

The main breaker branch's sub-modules (SMs) will experience varying electrical stresses when the HMPDCCB operates in different states. The HMPDCCB's design is directly influenced by the maximum current and voltage stress, making series and parallel connections crucial for its protection during operation [56]. This is the reason in the proposed HMPDCCB, it includes surge arresters installed in parallel in the main breaker branch. When IGBTs are turned off, surge arresters reduce resistance and snub voltage spikes, allowing the breaker to operate uninterruptedly, safely, and smoothly, eliminating the need for IGBTs to bear significant turn-off power stresses.

Table 4.2 displays the power electronic components needed for a 250kV HMPDCCB, along with their cost and operational time. IGBTs, thyristors, and diodes are fast enough resulting in a breaker current interruption time of less than 1.8ms and altogether restoring the breaker within 3ms.

The number of IGBTs in each group of SM increases with a larger n, resulting in a more steady and smooth current. However, current limiting requires fault current magnitude, not current stability, so n_{SM} doesn't need to be large for circuit breaker control.

Surge arresters in sub-modules of the main breaker branch protect IGBTs from large voltage or current stresses. AC side protection is insufficient for large direct current faults in multi-terminal direct current transmission systems. DC transmission lines have negligible impedance, making fault currents abrupt and damaging systems within milliseconds. The commercial implementation of a hybrid multi-port direct current circuit breaker is necessary to harness renewable energy in remote locations through cheap HVDC transmission. The proposed topology is rigorously tested on software, however, hardware implementation could be implemented in the future.

5.5 Results and Discussion

This section provides a comprehensive critical analysis of the proposed hybrid multi-port direct current breaker's (HMPDCCB) electrical currents, voltages, and energy behavior. Moreover, comparative analysis is also presented in this section.

5.5.1 Electrical Current Analysis

Fast fault current interruption is crucial in high voltage direct current transmission due to its negligible line impedance, causing a sudden increase in fault current and potential damage within milliseconds [128]. The proposed hybrid multi-port direct current circuit breaker topology (HMPDCCB) significantly reduces fault current interruption time to 1.8ms by using a shared energy dissipation branch for fault at any transmission line. This reduces the number of breaker components, resulting in reduced turn-on time for

switching. Moreover, the current limiting inductors (CLIs) of the breaker slow down the abrupt rise of the fault current, thus providing a window to interrupt the fault current before reaching its maximum threshold level. The main breaker branch is connected to a Thomson-coil actuator with a fast action speed and 1ms opening time, capable of handling and interrupting maximum current quickly, featuring both magnets for attraction or repulsion as mentioned in [126].

The current analysis of the proposed HMPDCCB topology shows that the amount of current flowing from each branch and component holds a significant value. This study primarily focuses on the current interruption time of the fast fault. For instance, Fig. 5.14(a) represents the current waveform of port-2. The figure shows that before time t_0, normal operation is running in the system with a system current of 2kA. However, at 0.3s, the fault occurs, and the fault current starts increasing abruptly. A line-ground fault has been created in our test-bed simulations to check the effectiveness of the proposed breaker topology. Thus, the proposed breaker HMPDCCB has interrupted the fault current around 5.9kA within 1.8ms. The threshold on breakers' inductors voltages is set to detect fault presence when V_{CLI1} exceeds V'_{CLI1}, initiating the fault-clearing process. In contrast to our breaker, the article [141] breaker takes 3ms to interrupt when its fault current reaches 9kA, due to its inductor bypass branch (IBB) and main breaker branch (MBB), which increases the breaker's size and fault current interruption time. Similarly, another study [143] shows a fault current interruption time of 5ms due to separate main selector branches protecting transmission lines, while the complex topology of the main breaker branch for energy dissipation leads to longer switching times and increased interruption time. Moving forward, [145] and [146] have fault current interruption times of 3ms and 9.8ms respectively, they have a topological configuration with series-parallel combination, along with a reverse and forward fault current behaviour analysis, for this analysis, their fault current interruption time is significantly compromised.

Furthermore, the proposed HMPDCCB breaker gets reset within 3ms, and it gets operational for the next operation, which is also a distinguished feature as other topologies take a minimum of more than 6ms as given in Table 5.2. This is because the IGBTs (5SNA3000K452300) and thyristors (k0900ME650) used in the proposed topology have

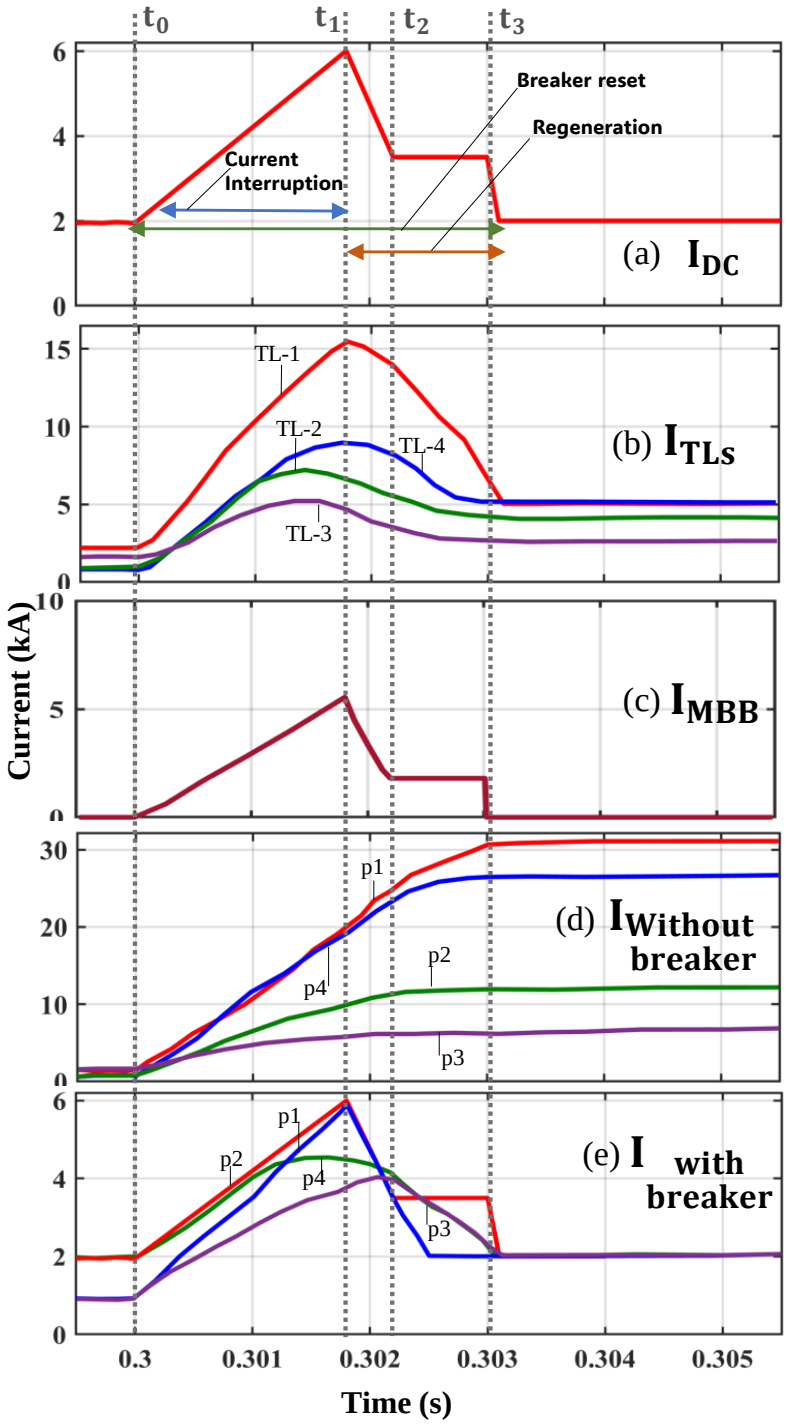


FIGURE 5.14: Current waveforms of the hybrid multi-port DC circuit breaker (HMPDCCB) for its four operation states (t_0 to t_3).

a turn-on time in nano-seconds. Moreover, when the main fault current is interrupted at time t_2 and the fault current starts decreasing, some of the fault current will be regenerated and sent back to the grid as thoroughly discussed in the operational states of HMPDCCB (Section 5.2.3.4). Thus, the current of port-2 will increase to 3.5kA during

current regeneration as the fault current is completely cleared at t_3.

Fig. 5.14(b) represents the current flowing through the transmission lines of all four ports of the proposed HMPDCCB. For instance, before t_0 normal currents of port-1, port-2, port-3, and port-4 are 0.89kA, 2KA, 0.82kA, and 2kA respectively. During the fault, the current starts rising until the trip signal is received at time t_1. The maximum current during a fault in multiple ports reaches 14kA, 7kA, 6kA, and 4kA, respectively. The CLIs of the breaker topology effectively limit fault current from reaching the system's maximum threshold, with the faulty port being taken based on its maximum current being almost five times greater, like $I_{TL(n)} \gg 5I'_{TL(n)}$ than all other ports.

When a fault occurs, all transmission lines current rush towards a less impedance path. The interruption process is facilitated by the current limiting state, which diverts fault current towards the main breaker branch having surge arresters. These surge arresters absorb the spike of fault current around 5.9kA between time t_1 and t_2 as depicted in Fig. 5.14(c) that I_{MBB} is the current flowing through the main breaker branch surge arresters. The maximum current absorbed by the main breaker branch is 11kA during the current interruption state and dissipates in the form of heat. After t_2 when the main fault current is interrupted the current in the surge arrester will start decreasing due to the regeneration branch reducing the burden on surge arresters. Although this surge absorption is more or less similar to other studies [141, 143, 146] for fault interruption. The proposed HMPDCCB differs from other studies in that after fault interruption, regeneration processes begin, reducing the burden on the surge arrester. Fault current is reused and sent back to the grid, eliminating the need for absorbing it further.

The regeneration process begins at time t_2 and reuses energy stored in the breaker's inductor (CLI-1) from t_2 to t_3. Around 1.5kA current is regenerated when T_1 and T'_2 thyristors are turned on sequentially to reuse fault energy instead of dissipating it. Thus, the proposed HMPDCCB outperforms other studies [141–146] in terms of regenerated energy and interruption time.

Fig. 5.14(d) shows that without a breaker, all ports' currents reach peak values after a fault, causing the entire HVDC system to be damaged within milliseconds. This demonstrates that converter-side protection or AC protection is insufficient for dealing

with large fault currents in high-voltage DC situations, as it can cause significant losses and system damage. The graph highlights the importance of a breaker, as, without a breaker, currents of port-1, port-2, port-3, and port-4 reach 30kA, 12kA, 8kA, and 28kA, respectively, causing system damage within milliseconds. Therefore, a breaker is crucial for preventing system damage.

Fig. 5.14(e) represents the graphs with the breaker, sooner the fault is detected at time t_0 where the fault current starts increasing our breaker HMPDCCB, interrupts the fault current within 1.8ms. As it is a hybrid multi-port DC circuit breaker (HMPDCCB), thus the currents of the ports are interrupted, like port-1 at 5.9kA, port-2 at 6kA port-3 at 4kA, and port-4 around 5kA, which will disconnect right after the occurrence of the fault; all this is done within milliseconds. The result shows that the proposed breaker is efficient enough to break faults with quick fault interruption time.

5.5.2 Voltage Analysis

The HMPDCCB's effectiveness is assessed by measuring voltages across various components of the proposed circuit breaker. Fig. 5.15(a) shows voltage variations across current limiting inductors of all ports after a fault. Port-1 voltage increases to 300kV, while port-2, port-3, and port-4 voltages increase to 100kV, 90kV, and 80kV, respectively. The graphs of the current-limiting inductor show significant variations in voltages across all CLIs after fault, despite their weight being the same 300mH. To identify a faulty port, the voltages of the CLIs of the breaker are sensed continuously by the breaker's controller. A port with a voltage five times higher than all other ports is considered faulty, as indicated by $V_{CLIn} >> 5V'_{CLIn}$. In our testbed model of the proposed topology $V_{CLI1} >> 5V'_{CLI1}$,thus, port-1 is declared faulty. The plot reveals that voltage is initially less before fault time t_0, but after the fault occurrence, the fault current is commutated towards the main breaker branch, and the voltage spike is absorbed by the surge arresters. Thus, fault current interruption with minimal voltage stress is possible with the proposed HMPDCCB due to the parallel configuration of IGBTs and surge arresters in the main breaker branch. The proposed HMPDCCB effectively detects and interrupts faults within 1.8ms, allowing inductor energy to dissipate, a significant impr-

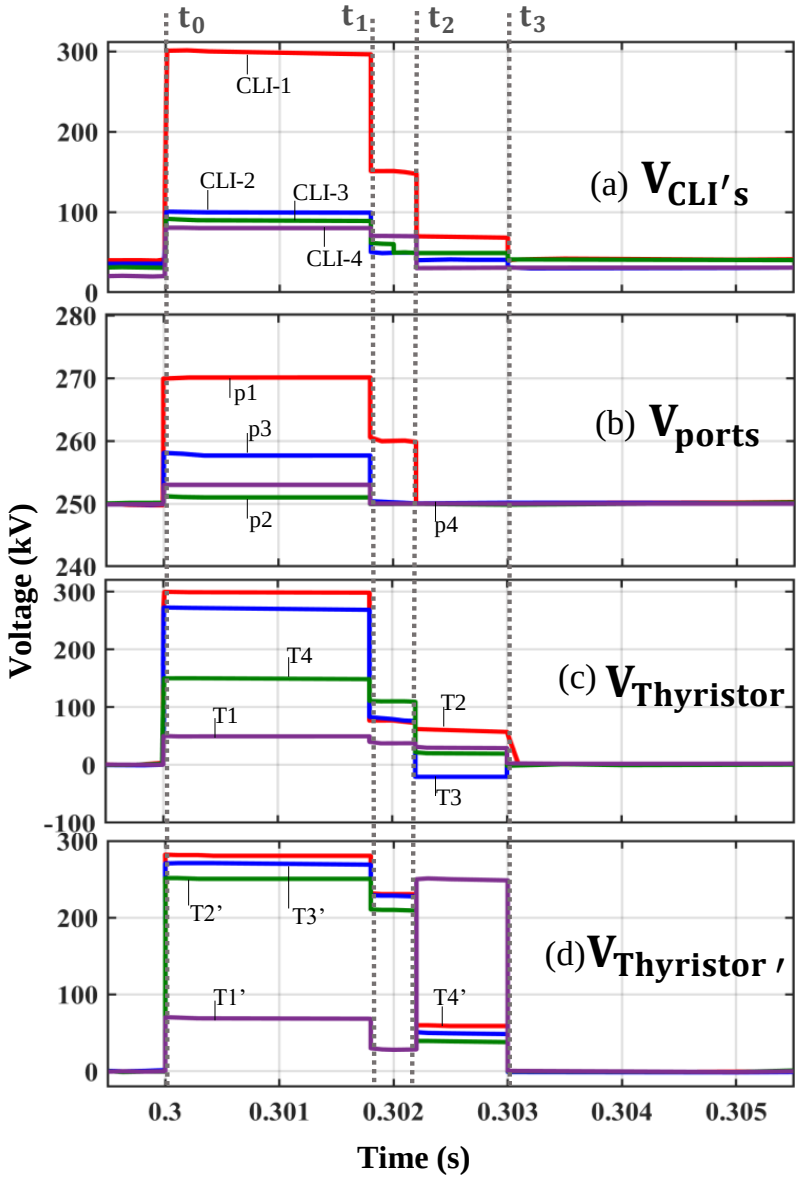


FIGURE 5.15: Voltage waveforms of the hybrid multi-port DC circuit breaker (HMPDCCB) for its different operation states (t_0 to t_3).

-ovement over previous literature studies [141, 143, 145, 146] that require a minimum current interruption time of over 3ms.

Fig. 5.15(b) illustrates the voltage across various ports before and after the occurrence of a fault. The ports' voltages also fluctuate. The voltage at port-1, port-2, port-3, and port-4 increased to 270kV, 252kV, 268kV, and 254kV, respectively. The Port voltages demonstrate that the terminal with the lowest port voltage can receive the regeneration voltage. In this case, the port voltages above show that port-2 has the lowest voltage as compared to all other ports, making it suitable to receive the regeneration voltage.

Similarly, the voltage across the thyristor branch is represented as $V_{Thyristor}$ in Fig. 5.15(c). The thyristor voltage indicates that all open switches have very high voltages. For instance, T_2, T_3, T_4 have high voltages. However, thyristor-1 (T_1) is triggered for current interruption and regeneration later on, acting as a close switch, causing its voltage to decrease during time t_0 to t_1 compared to other switches. Additionally, thyristors are controlled switches that are adaptable to system requirements. Moreover, the thyristor (k0900ME650) has a turn-on time of nano-seconds according to its datasheet making the proposed topology efficient as compared to other studies.

Thyristor complement voltages are compared to validate the efficacy of the proposed circuit breaker HMPDCCB. The voltage waveforms depicted in Fig. 5.15(d) represent the voltage across all thyristors compliments in the topology of HMPDCCB. When a fault occurs at time 0.3s and fault current is routed by triggering thyristor-1 compliment, thus the voltage during its turn-on time will be minimum as compared to voltages flowing through all other thyristor compliment switches e.g., T_2', T_3', T_4' from t_0 to t_1, as these switches are open and have maximum voltage as shown in the graph as well. However, the voltage across thyristor-2 compliment T_2' decreased after t_2 to t_3 during the regeneration process because it will be turned on during this duration. The plot reveals that the voltage stress passing through the thyristors and thyristor complement branch is lower than the existing MHCB topologies in the literature [141, 143, 145, 146] making the proposed HMPDCCB smart and efficient as compared to all other studies.

5.5.3 Comparative Analysis

Fig. 5.16 represents the comparative analysis of the proposed HMPDCCB topology with the DC circuit breaker topologies present in the literature. The graph in blue solid line depicts the fault current interruption time of the proposed HMPDCCB is 1.8ms which is far less than compared topologies. Secondly, the fault current is interrupted around 5.9kA, which is also the distinguishing feature, like the system is interrupted before reaching its maximum threshold level. The major reason for achieving this improved fault current interruption time is the compact topology of the proposed topology with less number of switches, consequently switches turn-on time decreases manifolds. Sec-

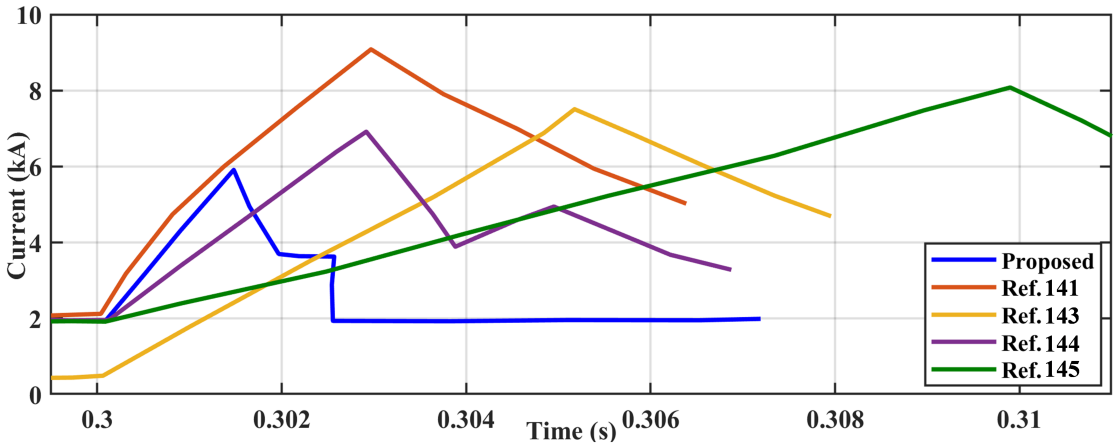


FIGURE 5.16: Comparative analysis of the proposed HMPDCCB fault current interruption time with the recent DC circuit breaker topologies present in the literature.

-ondly setting an appropriate threshold by selecting the current limiting inductor CLI's voltage as a decision maker to ascertain fault. Collectively these factors contribute to achieving shorter fault current interruption time and outperform the existing topologies on DC circuit breaker.

The study in [141] shown in orange solid line in Fig. 5.16 shows the fault current interruption time of 3ms, which is far greater in the case of HVDC. Because DC has less transmission line impedance, the fault current increases abruptly and can damage the entire system within milliseconds. The main reason for delayed interruption time is that their topology is comprised of various branches which include several switches which have different turn-on times. Secondly, the fault current is interrupted around 9kA, which is also a higher fault current in the case of DC. The researchers proposed topology in [143] of DC circuit breaker with fault current interruption time of 5ms and fault current is interrupted around 7.6KA as shown on yellow colour in Fig. 5.16. Their suggested topology has a main selector branch separately for each transmission line for the detection of fault leads to the complex control algorithm. Secondly, large surge arresters are installed to dissipate fault energy after the interruption of the main fault current as the concept of fault current regeneration is ignored leading to increased overall cost and the size of the circuit breaker.

In [145], fault current interruption time is improved to 3ms which is still greater. They proposed numerous series and parallel combinations of switches. Ultimately not only

size and the cost of the circuit breaker topology increase but after the interruption even, the fault current again started increasing as shown in the purple solid line in Fig. 5.16 which interrupted the second time around 5ms.

Lastly, the proposed fault current interruption time in [146] is 9.3ms, interrupting fault current around 8kA, and taking more time than other literature studies as shown in green solid line in Fig. 5.16. They suggest a modular topology structure with various multi-level branches, which leads to more switches, and complex control. Ultimately cost and size of the breaker are compromised.

Summarizing above, it can be concluded that fast fault current interruption is crucial in HVDC transmission although suggested studies have made improvements, there is still room for improvement to achieve quick fault interruption. Secondly, none of the above studies have explored the concept of fault current regeneration after the interruption. The goal is to safeguard the entire HVDC system from the potential consequences of fault.

5.5.4 Energy Discussion

This sub-section presents a graphical and critical analysis, emphasizing the superiority of the suggested HMPDCCB topology over traditional circuit breaker topologies.

5.5.4.1 Graphical Analysis

The suggested hybrid multi-port DC circuit breaker (HMPDCCB) is designed for a multi-terminal high-voltage DC network. Its port-2 has 250kV and 2kA voltage and current ratings during normal operation, as shown in Fig. 5.17. The analysis of this port is done because, after a fault, when the fault current starts rising, consequently port power will also increase.Thus, the normal power flowing through the MMC2 is 500MW before the time 0.3s. However, when the fault occurred at point 0.3s, the fault current and voltage across the breaker started increasing. As a result, power also starts increasing as it is the product of voltage and current. The power of port-2 reaches the

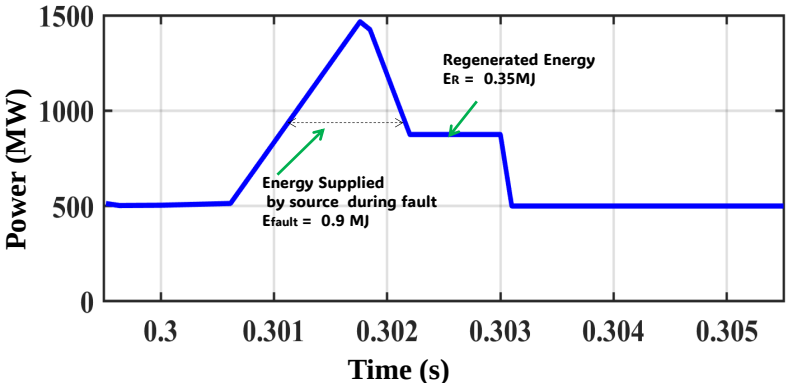


FIGURE 5.17: Power waveform of port-2 from normal operation to current breaking and regeneration operations.

maximum value of 1,490MW. Whereas, energy is the product of time and power. Thus, the source energy at this time is around 0.9MJ, this is the maximum energy until the current breaking. After the current breaks around 0.3018s, the current starts decreasing. As this port has a minimum voltage after the occurrence of a fault, thus this port is selected as the regenerated port. Thus after the interruption of the main fault current and fault current start decreasing at this time reuse/regeneration states begin. At 0.3022s, the breaker has reused the fault current of around 1.5kA so the new current flows through port-2 will be 3.5kA. Resultantly, the port-2 power flow including regeneration current will be 875MW and the energy of the port will be 0.35MJ. This energy could be used for future purposes from the suggested topology of the HMPDCCB. This highlights the severity of fault conditions and the need for a fast and efficient breaker topology.

Overall, the energy analysis reveals that the suggested HMPDCCB topology effectively handles high fault currents while minimizing energy losses, ensuring stability and reliability in power systems, particularly in high power level applications. This highlights its potential for various power system applications.

5.5.4.2 Critical Analysis of Energy

In traditional topologies, when the main current is interrupted, even after that a large number of surge arresters are installed in parallel to dissipate the remaining fault energy as heat to bring back the system to normal operation. This causes the breaker's size to increase in addition to raising its cost. However, the suggested topology, instead

of dissipating that energy in arch-quenching chambers or surge arresters. After the fault current interruption state, this topology of HMPDCCB provides a path through the IGBTs of the main breaker branch to save the cost, size, and energy losses of the breaker as depicted in Fig. 5.9. Energy could be calculated through *Joule Thomson* effect as $P_{loss} = i^2R$. The energy losses through the surge arresters are far greater than energy losses through the IGBTs of the main breaker branch. For instance, if we take the value of resistance from the datasheet of surge arrester model 3EL5 at current 2kA and voltage 2.5V is R=350Ω thus,

$$\begin{aligned} E_{\text{loss (MOV)}} &= \int_0^{t^+} P_{\text{loss}}\, dt, \\ &= \int_0^{t^+} (i'_{p(1)})^2 R\, dt, \\ &= \int_0^{t^+} (i'_{p(1)})^2 R_{\text{MOV}}\, dt, \\ &= \int_0^{t^+} (i'_{p(1)})^2 (350)\, dt, \\ &= 350 \int_0^{t^+} (i'_{p(1)})^2\, dt, \end{aligned} \tag{5.17}$$

$$E_{\text{loss (MOV)}} = 350k, \tag{5.18}$$

where, $k = \int_0^{t^+} (i'_{p(1)})^2\, dt$. However, the energy losses through the IGBT path can be calculated as,

$$\begin{aligned} E_{\text{loss (IGBT)}} &= \int_0^{t+} P_{\text{loss}} dt, \\ &= \int_0^{t^+} (i'_{p(1)})^2 R_{\text{CE}} dt, \\ &= \int_0^{t^+} (i'_{p(1)})^2 (0.00125) dt, \\ &= 0.00125 \int_0^{t^+} (i'_{p(1)})^2 dt, \end{aligned} \tag{5.19}$$

$$E_{\text{loss (IGBT)}} = 0.00125k. \tag{5.20}$$

If we take the value of resistance from the datasheet of IGBT model 5SNA3000K452300 at current 2kA and voltage 2.5V, that will be $R_{CE} = V/I$; thus, R_{CE} =0.00125. By

TABLE 5.2: Comparison of the hybrid multi-port DC circuit breaker (HMPDCCB) with existing circuit breakers in terms of interruption time, breaker reset/recovery time, and regeneration capability.

Circuit breaker	Interruption time	Breaker reset/recovery time	Regeneration
Proposed HMPDCCB	**<1.8ms**	**<3ms**	**Yes**
Xiao *et al.* [141]	<3ms	14ms	No
Zhang *et al.* [142]	<4ms	15ms	No
Shuo *et al.* [143]	<9.3ms	12ms	No
Liu *et al.* [144]	<5.9ms	11ms	No
Guibin *et al.* [145]	<3ms	6ms	No
Kaiming Li *et al.* [146]	<9.8ms	19ms	No

comparing 5.18 and 5.20, it can be inferred that power losses from surge arresters are greater than the path of IGBTs. Surge arresters exhibit higher resistance, 350Ω, while IGBTs only display a resistance of 0.00125Ω when the same current is passed through them. Consequently, the suggested breaker topology has an advantage over the circuit breaker topologies that were previously in use [141–146].

The proposed HMPDCCB topology offers potential for future energy regeneration, distinguishing it from existing circuit breaker literature.

5.5.5 Performance Comparison

The HMPDCCB, a hybrid multi-port DC circuit breaker, is compared to advanced circuit breakers based on performance indicators like current interruption speed, reset and recovery times, regeneration capabilities, physical size, and control complexity in Table 5.2.

5.5.5.1 Current Interruption Time

The hybrid multi-port DC circuit breaker (HMPDCCB) is a highly efficient solution for reducing system damage and enhancing power network reliability. It not only halts fault spread but also reduces stress on breaker components, extending the device's lifespan and reducing maintenance costs. The HMPDCCB achieves a fast current interruption time of less than 1.8 milliseconds, outperforming other circuit breakers by 55%, 80%, and 68%, in [144], [146] and [143] respectively, demonstrating its superior speed in interrupting fault currents.

5.5.5.2 Breaker Reset Time

A fast circuit breaker reset time is crucial in power systems to restore normal operations after faults are addressed, minimizing downtime, improving system reliability, and preventing defects from escalating into larger issues, thereby ensuring system stability. The HMPDCCB circuit breaker outperforms other circuit breakers in terms of reset times, with a remarkable 3 millisecond time, 69 times faster than the best reported time in [141], 70 times faster than those in [142], and significantly faster than breakers in [145] and [146]. The HMPDCCB, with its innovative topology and rapid reset capability, is an efficient and robust alternative to traditional circuit breakers for high-voltage DC power systems, reducing the risk of prolonged shutdowns and associated costs.

5.5.5.3 Regeneration Capability

The HMPDCCB is a unique circuit breaker design that offers energy regeneration capabilities, allowing for the recovery of stored energy after main fault current interruption, reducing energy loss and enhancing power system sustainability. Its short reset time improves system reliability, allowing it to handle subsequent faults quickly and minimize cascading failure risks. The HMPDCCB significantly enhances the amount of regenerated current and energy compared to the low-voltage DC topology of [150], suggesting its potential to improve the efficiency for high-voltage DC networks by capturing and reusing wasted energy. What truly sets the HMPDCCB apart, as detailed in Table 5.2, is its unique ability to recycle energy stored in passive components. This makes it exceptionally well-suited for HVDC systems, offering a powerful opportunity to boost both the efficiency and sustainability of modern power grids. By integrating energy regeneration into its design, the HMPDCCB circuit breaker not only provides superior fault protection but also contributes to a more eco-friendly and resource-efficient power infrastructure.

5.5.5.4 Size of the Breaker

The hybrid multi-port DC circuit breaker (HMPDCCB) addresses the issue of the phy-

-sical size of a circuit breaker by using a shared energy-dissipating branch across all terminals, thereby reducing its overall size and offering a more compact solution compared to other circuit breakers discussed in [141, 142, 146].

The HMPDCCB is a unique design that utilizes energy reuse instead of surge arresters after fault interruption. This feature not only reduces the need for surge arresters but also allows for energy recovery from passive elements, thereby reducing the breaker's size.

The HMPDCCB's compact design and energy recovery functionality enhance performance and fault-clearing times, making it an ideal choice for high-voltage direct current (HVDC) systems with space and cost constraints. Its ability to balance efficiency with a smaller footprint enhances its value for modern HVDC networks.

5.5.5.5 Control Complexity

The HMPDCCB topology simplifies control systems with fewer switches s compared to [141, 145, 146], resulting in lower complexity and cost savings. It enhances reliability and availability by reducing failure or malfunction chances, and reduces the number of circuit breaker components.

5.6 Chapter Summary

This chapter presents a novel hybrid multi-port HVDC circuit breaker (HMPDCCB) specifically engineered for n-terminal high-voltage direct current (HVDC) systems. This innovative circuit breaker uses a common breaker, energy dissipating and regenerating branch for all the connected lines. It also integrates Current Limiting Inductors (CLIs) with a hybrid DC circuit breaker (HDCCB), enabling it to effectively limit fault current instantaneously. These features are the key differentiator, setting the HMPDCCB apart from conventional circuit breakers. The HMPDCCB distinguishes itself through several notable results. Firstly, it significantly reduces both the current interruption time to 1.8ms and the reset/recovery time to 3ms. Secondly, it offers selective protection of all

the connected DC lines. Thirdly, it incorporates a regeneration capability, which is not typically found in standard circuit breakers. This allows for more efficient energy management, as it reuses energy that would otherwise be dissipated. Fourthly, when compared to other circuit breakers, the HMPDCCB offers substantial cost savings, making it a more economically viable option for modern HVDC systems. Another critical advantage of the HMPDCCB is its suitability for high-voltage DC systems with multiple terminals (MTDC). Its rapid current interruption and quick breaker reset/recovery times are particularly beneficial for these complex systems, ensuring reliability and stability under fault conditions. Furthermore, the HMPDCCB's compact structure and simplified control mechanism enhance its compatibility with MTDC system applications, making it an ideal solution for the evolving demands of advanced power systems. The study investigates a hybrid multi-port DC circuit breaker and its equivalent circuits, offering a comprehensive simulation result, and suggesting future research should focus on prototype development.

Chapter 6

Thesis Summary

6.1 Discussion

This research aims to improve the performance and reliability of high-voltage direct current (HVDC) circuit breakers (DCCBs) by addressing issues like large fault energy dissipation, longer fault current interruption time, and delayed breaker reset time in multi-terminal direct current systems. It begins with a comprehensive literature review, analyzing existing topologies, particularly hybrid DCCBs, to identify gaps and formulate a problem statement, thereby enhancing the reliability of DCCBs.

The research proposes two hybrid DCCB topologies to address large fault energy dissipation in MTDC systems: modular hybrid DCCB with fault current self-adaptive control and protective coordination (MHDCCB) and improved hybrid DCCB with battery banks for energy storage (HDCCB). The MHDCCB features a two-stage current limiting mechanism that extends the current limiting duration and adapts to primary and backup protection. The improved HDCCB topology uses a resistor-inductor-capacitor resonance to create current zero-crossings and store inductive energy from network faults in battery banks for future use. Both topologies integrate battery banks to store the breaker's energy during fault events. However, the major setback is increased system cost due to occasional faults and battery degradation or underutilization.A novel regenerative hybrid high-voltage direct current circuit breaker (HDCCB) topology is proposed

to address the limitations of installing battery banks for breakers' energy storage after interruption. This topology introduces fault current regeneration, regenerating fault energy during fault occurrences and sending it back to the grid for future use. It minimizes fault current interruption and breaker reset time, allowing fault interruptions under 2ms and restoration to normal operation within 5ms. The topology features a current-limiting branch to reduce peak fault currents and a compact topology with reduced component count, simplifying control schemes and improving integration with HVDC systems. The regeneration feature enables the recovery and reuse of 1.5MJ of fault energy, surpassing the traditional topology's 17.07kJ.

One of the primary objectives of this work is to minimize fault interruption time. Given the low impedance of HVDC transmission lines, significant fault currents can arise, making swift interruption crucial to prevent cascading failures. The proposed designs aim to address these challenges by rapidly interrupting fault currents, thereby safeguarding system integrity.

A novel hybrid multi-port direct current circuit breaker (HMPDCCB) topology is proposed for protecting multiple transmission lines using a single HMPDCCB. This design reduces the breaker's size and cost by using a common main breaker branch for all lines during fault events. The breaker efficiently protects HVDC systems by reducing current interruption time to under 1.8ms and resetting within 3ms. It also incorporates a fault current regeneration feature, retrieving 0.35MJ of energy, and uses current-limiting inductors to prevent sudden surges. The simplified controller monitors the voltage across CLIs to identify fault lines, selecting the port with the minimum voltage as the receiving port for regenerated energy.

The research highlights the need to reduce the size of direct current circuit breakers (DCCBs) in high-voltage direct current (HVDC) systems. The regenerative hybrid high-voltage direct current breaker (HDCCB) and hybrid multi-port direct current circuit breaker (HMPDCCB) are proposed topologies that enhance size, performance, and cost-effectiveness. The HDCCB uses energy regeneration to recover stored energy from the inductor, eliminating the need for bulky battery banks or surge arresters. The HMPDCCB uses a shared energy-dissipating branch, simplifying the design and improving system performance. Both topologies represent significant advancements in

HVDC breaker technology, addressing size and complexity challenges and paving the way for more robust and efficient HVDC systems.

Both proposed topologies represent significant advancements in HVDC breaker technology. Their capacity to deliver effective fault management while addressing size and complexity challenges positions them as suitable candidates for modern high-voltage direct current applications. As the demand for efficient and reliable power systems continues to grow, the contributions of this research lay the groundwork for future innovations and improvements in DCCB design and operation, paving the way for more robust and efficient HVDC systems.

In summary, this research presents significant advancements in hybrid direct current circuit breaker (DCCB) technology, particularly in the regeneration of fault current energy and rapid fault interruption. The development of novel DCCB topologies addresses critical challenges in multi-terminal HVDC systems, offering enhanced efficiency and reliability. Key innovations include designs that effectively manage fault energy dissipation, achieve faster interruption and reset times, and reduce the overall size and complexity of the systems. By minimizing components and costs while improving performance, these topologies represent a substantial step forward in HVDC breaker technology, making them well-suited for contemporary applications.

6.2 Research Output

The main research outputs are stated as follows:

- One of the key achievements of this research is the development of a novel hybrid direct current circuit breaker (DCCB) topologies that effectively regenerate fault current energy and return it to the grid, addressing the challenge of large fault energy dissipation in multi-terminal HVDC (MTDC) systems. Two hybrid DCCB topologies were initially proposed: the modular hybrid DCCB with fault current self-adaptive control and protective coordination (MHDCCB) and an improved hybrid DCCB (HDCCB) with integrated battery banks for energy storage. However,

the use of battery banks led to increased system costs and battery degradation or underutilization. Two further topologies were developed, a regenerated hybrid DCCB and a hybrid multi-port DCCB, which successfully regenerated 1.5MJ and 0.35MJ of energy, respectively.

- Another output of this research is the development of two novel topologies of DCCB for faster fault current interruption. The first topology, the regenerative HDCCB, achieves a primary fault current interruption time of less than 2ms, which is considerably faster compared to other well-known circuit breakers. It interrupts fault currents 50% faster than the design in [123], and 80% faster than that in [124]. This rapid interruption time prevents fault propagation, reduces stress on expensive components, and lowers maintenance costs. The second topology, the hybrid multi-port DCCB, achieves an even faster interruption time of less than 1.8ms, 55% faster than the breaker in [144], 80% faster than [146], and 68% faster than [143]. This research marks a significant breakthrough in fault current management and regenerative circuit breaker design for HVDC systems.

- The proposed topologies offer significantly reduced reset times, enhancing system reliability and stability. The first topology, a regenerative hybrid HVDC circuit breaker (HDCCB), achieves a short reset time of just 5ms, four times faster than cited in [130], and twenty-five times faster than the latest reset time reported in [131]. This faster reset time allows the system to quickly restore normal operation after a fault, handle subsequent faults, and reduce the risk of cascading failures. The second topology, a hybrid multi-port direct current circuit breaker (HMPD-CCB), offers an even faster reset time of 3ms, 69 times faster than in [141] and 70 times faster than those in [142]. This rapid reset time further enhances system recovery, reducing downtime, potential damages, and associated costs from extended system shutdowns.

- This research focuses on reducing the size of the DCCB to address space and cost constraints in high-voltage direct current systems. The first topology, a regenerative hybrid HDCCB, uses energy regeneration to recover stored energy in the inductor of the current-limiting branch instead of installing battery banks or using a surge arrester even after interruption of fault, reducing the breaker's size

and improving fault-clearing time. This compact design is ideal for HVDC applications. The second topology, a hybrid multi-port direct current circuit breaker (HMPDCCB), uses a shared energy-dissipating branch for all terminals, reducing the need for surge arresters and improving performance. Both topologies offer compact and cost-effective solutions for HVDC power systems.

- This research focuses on simplifying control systems by using fewer components, reducing complexity, improving reliability, and lowering costs. The first topology, a regenerative HDCCB, employs fewer components than previous topologies in [122, 131], reducing size and control complexity. This topology enhances system reliability and availability by minimizing the number of switches. The second topology, HMPDCCB, also reduces control complexity by utilizing fewer switches, reducing the risk of failure and improving system reliability. The simpler design offers significant cost savings by minimizing the number of circuit breaker components and potential maintenance requirements as compared to the more component-heavy systems in [141, 145, 146]. Both topologies contribute significantly to the advancement of HVDC breaker technology, making them suitable for modern high-voltage direct current applications.

In summary, this research demonstrates five key achievements in developing DCCB topologies for multi-terminal direct current transmission systems. These include energy regeneration, faster fault current interruption, reduced reset times, compact design, and simplified control systems.

6.3 Limitations

This research has limitations, including a focus on simulation-based validation, which is primarily used to evaluate the performance of the proposed topologies, for instance, the hybrid multi-port direct current circuit breaker (HMPDCCB) and the regenerative hybrid high-voltage direct current circuit breaker (HDCCB). This lack of physical validation, such as real-world deployment or hardware testing, could potentially introduce

challenges or may be deviations from the simulated outcomes in industrial HVDC systems. Thus, prototype development is the major limitation of the proposed work. It was basically due to the high cost of components and financial constraints in underdeveloped countries. This lack of experimental testing is a critical gap in understanding the practical performance, reliability, and robustness of the proposed topologies. Simulations cannot fully replicate complex, unpredictable behaviors in actual HVDC systems, and physical testing could reveal additional challenges related to control schemes and integration with existing systems. Future research could benefit from funding to acquire HVDC components for physical testing, confirming theoretical findings and providing reliable data for practical industrial applications.

Another limitation of this research is the large voltage stresses experienced by insulated gate bipolar transistors (IGBTs) during fault energy dissipation. These high voltage stresses could pose significant risks if not managed properly, especially during high-speed switching operations required in HVDC fault conditions. The compact topology of the breaker design places more reliance on IGBTs for critical switching functions, which could compromise the breaker's reliability and operational lifespan. The simulation models used in the research assume ideal conditions for IGBT performance. The simplified control scheme may lack the sophistication needed to respond to real-time voltage surges during fault conditions. Future work should focus on developing robust mitigation strategies and real-world testing to fully realize the benefits of these designs in industrial HVDC systems.

The HMPDCCB and regenerative HDCCB topologies have introduced fault current interruption times of 1.8ms and 2ms, respectively, but they may still be insufficient for HVDC systems due to the rapid rise in fault currents due to low line impedance. Multi-terminal HVDC systems, where multiple transmission lines are interconnected, make the situation more complex. The ability to handle multi-terminal faults is crucial for HVDC grids, as these systems connect renewable energy sources across wide geographic areas. The existing design relies on current-limiting inductors to manage fault current surges, but further optimization is needed to reduce fault interruption times and ensure the breaker can cope with the dynamic nature of fault currents in multi-terminal HVDC systems. Addressing this limitation would enhance the practical application of these

topologies in real-world HVDC grids, ensuring greater protection and reliability for modern power systems.

Another key limitation of this study is the lack of a detailed cost analysis for the proposed breaker topologies, which is crucial for evaluating their economic feasibility in HVDC applications. While the HMPDCCB and regenerative HDCCB topologies demonstrate fault current regeneration, their overall efficiency and cost-effectiveness remain uncertain without a comprehensive financial evaluation. The 1.5MJ regenerative capacity of HDCCB represents only a fraction of total fault energy, potentially limiting its suitability for large-scale HVDC systems. The proposed Hybrid HVDC Circuit Breaker, with fewer branches and components, suggests a cost advantage, but its financial viability remains uncertain without a thorough economic assessment. Factors such as manufacturing costs, material expenses, and operational reliability must be analyzed to validate the practical benefits. While this study provides valuable insights into fault current interruption and regeneration, a detailed cost-benefit analysis is a limitation for quantifying the economic impact and real-world applicability of the proposed designs.

The proposed study has not explicitly calculated the losses associated with the regeneration process, which is acknowledged as a limitation of this work. To simplify the analysis, ideal assumptions were considered regarding voltage drop, switching losses, and other potential energy dissipation factors. While this approach facilitates a clearer theoretical evaluation of the proposed topologies, it does not fully account for the inherent losses present in practical HVDC systems. In real-world applications, factors such as conduction losses in power electronic devices, transient switching losses, and control inefficiencies can influence the overall efficiency of the regenerative process. The absence of a detailed loss calculation introduces a level of uncertainty in assessing the precise energy recovery performance of the breaker. The absence of a detailed loss calculation introduces a level of uncertainty in assessing the precise energy recovery performance of the breaker. The absence of a detailed loss calculation introduces a level of uncertainty in assessing the precise energy recovery performance of the breaker. Although the study provides valuable insights into the fault current interruption and regeneration capabilities, incorporating a comprehensive loss analysis would enhance the accuracy of performance evaluation in industrial HVDC environments.

6.4 Conclusions

This research focuses on the issue of large fault energy dissipation in multi-terminal direct current (MTDC) systems, which significantly impacts the reliability and efficiency of high-voltage direct current (HVDC) networks. Two novel hybrid direct current circuit breaker (DCCB) topologies are introduced: the modular hybrid DCCB with fault current self-adaptive control (MHDCCB) and the improved hybrid DCCB (HDCCB) featuring integrated battery banks for energy storage. The MHDCCB employs a two-stage current limiting mechanism for robust fault management, while the improved HDCCB uses a resistor-inductor-capacitor resonance technique to create current zero-crossings for energy storage during faults. However, these initial designs revealed limitations such as increased system costs and battery degradation.

In response to these challenges, further research led to the development of a regenerative hybrid DCCB (HDCCB) that introduces fault current regeneration, allowing for the reuse of fault energy by sending it back to the grid. This innovative approach achieves rapid fault interruptions of under 2ms and restoration to normal operation within 5ms. Notably, this topology recovers 1.5MJ of fault energy, marking a significant improvement over traditional systems.

The research culminates in the introduction of the hybrid multi-port DCCB (HMPDCCB) topology, which offers efficient protection for multiple transmission lines using a single circuit breaker. This design not only reduces current interruption time to under 1.8ms and reset time to 3ms but also incorporates a fault current regeneration feature that retrieves 0.35MJ of energy. By utilizing common components, the HMPDCCB achieves a more compact and cost-effective solution while enhancing system efficiency and reliability.

Overall, the methodologies employed in this research, using advanced simulation techniques, performance evaluations, and innovative design strategies, showcase significant advancements in HVDC circuit breaker technology. It provides a framework for future fault management and energy efficiency, contributing to the evolution of sustainable and resilient electrical infrastructures in the rapidly changing energy landscape.

6.5 Future Work

The future work in this research focuses on several key areas to further validate and optimize the hybrid high-voltage direct current circuit breaker (HDCCB) and hybrid multi-port DC circuit breaker (HMPDCCB) designs in real-world HVDC systems. Key areas include prototype development, economic feasibility analysis, and energy storage optimization. These areas will translate theoretical and simulated successes into practical, commercially viable solutions for modern HVDC infrastructure.

- The proposed HDCCB and HMPDCCB designs have been tested using MATLAB's Simulink®/Simpowersystems, but the next step is to build physical prototypes to validate their performance in real-world conditions. This involves constructing scaled-down versions of breakers in a controlled environment. The prototype development process includes selecting components like IGBTs, thyristors, and CLIs to ensure practical implementation. Key parameters to be tested include fault current interruption times, breaker reset/recovery times, and energy regeneration efficiency. Real-world testing will provide valuable insights into the actual performance of the designs under different fault conditions.

- Future research should focus on managing voltage stresses on IGBTs during fault energy dissipation in proposed circuit breaker designs. These high-voltage stresses pose risks, especially during high-speed switching operations under HVDC fault conditions. The compact design of the breakers increases reliance on IGBTs for critical switching functions, potentially jeopardizing system reliability and operational lifespan. To enhance the designs' robustness, researchers should develop effective mitigation strategies and conduct real-world testing to evaluate performance under actual fault conditions. This will ensure the proposed topologies are theoretically sound, practical, and reliable for industrial HVDC applications.

- This research presents designs for HDCCB and HMPDCCB, which offer significant performance improvements. However, a detailed economic assessment is needed to evaluate their commercial viability in real-world HVDC applications. A cost-benefit analysis should compare the overall investment, maintenance, and

operating costs of these breakers with existing solutions, considering component costs, energy dissipation savings, increased system up-time, and reduced downtime due to faster fault clearance times. The economic assessment should also consider scalability, as larger HVDC grids may require additional investments in breaker capacity, energy storage systems, and protection schemes. Comparing the designs with alternative technologies like solid-state circuit breakers will help determine if the HDCCB and HMPDCCB offer a more cost-effective long-term solution.

- The HDCCB and HMPDCCB designs have the potential to regenerate fault energy, improving the sustainability and efficiency of HVDC systems. However, energy storage systems must be optimized to handle large fault events and varying conditions. Future work should focus on selecting and testing efficient, scalable, and cost-effective energy storage technologies for HVDC applications, including exploring battery chemistries and super-capacitors. Optimizing charging and discharging rates for fast fault response and maintaining system reliability may require the development of advanced control algorithms that can predict fault energy levels and manage storage systems in real-time. Assessing energy conversion efficiency from fault energy capture to grid reintegration is also necessary, involving rigorous testing of power electronics and integration with advanced real-time monitoring systems.

- Future research should focus on optimizing fault current interruption times of HMPDCCB and regenerative HDCCB, which currently have 1.8ms and 2ms respectively. These times may be insufficient in HVDC systems due to the rapid rise in fault currents due to low line impedance. Multi-terminal HVDC systems, often linking renewable energy sources across large geographic areas, require effective fault management capabilities. The current design employs current-limiting inductors to mitigate fault current surges, but additional optimization is needed to reduce interruption times and enable breakers to adapt to dynamic fault currents. Addressing these limitations is crucial for improving the practical applicability of circuit breaker topologies in real-world HVDC grids.

- The proposed HMPDCCB and regenerative HDCCB topologies currently offer

fault current regeneration capabilities but their regenerative capacity is only a small fraction of the total fault energy, especially in large-scale HVDC systems. This gap in practical application is particularly significant in expansive HVDC grids with complex fault conditions and higher fault energy surges. The economic viability of these regenerative features is also crucial, as current uncertainties may stem from design inefficiencies or control mechanisms. Future efforts should focus on optimizing these topologies' regenerative capabilities, exploring advanced design modifications, control strategies, and cost-benefit analyses to better align these technologies with large-scale HVDC system demands.

- The study suggests that future research should consider additional fault types beyond line-to-ground faults, such as bus faults, line-to-line faults, and source faults, to ensure the robustness of the proposed circuit breaker topologies. This will provide deeper insights into the circuit breaker's response under diverse fault scenarios, enabling a more comprehensive validation of its effectiveness. This will also enhance the breaker's adaptability in complex HVDC grids, particularly in multi-terminal configurations where fault characteristics can vary significantly. Incorporating these fault types in future studies will contribute to the practical deployment and reliability of the proposed topologies in real-world HVDC applications.

Concluding above, future work should focus on prototype development, economic feasibility, energy storage optimization, and fault current interruption enhancements to refine the proposed HDCCB and HMPDCCB designs. Additionally, broader fault analyses, including bus, line-to-line, and source faults, are essential for ensuring the robustness and practicality of these circuit breakers in complex HVDC grids. These advancements will contribute to the reliable and efficient deployment of the proposed topologies in real-world applications.

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