CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY, ISLAMABAD

Harmonics Mitigation using Shunt Active Power Filter Based on Modified Synchronous Reference Frame Theory

by

Ikramullah

A thesis submitted in partial fulfillment for the degree of Doctor of Philosophy

in the

Faculty of Engineering
Department of Electrical Engineering

2020

Harmonics Mitigation using Shunt Active Power Filter Based on Modified Synchronous Reference Frame Theory

By

Ikramullah

(DEE 151006)

Dr. Adrian Traian Plesca, Professor

Gheorghe Asachi Technical University of lasi, Romania

(Foreign Evaluator 1)

Dr. Arfakhshand Ali Qazalbash

Fiat Chrysler Automobiles, USA

(Foreign Evaluator 2)

Dr. Muhammad Ashraf

(Thesis Supervisor)

Dr. Noor Muhammad Khan

(Head, Department of Electrical Engineering)

Dr. Imtiaz Ahmed Taj

(Dean, Faculty of Engineering)

DEPARTMENT OF ELECTRICAL ENGINEERING

CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

ISLAMABAD

2020

Dedicated to my parents

CAPITAL UNIVERSITY OF SCIENCE & TECHNOLOGY
ISLAMABAD

Expressway, Kahuta Road, Zone-V, Islamabad
Phone:+92-51-111-555-666 Fax: +92-51-4486705
Email: info@cust.edu.pk Website: https://www.cust.edu.pk

CERTIFICATE OF APPROVAL

This is to certify that the research work presented in the thesis, entitled "**Harmonics Mitigation using Shunt Active Power Filter based on Modified Synchronous Reference Frame Theory**" was conducted under the supervision of **Dr. Muhammad Ashraf**. No part of this thesis has been submitted anywhere else for any other degree. This thesis is submitted to the **Department of Electrical Engineering, Capital University of Science and Technology** in partial fulfillment of the requirements for the degree of Doctor in Philosophy in the field of **Electrical Engineering.** The open defence of the thesis was conducted on **August 20, 2020.**

Student Name : Ikram Ullah (DEE151006)

The Examination Committee unanimously agrees to award PhD degree in the mentioned field.

Examination Committee :

(a) External Examiner 1: Dr. Muhammad Ahmad Chaudhary
Professor
UET Taxila

(b) External Examiner 2: Dr. Shaikh Saaqib Haroon
Associate Professor
UET Taxila

(c) Internal Examiner : Dr. Umer Amir Khan
Assistant Professor
CUST, Islamabad

Supervisor Name : Dr. Muhammad Ashraf
Professor
CUST, Islamabad

Name of HoD : Dr. Noor Muhammad Khan
Professor
CUST, Islamabad

Name of Dean : Dr. Imtiaz Ahmed Taj
Professor
CUST, Islamabad

AUTHOR'S DECLARATION

I, **Ikram Ullah (Registration No. DEE151006)**, hereby state that my PhD thesis titled, '**Harmonics Mitigation using Shunt Active Power Filter based on Modified Synchronous Reference Frame Theory**' is my own work and has not been submitted previously by me for taking any degree from Capital University of Science and Technology, Islamabad or anywhere else in the country/ world.

At any time, if my statement is found to be incorrect even after my graduation, the University has the right to withdraw my PhD Degree.

(**Ikram Ullah**)

Dated: 20 August, 2020

Registration No : DEE151006

PLAGIARISM UNDERTAKING

I solemnly declare that research work presented in the thesis titled "**Harmonics Mitigation using Shunt Active Power Filter based on Modified Synchronous Reference Frame Theory**" is solely my research work with no significant contribution from any other person. Small contribution/ help wherever taken has been duly acknowledged and that complete thesis has been written by me.

I understand the zero tolerance policy of the HEC and Capital University of Science and Technology towards plagiarism. Therefore, I as an author of the above titled thesis declare that no portion of my thesis has been plagiarized and any material used as reference is properly referred/ cited.

I undertake that if I am found guilty of any formal plagiarism in the above titled thesis even after award of PhD Degree, the University reserves the right to withdraw/ revoke my PhD degree and that HEC and the University have the right to publish my name on the HEC/ University Website on which names of students are placed who submitted plagiarized thesis.

(**Ikram Ullah**)

Dated: 20 August, 2020

Registration No : DEE151006

List of Publications

It is certified that following publication(s) have been made out of the research work that has been carried out for this thesis:-

Journal Publications

1. **Ikramullah**, M. Ashraf, "Comparison of Synchronization Techniques under Distorted Grid Conditions," *IEEE ACCESS*, vol. 7, pp. 101345-101354, 2019.

2. **Ikramullah**, M. Ashraf, "Sliding mode control for performance improvement of shunt active power filter," *SN Applied Sciences*, vol. 1, pp. 531-540, 2019.

Conference Publications

1. **Ikramullah**, M. Ashraf, Abdur Rehman, "Performance Analysis of Current Injection Techniques for Shunt Active Power Filter," *IOP Conference Series: Earth and Environmental Science*, vol. 168, pp. 012014, 2018.

2. **Ikramullah**, M. Ashraf, Abdur Rehman, "Comparison of Reference Current Generation Techniques for Shunt Active Power Filter," *2018 5th International Conference on Electrical and Electronic Engineering* , vol. 5, pp. 62-66, 2018.

Ikramullah
(DEE 151006)

Acknowledgements

I am honored with the opportunity to undertake such a challenging but rewarding research. It is indeed a satisfying experience to pursue this research. I extend my profound thanks to my family, friends, colleagues and supervisor for their constant support. I sincerely thank my supervisor, Dr. Muhammad Ashraf, for his constant guidance and encouragement throughout my research work. I am immensely grateful for all the time that he has dedicated for discussions on my work. I also thank Mr. Yasine Terriche, Alborg University, Denmark for his great support in my research. I thank my family for their unconditional love, support and prayers. This research could not have been completed without them. I would like to thank Almighty Allah for providing me with wisdom and help from all the people listed above, and many others who have been a great support in many ways.

Abstract

The dependency on electrical energy is being increased rapidly with the advancement of technology. The use of smart appliances has also increased to save the electrical energy. The power electronic converters and non-linear loads are also the sources of harmonics and reactive power which, greatly reduces the power quality. Therefore, proper methods are required for mitigation of current harmonics which will enhance the reliability of grid-connected systems.

Many techniques have been used by researchers for mitigation of harmonics but, the most common method is the active power filtering due to its excellent performance in reducing harmonic distortion. This research is focused on shunt active power filter used for mitigation of current harmonics. The SAPF is consisting of two main parts which are reference current generation and injection of current at the point of common coupling. Many control strategies have been developed for reference current generation like instantaneous reactive power theory, synchronous reference frame theory and discrete fourier transform. Similarly many techniques are being used for current injection but hysteresis current control is most widely used. These techniques have been hardly evaluated under adverse grid conditions. The aim of this thesis is to develop a control strategy that works under all types of grid disturbances.

Synchronization of active power filter with the grid voltage is very important under the effects of frequency drift, phase angle variation and presence of dc offset. Existing phase locked loop techniques like synchronous reference frame PLL, moving average filter PLL and cascaded delayed signal cancellation PLL have been investigated for estimation of frequency and phase under adverse grid conditions. Cascaded delayed signal cancellation technique is shown to have best performance in terms of dynamic response and filtering capability. This identified technique is being applied to synchronize the active power filter with the grid using synchronous reference frame theory.

This thesis contributes by developing a modified reference current generation technique that employs cascaded delayed cancelation PLL instead of the conventional

synchronous reference frame PLL to estimate frequency and phase of the grid voltage. Furthermore, sliding mode control strategy has been developed to inject the reference current accurately at the point of common coupling. The proposed strategy is tested under various grid disturbances and results are compared with the instantaneous reactive power theory which does not require frequency and phase information. Matlab/Simulink environment is used to evaluate the performance of shunt active power filter. The performance of the conventional control strategy of shunt active power filter is being investigated under normal grid conditions and found satisfactory but under distorted grid conditions such as presence of frequency drift, phase angle variation and dc offset, it is not able to reduce harmonics distortion within limits of IEEE-519 standard. On the other hand a control strategy is proposed that is able to show excellent performance under both normal and adverse grid conditions. The total harmonic distortion of the compensated source current in each test case of grid disturbances does not exceed the standard limit. The proposed topology enhances the harmonic compensation capability and robustness compared with the conventional APF topologies in grid-connected systems.

Contents

List of Figures

List of Tables

Abbreviations

3P3W	Three Phase Three Wire System
ANN	Artificial Neural Network
APF	Active Power Filter
ASD	Adjustable Speed Drive
CDSC	Cascaded Delayed Signal Cancellation
CSI	Current Source Inverter
DBHCC	Double Band Hysteresis Curent Control
DFT	Discrete Fourier Transform
DG	Distributed Generation
DSC	Delayed Signal Cancellation
EP	Equilibrium point
GTFDSC	Generalized Trigonometric Function
HCC	Hysteresis Current Control
HCR	Harmonics Compensation Ratio
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IRP	Instantaneous Reactive Power
LPF	Low Pass Filter
OCC	One Cycle Control
PCC	Point of Common Coupling
PFC	Power Factor Correction
PHC	Perfect Harmonic Cancellation
PLL	Phase Locked Loop
PSO	Particle Swarm Optimization

PV	Photovoltaic
SAPF	Shunt Active Power Filter
SBHCC	Single Band Hysteresis Curent Control
SMC	Sliding Mode Control
SPWM	Sinusoidal Pulse Width Modulation
SRF	Synchronous Reference Frame
THD	Total Harmonic Distortion
THD$_i$	Total Harmonic Distortion of Current
THD$_v$	Total Harmonic Distortion of Voltage
UPS	Uninterupted Power Supply
UPF	Unity Power Factor
VCO	Voltage Controlled Oscilator
VLLMS	Variable Leaky Least Mean Square
VSD	Variable Speed Drives
VSI	Voltage Source Inverter

Symbols

C_{dc}	DC Link Capacitor
C_L	Load Capacitor
E_r	Error in DC link voltage
i_L	Load Current
i_s	Source Current
i_c	Compensating Current
i_c*	Reference Current
i_{dref}	d component of reference current
i_{qref}	q component of reference current
K_i	Integral Gain
K_p	Proportional Gain
P	Active Power
$p.u$	per unit
Q	Reactive Power
R_L	Load Resistor
rms	Root Mean Square
T_{on}	On time of hysteresis band
T_{off}	Off time of hysteresis band
T_{s1}	Time period of hysteresis band
U_{eq}	Equivalent control
U_n	Continous control
u_H	Micro Henry
u_f	Micro Farad

V_{dc}	DC Link Capacitor Voltage
$V_{dc}ref$	Reference DC Link Capacitor Voltage
V_{ih}^{+}	Amplitude of positive interharmonic component
V_{ih}^{-}	Amplitude of negative interharmonic component
V_{sa}	Source Voltage Phase A
V_{sb}	Source Voltage Phase B
V_{sc}	Source Voltage Phase C
ω	Angular Speed
θ	Phase Angle
ϕ_{vh}	Phase of harmonic voltage
ϕ_{ih}	Phase of harmonic current

Chapter 1

Introduction

Power quality improvement has gained a lot of importance in recent times. Power quality is defined as, "A set of electrical boundaries that makes proper functioning of equipment without any failure or performance degradation"[1]. The efficiency and lifespan of power-driven appliances is dependent on the voltage, current and frequency applied to them. There are many aspects that are accountable for lowering the power quality. This chapter begins by discussing briefly the power quality problems that occur frequently. Harmonics issue has been addressed in detail along with its mitigation techniques. The working of different blocks of SAPF is explained. The parameters used for performance evaluation of SAPF are also briefly discussed. Finally, objectives and motivation of the research are presented.

1.1 Power Quality Problems

The performance of different electric apparatus is directly affected by bad power quality. Whenever the voltage waveform of the power source is distorted, or the amplitude deviates from a set reference level, power quality is degraded [2]. Voltage fluctuations, voltage sags, voltage unbalance, transients and harmonics are some

of the common problems causing poor power quality [3, 4]. A brief description of different power quality problems is given here:

1.1.1 Voltage Sag

Voltage sag means a drop in voltage amplitude from 10-90 % of rms voltage for a time interval of 10 ms to 1 minute as shown in Fig. 1.1. The most common reasons of voltage sag include power-on of heavy induction motors, short circuits in other branches of the supply system and defective wiring. Some of the drawbacks include malfunction of electronic equipment, decrease in efficiency of rotating machines and tripping of circuit breakers. [5].

FIGURE 1.1: Voltage Sag

1.1.2 Voltage Spike

A quick deviation in voltage value within a number of microseconds to few milliseconds is known as voltage spike and is shown in Fig. 1.2. The main causes of voltage spike are lightning, PFC capacitors and detachment of heavy loads. Voltage spikes results in malfunctioning of the electronic components, errors in data processing and electromagnetic interference [6].

FIGURE 1.2: Voltage Spike

1.1.3 Voltage Swell

An increase in voltage beyond the range for a small duration of 20 ms to few seconds at the grid frquency is known as voltage swell. It occurs due to connection/disconnection of heavy loads, abrupt changes in load and damaged or loose neutral connection. The drawbacks of voltage swell are light flickering, data loss and damage of sensitive equipment [7]. A voltage swell is shown in Fig. 1.3

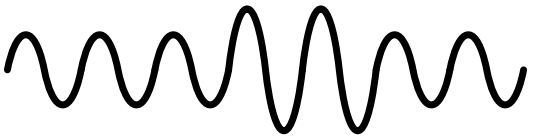

FIGURE 1.3: Voltage Swell

1.1.4 Harmonic Distortion

Harmonics are the integral multiples of fundamental frequency. Their main cause is the presence of non-linear loads. The main disadvantages include maximum chance in existence of resonance, overload in neutral conductors, overheating of cables and equipment, disturbances in the communication network, overheating of transformers, errors of measuring instruments and tripping of circuit breakers [8]. Fig. 1.4 shows a harmonically distorted wave.

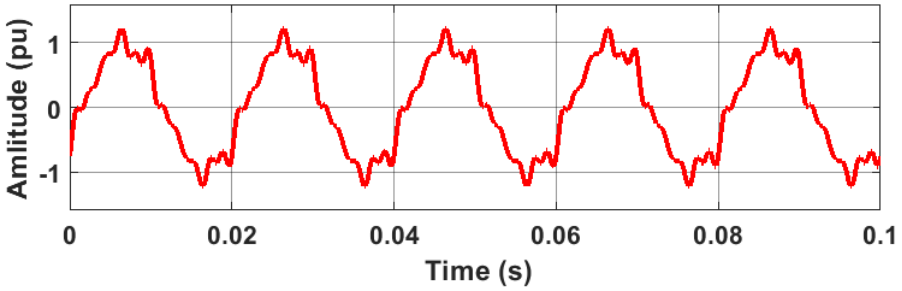

FIGURE 1.4: Harmonic Distortion

1.1.5 Voltage Fluctuations

They are defined as random variations of voltage amplitude due to sudden changes in load [9]. The examples of loads that may cause voltage fluctuations are arc furnaces, air conditioners, rolling mills and arc welders. Voltage fluctuations may produce flicker in lighting. Fig. 1.5 shows a fluctuation in voltage.

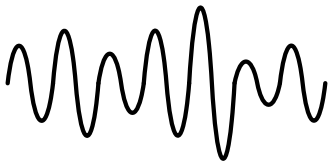

FIGURE 1.5: Voltage Fluctuations

1.1.6 Noise

Any external and unwanted information that interferes with the transmission signal is known as noise. Noise is not a part of the original signal. It is caused by electromagnetic interference, radio frequency interference and ignition systems. The negative effects of noise include troubles of sensitive electronic equipment, loss of data and errors in data processing [10]. Fig. 1.6 shows a noisy signal.

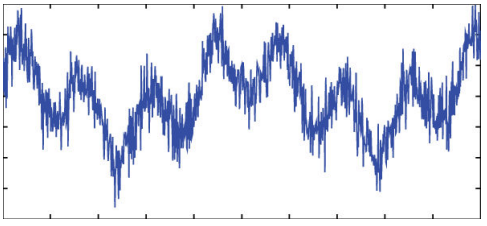

FIGURE 1.6: Noise

1.1.7 Voltage Unbalance

Voltage unbalance happens when the magnitude of the three phase voltages is not equal along with unequal phase difference between them. The large single-phase loads and improper load sharing in three phase systems can cause voltage

unbalance. Negative sequence is present due to the unbalanced system which is dangerous for all three phase loads especially three-phase induction machines [11]. A volage unbalance is shown in Fig. 1.7.

In the following section effects of harmonics on the grid supply, causes of harmonics and the techniques used for its mitigation are discussed.

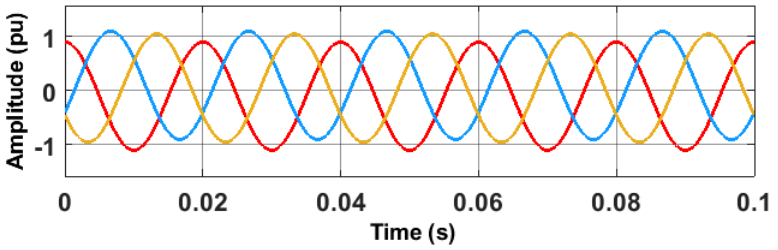

FIGURE 1.7: Voltage Unbalance

1.2 Harmonics

Harmonics is considered as the major issue out of all power quality problems [12]. Recently mitigation of harmonics has gain a lot of attention due to the increased use of non-linear loads.

1.2.1 Harmonics Definition

The term harmonic is known as component of a waveform that occurs at an integer multiple of the fundamental frequency. The presence of harmonics in electrical systems means that current and voltage are distorted and deviate from sinusoidal waveforms [13]. If the fundamental frequency of an alternating current (AC) signal is represented by f then the harmonic frequencies like second harmonic and third harmonic will be represented by 2f, 3f and so on. The fundamental frequency is the frequency at which most of the energy is contained or at which the signal is defined to occur.

Almost all signals have energy at harmonic frequencies, in addition to the energy

at the fundamental frequency. The signal will be a perfect sine wave if all the energy in it is contained at the fundamental frequency. On the other hand the presence of harmonics makes the sine wave distorted. Examples of some largely distorted waveforms are square waves, sawtooth waves, and triangular waves.

1.2.2 Mathematical Description

A distorted voltage waveform can be represented as a sum of fundamental component V_1 and harmonic component V_h as shown by Eq. (1.1) [14, 15].

$$V_s = V_1 \sin(2\pi f_1 t) + \sum_{h=2}^{p} V_h \sin(2\pi f_h t + \phi_{vh}) \tag{1.1}$$

Where ϕ_{vh} is the phase of harmonic voltage and f_h is the frequency of harmonic component of voltage.
Similarly a distorted load current waveform can be represented as a sum of fundamental component I_1 and harmonic component I_h as represented by Eq. (1.2).

$$I_L = I_1 \sin(2\pi f_1 t + \phi) + \sum_{h=2}^{M} I_h \sin(2\pi f_h t + \phi_{ih}) \tag{1.2}$$

Where ϕ_{ih} is the phase of harmonic current.

1.2.3 Classification of Harmonics

There are many types of harmonics which are briefly explained here [16]. The significance of each type is also discussed.

1.2.3.1 ODD Harmonics

When the distorted waveform under observation is symmetrical above and below its average centerline, the harmonic frequencies will be odd integer multiples of the

fundamental frequency only and their will be no even integer multiples. The most of loads produce such current waveforms thus odd harmonics are more dominant.

1.2.3.2 Even Harmonics

In power systems usually, the even-numbered harmonics (2nd, 4th, 6th, 8th, 10th, 12th,etc.) are not present due to symmetry between the positive and negative halves of a cycle. Thus the limits on even harmonics are more relaxed as compared to those on odd harmonics.

1.2.3.3 Triplen Harmonics

Triplen harmonics are defined as odd multiples of the third harmonic and are of a particular concern in three-phase power systems. They cause a sharp increase in zero sequence current thus increases the current in the neutral conductor.

1.2.3.4 Interharmonics

Interharmonics are non integer multiples of fundamental frequency. Interharmonics add extra signals to the power system which can cause a number of effects, particularly if they are magnified by resonance. The risk of resonance increases with the presence of wider range of frequencies. Many of the effects of interharmonics are similar to those of harmonics, but some are unique as a result of their non-periodic nature.

1.2.3.5 Sub Harmonics

Sub harmonics are the harmonics with frequencies less than the fundamental frequency. Series capacitors are used to increase the amount of real power by cancelling a portion of the inductive reactance but this creates a new problem in the system. When a capacitor is used in a transmission line as a series element, sub-harmonic currents are created.

1.2.3.6 Positive Sequence, Negative Sequence and Zero Sequence Harmonics

Positive sequence harmonics rotate with the same sequence as the fundamental such as the 7th harmonic. On the other hand negative sequence harmonics rotate in the opposite sequence as the fundamental like the 5th harmonic. Triplen harmonics which don't rotate at all because they're in phase with each other, are called zero sequence.

1.2.4 Effects of Harmonics on Electrical Utility System

Electrical utility system is affected by both voltage and current harmonics. These effects are separately described below.

1.2.4.1 Voltage Harmonics

The frequent cause of voltage harmonics is the current harmonics. The current harmonics will distort the source voltage due to source impedance. In case of small source impedance, current harmonics will cause only small voltage harmonics. It is usually the case that voltage harmonics are definitely small compared to current harmonics. This is why the voltage waveform can generally be approximated by the fundamental frequency of voltage. This approximation results in no effect of current harmonics on the real power transferred to the load. However, in case of higher voltage harmonics, current harmonics do make a contribution to the real power transferred to the load.

1.2.4.2 Current Harmonics

Normally the current varies sinusoidally at a specific frequency, usually 50 or 60 hertz. The linear load draws a sinusoidal current at the same frequency as the voltage. Current harmonics are caused by non-linear loads. When a non-linear load,

such as a rectifier is connected to the system, it draws a non sinusoidal current. The complexity of distortion in the current waveform depends on the type of load and its interaction with other components of the system. Semiconductor devices like transistors, IGBTs, MOSFETS, diodes etc are all non-linear loads. Electric motors do not normally contribute significantly to harmonic generation. Both motors and transformers will however create harmonics when they are over-fluxed or saturated. Non-linear load currents create distortion in the pure sinusoidal voltage waveform supplied by the utility, and this may result in resonance.

The neutral conductor usually carries the zero sequence current due to the unbalanced loading among phase conductor. As more and more electronic equipments being used, the harmonic currents drawn by their rectifier front ends also become significant. Especially, the zero sequence triplen (3rd, 9th, 15th) harmonics accumulate in the neutral conductor, thus result in its overloading [17]. Excessive harmonic currents in the neutral conductor can cause wiring failure due to improper sizing. Also the excessive neutral to ground voltage due to a voltage drop caused by the neutral current can result in the malfunction of sensitive electronic components [18].

In the presense of harmonics the current can have a high crest factor resulting in an inaccurate secondary current in transformers. High current peaks may lead to transformer saturation. When the saturated secondary current is fed through a resistance, the resulting voltage wave will have suppressed or flattened peaks [19].

1.2.5 Harmonics Assessment and Quantifiation

Harmonics assessment is made by connecting a non-linear load to a three phase AC source at the point of common coupling. Harmonics are extracted from the load current using a reference current generation technique. FFT tool in Matlab/Simulink is used to calculate harmonic distortion in the current waveform.

The quantification of harmonics in voltage and current signals is made through a parameter known as Total Harmonic Distortion (THD). The Total Harmonic Distortion for current, THD_i is mathematically expressed by Eq. (1.3) and is defined

as, "A ratio of addition of all the harmonic components of the current waveform to the fundamental component of the current waveform "[20].

$$\text{THD}_\text{i} = \sqrt{\frac{{I_2}^2 + {I_3}^2 + {I_4}^2 + \ldots . {I_n}^2}{{I_1}^2}} \times 100\% \tag{1.3}$$

Where I_1 is the fundamental current and I_n is the nth harmonic component of current.

The total harmonic distortion for a voltage, THD$_v$ is mathematically expressed by Eq. (1.4)

$$\text{THD}_\text{v} = \sqrt{\frac{{V_2}^2 + {V_3}^2 + {V_4}^2 + \ldots . {V_n}^2}{{V_1}^2}} \times 100\% \tag{1.4}$$

Where V_1 is the fundamental voltage and V_n is the nth harmonic component of voltage.

Harmonics compensation ratio i.e the HCR factor can be used to evaluate the performance of harmonics mitigation technique and is calculated by Eq. (1.5) [21].

$$HCR = \frac{THD \;\; after \; compensation}{THD \;\; before \; compensation} \times 100\% \tag{1.5}$$

1.2.6 Standards governing Harmonics

The standards governing harmonics are briefly described here.

1.2.6.1 IEEE-519 Standard

IEEE-519 standard is a handy discription of harmonics and applying harmonic limits in power systems. It is useful to understand harmonics in terms of percent of fundamental to get an understanding of the relative harmonic levels in a system. Harmonic voltage distortion on power systems 69kV and below is limited to 5 % THD with each individual harmonic limited to 3 % according to IEEE-519. The limit for current harmonics vary based on the short circuit strength of the system

in which they are being injected. Basically, the more the system is able to handle harmonic currents, the more the customer is allowed to inject. The aim of applying harmonic limits according to IEEE-519 is to prevent one customer from causing harmonic problems for another customer or for the utility. Thus applying this standard will result in a good power quality.

1.2.6.2 IEC-61000-3-2 Standard

The aim of IEC 61000-3-2 is to set limits to the harmonic currents drawn by electrical apparatus and thus maintaining mains voltage quality. The IEC has developed harmonic limits specifically to maintain voltage quality. Planning levels for voltage harmonics are established based on electromagnetic compatibility requirements for end-use equipment. For the general case, the IEC recommends that permissible voltage harmonic emission levels be converted to current harmonic emission levels using the actual system frequency dependent impedance.

1.2.6.3 EN50160

EN50160 is the standard which defines the main characteristics of the voltage at a network users supply terminals in public low voltage and medium voltage electricity distribution systems under normal operating conditions. EN50160 gives the limits or values within which the voltage characteristics can be expected to remain, and does not describe the typical situation in a public supply network. According to this standard THD of the supply voltage including all harmonics upto 40th order should be less than or equal to 8%.

1.2.6.4 ANSI C82.77

This standard specifies harmonic limits and methods of measurement for lighting equipment. Harmonic emission limits defined by this standard include both harmonic and interharmonic emissions over the low frequency range 0 - 9 kHz.

1.2.7 Why Harmonics Mitigation

The flow of harmonic currents badly affects the power system by lowering the power factor and deteriorating the voltage quality. Addition of harmonic generating loads such as power electronic equipment by consumers is increasing the level of harmonic current flow in power systems. The increasing use of non linear loads in the industry caused serious perturbation issues in the electric power distribution grids. In addition to high consumption of reactive power, regular increase in the harmonic emissions and current unbalance can also be noticed. The flow of harmonic currents in the electric grids can also cause voltage harmonics. These harmonic currents can interrelate harmfully with a wide range of power system equipments, control systems, protection circuits, and other harmonic sensible loads. Harmonic currents result in not only voltage distortions at PCC, but also increase RMS-value and peak-value of the line current which can cause additional losses like overheating and overloading, sometimes failure of power system equipments like capacitors, transformers and motors, frequent tripping of circuit breakers, and blowing of the fuses. Moreover, they can also cause interference with telecommunication lines, errors in power metering, and resonances in distribution systems. Thus harmonics is the main issue out of all power quality problems and it is necessary to mitigate the harmonics.

1.3 Harmonics Mitigation Techniques

In Power systems the use of power electronic converters is very common . These converters have some benefits but also causes some adverse effects due to the non-sinusoidal current taken by them. Moreover, the trend of using energy saving appliances has increased greatly in few years. The drawback of these loads is the introduction of harmonics onto the distribution systems [22].

In [23] a review of harmonic analysis and its mitigation techniques is presented describing their advantages and disadvantages. Active power factor correction techniques, using smart algorithm to cancel the distortive power, have been reviewed

for further research. Nonlinear physics of harmonic phenomenon is described to explore its applications.

In [24] an optimal selective harmonic mitigation (OSHM) method is implemented using the least possible switching frequency to satisfy three grid codes EN 50160, CIGRE JWG C4.07 and IEC 61000-3-6. The proposed method also minimizes the individual harmonics as much as possible. The harmonics up to 40th are mitigated to satisfy three voltage harmonic standards EN 50160, CIGRE JWG C4.07 and IEC 61000-3- 6 from both individual harmonics and THD point of view. [25] presents a new SHM-PWM control strategy which is capable of meeting grid codes even under non-equal DC link voltages. The method is based on the interpolation of different sets of angles obtained for specific situations of imbalance. Both simulation and experimental results are presented to validate the proposed control method.

In most countries the standard value of frequency for power systems is 50 or 60 Hz. Harmonics are mainly caused by the connection of non-linear loads to the supply. Harmonics may lead to large currents in neutral conductors in a three phase four wire sytem [26]. Furthermore, voltage and current waveforms remain no longer sinusoidal [27]. The power electronic devices are frequently used in almost all power levels due to their efficient performance and control features [28]. Hence, the problem of power harmonics has increased to a great extent. The negative effects of harmonics include tripping of circuit breakers, overheating of cables and transformers, failure of capacitors, increase in resistive losses or voltage stress and power factor reduction. [29]. A distorted waveform can be represented by Eq. (1.6).

$$x\left(t\right) = X_0 + \sum_{k=1}^{k=\infty} X_k \sqrt{2} \sin(k\omega t - \phi_k) \tag{1.6}$$

Moreover, the poor power quality increases the power cost [30, 31]. Passive and active both techniques are used for harmonics mitigation [32–38]. These techniques are briefly discussed here. The advantages and disadvantages of these techniques are also stated to best suit the application.

1.3.1 Passive Harmonic Mitigation Techniques

Various passive techniques are used for mitigation of harmonics in electrical network [39]. In passive techniques a high series impedance is inserted between the load and supply to block the flow of harmonics current into the system. The flow of harmonics current can also be diverted by creating a low impedance parallel path. Some of the passive techniques are briefly discussed below.

1.3.1.1 Passive Filters

In passive filters a resonant circuit is configured using capacitors and reactors which are tuned such as to eliminate a specific order of harmonics [40]. Thus a separate filter is needed to remove each order of harmonics. The cost of passive filters is low as compared to active filters but it covers only one operating point due to which it works inefficiently at partial load. Moreover, due to the internal constellation of chokes and capacitors, it results in a bad power factor. In series passive filters, inductors and capacitors are tuned to provide a high impedance at the selected harmonic frequency thus blocking the flow of harmonic currents. On the other hand the flow of fundamental current is made through the low impedance path created by the filter. In parallel passive filters low impedance path is offered to the flow of harmonics which are then grounded.

1.3.1.2 Line Reactor

This method is considered as simplest for reducing harmonics. In this method an inductive reactance is inserted in series with a harmonics producing load. The use of line reactor also results in absorbing the voltage transients that may cause tripping of VSD due to over-voltage. The effective impedance of this reactor is important in determining the amount of harmonic distortion and actual range of harmonics [41]. The main advantages of this technique are low cost, substantial decrease in voltage and current harmonics and availability in several standards of

percent impedances. There are also some drawbacks as it causes a drop in voltage and increase in system losses.

1.3.1.3 Mullti-Pulse Techniques

This technique include 12-pulse and 18-pulse rectifier schemes. In this scheme a special type of configuration is used for rectifier and transformer. In 12-pulse scheme transformer has two separate secondary windings and it can reduce the distortion level of harmonics between 10-20 %. In 18-pulse rectifier there are three secondary windings which results in a much better result in the range of 5-10 % [42].

Multi-pulse technique has the disadvantage that the current THD increases with decrease in load. It also requires the current drawn by each rectifier bridge to be balanced and the three phase voltages also should be balanced. Otherwise it can cause flow of triplen harmonics thus increasing the level of harmonics distortion.

1.3.2 Active Harmonics Mitigation Techniques

In active techniques the harmonics distortion can be reduced by adding current or voltage distortion of the same magnitude and anti phase at PCC. Active power filters are commonly applied for reducing harmonics distortion within the limits defined by IEEE-519 standard [43]. Active filters can be good alternative for controlling the harmonics level in power systems. They have many benefits as apposed to passive filters like adaptation with the variations in the load, selective harmonics compensation, reactive power compensation and no resonance problem [44]. The active filter works by first generating a reference current which is the inverse of extracted harmonics current and then by using power electronic switching, it injects the reference current at the PCC to cancel the individual harmonics [45]. Active power filters are mainly classified on the basis of power circuit configuration like series active power filter and shunt active power filter. They are briefly discussed here.

1.3.2.1 Series Active Power Filter

In this type the filter is inserted in series with the load and they are mainly used for compensation of voltage harmonics. It cancels out the voltage disturbances comming from the grid by injecting voltage in series with the supply voltage. [46].

1.3.2.2 Shunt Active Power Filter

In this type the filter is connected in parallel with the harmonics producing loads and is used for compensation of current harmonics. It is the most widely used technique due to its flexibility and capability to be integrated as part of the existing equipment. SAPF takes only a portion of the fundamental load current, thus they have lower component ratings as apposed to series active power filters. In case of series APF we will have the total current passing through the filter due to which ratings for power electronic switches will be high [47, 48].

1.4 Working Principle of SAPF

The main function of SAPF is to generate a reference current and injecting it at the PCC to reduce the level of harmonics distortion [49]. The current injection is done by precisely switching the VSI IGBTs using pulses generated by a suitable controller. Fig. 1.8 shows the working principle of SAPF and main building blocks of three phase SAPF are shown in Fig. 1.9.

FIGURE 1.8: Working Principle of SAPF

The two main parts of active power filters are reference current generation and current injection. Harmonics can be cancelled in two steps. The first step includes

generation of the reference current which is actually same in magnitude like the harmonics current but with reversed phase. A number of techniques are used for reference current generation in both time domain and frequency domain. Time domain techniques employ coordinate transformation of voltage and current signals, while frequency domain techniques are based on Fourier analysis. Some techniques use frequency and phase information of the source voltage like synchronous reference frame theory commonly known as d-q theory and other techniques does not need to estimate frequency and phase like instantaneous reactive power theory and DFT. The synchronization of active filters with the grid voltage is also very important aspect for good performance under adverse grid conditions. Under such conditions the generation of a precise reference current is very difficult. Thus it is important to consider this aspect in order to get superior and robust performance of SAPF.

The second step is to inject the reference current at PCC using a suitable control strategy. The current injection controller tracks the reference current and generate pulses to operate IGBTs of voltage source inverter. The injected current will result in cancellation of harmonics and a pure sinusoidal waveform is obtained. The regulation of DC link voltage is also necessary for accurate current injection and must be maintained at the required value. From the block diagram of SAPF the source current i_s can be mathematically expressed by Eq. (1.7).

$$i_s = i_l + i_c. \tag{1.7}$$

Where i_l represents the load current and i_c is the compensating current.

1.5 Motivation

In recent times the use of non-linear load by electric power consumers has increased to a large extent . Such loads introduce harmonics and other power quality problems thus affecting the power quality. Furthermore, the demand of energy saving

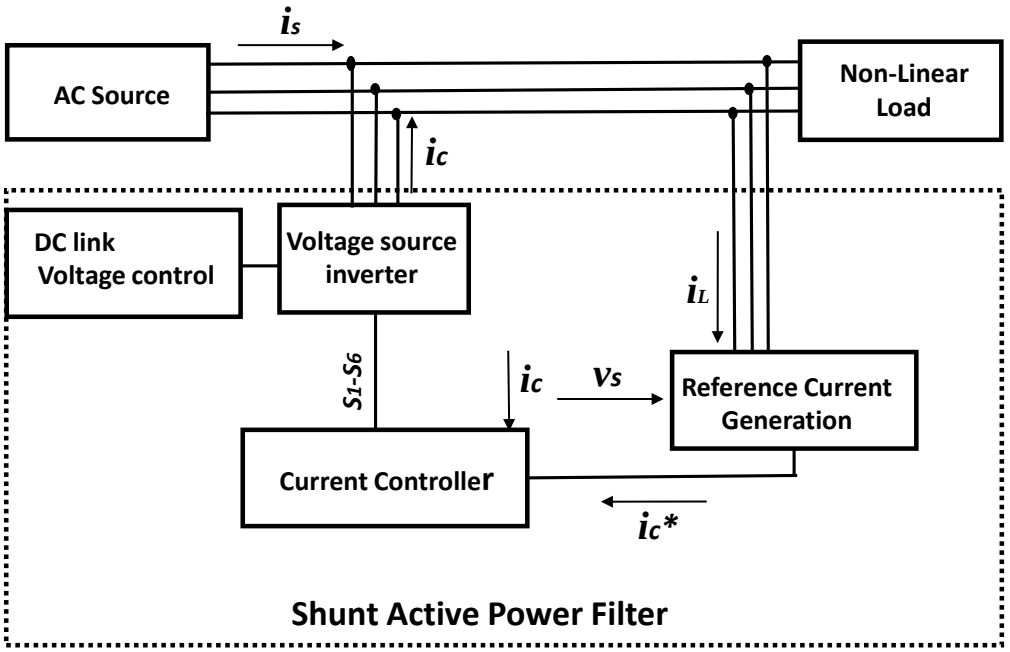

FIGURE 1.9: Block Diagram of SAPF

appliances in recent years has also increased. The use of such smart appliances also add harmonics to the power system. The polluted grid will result in more energy losses and cost of electric supply will considerably increase. Power quality is affected mainly by the current harmonics that gives a motivation for this research. The harmonics free supply will result in high efficiency and improved power factor thus energy saving and reduced cost objectives will be achieved.

1.6 Scope of the Thesis

The scope of this thesis covers the following points.

- Assessment of the impact of harmonics on power and need for harmonic compensation.
- Identification of problems affecting the power quality and harmonics mitigation techniques.
- Analysis of the impact of non-ideal grid conditions on the performance of SAPF.

- Analysis of the performance of phase locked loop techniques under various grid disturbances.
- Development of an improved reference current generation technique with added synchronization feature.
- Identification of the importance of DC link voltage regulation in the current injection process.
- Analysis of the effects of synchronization techniques on the performance of SAPF.
- Identification of the constraints of using APF without synchronizing it with the grid voltage under adverse grid conditions.
- Conclusion of the research work accomplished in this thesis and giving recommendations for future work.

1.7 Objective and Objective Function

The main objective is to minimize harmonics in the source current due to the presence of non -linear loads connected at the point of common coupling. The objective function is mathematically described by Eq. (1.8).

$$minimizeH(N) = \frac{1}{I_{s1}} \sqrt{\sum_{n=2,,3,.....}^{\infty} {I_{sn}}^2} \tag{1.8}$$

Where *H(N)*is defined as the objective function for minimization of harmonics, I_{s1} is the fundamental current and I_{sn} represents the harmonics. This function is subject to the constraint shown by Eq. (1.9).

$$THD_{Is} < THD_{limit} \tag{1.9}$$

Where THD_{limit} is 5% as defined by IEEE-519 standard.

1.8 Thesis Outline

Chapter 1: In this chapter power quality is defined and its importance in modern power distribution system is explained. Different issues affecting the power quality are briefly overviewed. Harmonics issue and the existing techniques for its mitigation are also briefly discussed. SAPF which is the research aim of this thesis is explained in detail. Motivation of the research and objectives and scope are also stated in this chapter.

Chapter 2: This chapter presents the literature review of the research efforts carried out in the domain of active power filtering and analytically studies the techniques proposed in the literature. Finally a research gap is identified in the previous work and a solution to fill this gap is suggested.

Chapter 3: This chapter discusses the techniques used for reference current generation. Mathematical model of SAPF is also developed here. Time domain and frequency domain techniques are studied and are evaluated in simulation by adding the reference current to the distorted source current to get a sinusoidal waveform. A low value of THD of the compensated source current will show the accuracy of the observed technique.

Chapter 4: This chapter deals with the current injection part of active power filters. An overview of three control techniques is presented which are used to generate gating signals for voltage source inverter in order to inject the reference current at the point of common coupling. The regulation of DC link capacitor voltage is briefly studied too in this chapter.

Chapter 5: In this chapter both conventional and advanced PLL techniques are overviewed and evaluated under distorted grid conditions. These techniques are tested for accuracy and quick response in the estimation of frequency and phase. The best evaluated technique is used for synchronization of SAPF. The SAPF is simulated both with and without synchronization feature under different grid disturbances like frequency drift, phase angle jump and dc offset. The results of proposed technique are also compared with previously published papers.

Chapter 6: This chapter concludes the research work and few recommendations for future work are also stated.

1.9 Summary

In this chapter the importance of power quality has been highlighted and various power quality problems are explained. Impact of these problems on power qulaity is studied. Among the various problems, harmonics and its drawbacks are discussed in detail. Furthermore, a brief overview of both passive and active techniques used for harmonics mitigation is presented. A detailed discussion on the working of shunt active power filter, highlighting its different parts is presented. In summary, shunt active power filter is being recognized as the best solution for mitigation of current harmonics. Furthermore, the control techniques used for reference current generation and current injection have a vital role to play in the performance enhancement of SAPF.

The following chapter presents the review of contributions made by different researchers in developing control techniques for active power filters.

Chapter 2

Literature Review

2.1 Introduction

This chapter discusses various approaches for developing control techniques of active power filters. The aim is to explore the efforts of researchers made in the past for developing control strategies of SAPF. The survey is presented by categorizing the main parts of SAPF and discussing the limitations and useful features of the control techniques. Literature review ends by exploring the research gap in the previous work and suggesting a solution to rectify the problem.

2.2 Reference Current Generation

In [50] comparison of four techniques used for generating the reference current was presented. These techniques include p-q theory, d-q theory, unity power factor (UPF) and perfect harmonic cancellation (PHC). The author proved the effectiveness of PHC technique as it was able to eliminate the imbalance also in addition to harmonics compensation. A harmonic detection scheme based on goertzel algorithm was proposed in [51]. The technique was effective in terms of using less computation time and fewer stored coefficients. In [52] a computationally efficient and robust technique based on discrete fourier transform was proposed for this

purpose. This technique was simulated under non-ideal conditions and its robustness and computational efficiency was verified by experimental results.

In [53] two theories were compared for generation of reference current and it was concluded that SRF theory was more efficient in reducing harmonic distortion as compared to p-q theory. In [54] six different techniques were evaluated for reference current generation and perfect harmonic compensation technique was found best among all.

Three techniques including p-q theory, SRF theory and DFT have been evaluated in the presence of different non-linear loads [55, 56]. For balanced load p-q theory gives better results but for un-balanced condition DFT shows better performance.

In [57] self-tuning filter algorithm is implemented to get the reference current. The key benefit of this technique is its simplicity and efficiency in non-ideal voltage condition.

In [58] Sundaram and Venugopal implemented the synchronous reference frame theory in active power filtering. They connected a non-linear load with a current THD of 29 % and were able to reduce it upto 2 % using SRF theory for reference current extraction. In [59] the instantaneous power theory was observed under the effects of supply voltage harmonics. It was concluded that in the presence of distorted supply the compensating current contained a disturbing component due to which this method was not able to extract the reference current.

In [60] the author used srf based control strategy for the real time implementation of sapf. They used RL and RLC load for evaluation and got good results in terms of low THD value according to IEEE-519 standard. Karthikeyan et al in [61] proposed an ADALINE based neural network control for load compensation. They extract the harmonic current using the proposed theory and found satisfactory results for RL load.

In [62] a review of control strategies used for reference current extraction, DC link voltage control and current control algorithms used for active power filtering is presented. Advantages of the techniques and their shortcomings are also discussed. Davood Yazdani in [63] proposed an adaptive notch filtering approach to generate the reference current. This method was able to extract the harmonic

current components efficiently. In [64] a real-time implementation of selective harmonic mitigation using an off-the-shelf mid-range microcontroller is presented and tested. The Exchange Market Algorithm (EMA), is considered and executed to achieve targets. In both cases, steady-state and transient response, the EMA-based method converged quickly and accurately, obtaining a good switching angle solution set in a reduced number of fundamental periods. In [65] an asymmetric selective harmonic current mitigation-PWM (ASHCM-PWM) technique is used to meet the current harmonic limits of a power quality standard with the effects of grid voltage harmonics considered in the equation set of its optimization process. The proposed technique can mitigate the current harmonics of CHB converters to meet the current harmonic limits defined in IEEE-519. In [66] a selective harmonic current mitigation pulse width modulation (SHCM-PWM) technique with low switching frequencies is proposed for grid connected cascaded H-bridge multilevel rectifiers to fully meet harmonic requirements within extended harmonic spectrum. In the proposed technique, instead of using the voltage references to calculate switching angles for the rectifier as in conventional selective harmonic elimination PWM (SHE-PWM) or selective harmonic mitigation-PWM (SHM-PWM), current references are used to compensate the current harmonics due to both grid voltage harmonics and rectifier input voltage harmonics so as to meet the current harmonic requirements and total demand distortion (TDD) within the whole harmonic spectrum. In [67] a modified p-q theory was presented to overcome the limitations of the conventional p-q theory. The method was able to achieve compensation objectives in a simplified approach. In [68] a novel reference current generation technique was proposed that was also able to eliminate other power quality problems. The proposed controller reduced the number of parameters used for tuning. Popescu in [69] presented the implementation of DSP based p-q theory. A comparison of IRP theory and Fryze current computation technique was presented in [70]. In [71] two adaptive filters were used by incorporating zero crossing detection technique for reference current generation. The technique used reduced computational resources in addition to good dynamic performance under adverse grid scenario. A multi frequency technique was proposed for calculation

of reference current [72]. The proposed method was able to transfer active power without low frequency ripple. In [73] a dual fundamental component extraction algorithm was proposed for reference current generation. In this method two STF based algorithms were used under the effects of unbalanced and distorted voltage. With this method an improved performance was achieved without inculding a low pass filtter for isolation of harmonics and fundamental components of load current and also no PLL circuitry was required. Yacine Terrechi in [74] proposed a matrix pencil based reference current generation technique. The author proved the effectiveness of the method having a good dynamic performance under unbalanced and distorted voltage. Voltage phase was also accurately estimated by the proposed method. In [75] a new strategy was suggested based on VLLMS algorithm for reference current extraction. The proposed controller also included a self-charging algorithm for controlling the DC link capacitor voltage. Results achieved proved the efficient performance and robustness of proposed controller under various grid disturbances. In [76] an improved controller based on DFT algorithm for selective harmonic compensation was proposed to overcome the slow dynamic response and sensitivity to frequency fluctuation of the traditional Repetitive Discrete Fourier Transform controller. Each harmonic frequency was individually treated for compensation purpose in the unique control configuration to attain best performance. With this structure the controller achieved fast transient response and stability. Sachin devassy in [77] proposed a novel technique by implementing the proportional resonant controller and second order sequence filter to extract the reference signal. This technique gave good accuracy with less computation burden as it was able to extract the load current active components of all three phases with a single sample and hold operation. Furthermore, the use of double stage PV system kept the DC link voltage close to the required value. In [78] a model predictive control was proposed to compensate the input disturbances and reduce the amount of harmonics distortion. Moreover, the effects of source voltage distortions were also eliminated by the proposed algorithm.

P-q theory has been widely used by researchers but it has the drawback of poor performance in the presence of unbalanced load. It does not require a PLL but

this benefit turns into a disadvantage in the presence of grid disturbances. SRF theory nedds a PLL for phase estimation but its performance is also affected by grid voltage disturbances. In case of frequency domain techniques DFT involves more calculations that is responsible for a slow dnamic response.

2.3 Synchronization Techniques

Synchronization of grid connected power converters is one of the important issue to be solved in industrial and power applications [79–81]. In order to ensure synchronization of power converters voltage, frequency and phase angle of the grid should be continuously monitored. "Synchronization is the process of extracting the information about frequency and phase angle of the fundamental frequency positive sequence component of the grid voltage" [82]. The phase information of the grid voltage is needed to obtain reference current [83, 84]. This infers that accurate phase information is required to achieve the best power quality objective.

Phase locked loop (PLL) is the commonly applied technique for synchronization of the grid [85, 86]. Between several types of PLL, the synchronous reference frame PLL (SRF-PLL) established on PI controller is perhaps the most frequently used because of its easy implementation and simple structure [87–91]. [92] presented the small signal model of SRF-PLL to eliminate the effects of dc offset. The state space model was used to eliminate the effects of dc offset. Many researchers have worked on SRF-PLL for the estimation of grid phase and proves its accuracy if the electric grid does not contain harmonics and is balanced [93]. Conversely, if the grid voltage contains harmonic components, the PI-based SRF-PLL shows inaccurate estimation of phase [94]. The performance of the implemented strategy can be improved by carefully selecting the tuning parameters of the PI controller [95]. However, by using this approach response time is increased. In [96], a feed forward action is applied to reduce the response time. Likewise, in [97, 98], a number of techniques are presented to remove unwanted ripples in the estimated phase, but a drift in the grid frequency of about 1-3 Hz is not taken into account in testing the proposed technique. In [99] a refined small signal SRF-PLL model

was suggested to examine the variations of input voltage magnitude. In [100] an adaptive SRF-PLL structure was proposed to work under the grid voltage disturbances but this method increases the computational burden. In [101] phase locked loop systems have been studied in the presence of in-loop filters.

In [102–104] moving average filter is used in the control loop of PLL. This technique has been proved to be effective under adverse grid, but, this approach results in reduction of open-loop bandwidth of PLL giving rise to slower dynamic response. A unique MAF-based PLL was presented in [105] employing SPLL to get high accuracy and fast reponse. In [106] design specifications of a MAF-PLL were given to implement the scheme with frequency feature. The author compared the performance of two algorithms of MAF-PLL, one using a PI controller and the other implemented a PID controller. The PID-type MAF-PLL showed better results in terms of dynamic response but reducing the ability to reject disturbances and noise immunity. The results of this approach were much better than the conventional SRF-PLL in terms of estimating the phase quickly and accurately. In [107], a quasi-type-1 PLL was suggested to achieve an increased open-loop bandwidth. This task was accomplished by using a simple gain instead of the PI controller. Though, the proposed approach was not able to perform well under the effects of dc offset and even order harmonics. In [108] a differential MAF-PLL was proposed that can narrow the MAF window width by rapidly eliminating the low order harmonics. In [109] PLL techniques including MAF-PLL were compared for synchronization of active power filter. In this case the performance was satisfactory in filtering different order of harmonics but speed of response was slow.

In order to improve the dynamic response, many techniques have been proposed by the researchers. Delayed signal cancellation PLL (DSC-PLL) is proposed in recent times in [110] that shows good capability in filtering only certain orders of harmonics. In [111] DSC based algorithm is proposed for a dynamic voltage restorer that has also the ability of sag detection. The transient response of CDSC-PLL is improved by cascading inside a phase lead compensator based on digitak filter [112]. In [113] a new open loop synchronization method is suggested which is based on compensation of phase deviation. For eliminating a quantified set

of harmonics multiple DSC blocks can be cascaded with different time delays [114–118]. Nevertheless, in order to eliminate all orders of harmonics five DSC blocks are necessary to be cascaded. In [119] an improved DSC-PLL including a phase lead compensator is proposed with good filtering capability and fast dynamic response. An adaptive DSC-PLL is proposed in [120] that can easily eliminate harmonics of different order thus making it more flexible and robust. In [121] delayed signal cancellation is invetigated for harmonic extraction under adverse grid by adopting a generalized trigonometric function (GTFDSC). Davood Yazdani in [122] presented a comparison of synchronization techniques for three phase systems in the presence of low order harmonics and unbalance conditions.
From the literature review it is observed that SRF-PLL does not perform well under adverse grid conditions. MAF-PLL overcomes the issues of SRF-PLL but transient response of this approach is slow. Researchers have proved that CDSC-PLL is better solution to get a fast transient response and accurate estimation of frequency and phase in the presence of grid disturbances.

2.4 Current Injection Techniques

The final stage of active power filtering is the injection of current at PCC. For this purpose a fast and accurate control method is required to generate pulses for VSI according to the waveform pattern . The control technique with accurate current injection capability results in good compensation performance of active power filters. In SAPF the most commonly used technique is the hysteresis control technique because of its simple implementation. In hysteresis method, the current being injected is kept inside the hysteresis band by controlling the switches of inverter. In this technique high switching losses occur due to increased switching frequency. Researchers have proposed some useful techniques for current injection [123–126]. The Deadbeat controller used for this purpose shows good dynamic response but has a drawback of implementation complexity and parameter dependency. In [127, 128] Repetitive control method is used to inject current but under certain conditions this controller has the issue of stability. One-cycle control is

proposed in [129] as current control technique and is being proved as robust and simple to implement. OCC controller has the disadvantage of instability for some types of loads. In [130, 131] the conventional method of hysteresis control is implemented for current control and has been proved to be efficient and simple to implement. It has the disadvantage of high switching frequency giving rise to high switching losses. Adaptive hysteresis current-control is used in [132] to decrease the switching frequency but it results in increased control complexity. In [133] Komurcogil proposed a modified hysteresis control method by using double band for single phase system and found it useful in terms of reducing switching frequency. In [134] two current control techniques including hysteresis control and sinusoidal PWM were compared for current injection. In [135] an array of resonant current controllers was used for selective harmonic compensation, which resulted in good performance of active power filter in terms of THD reduction. In recent times researchers have proposed some more techniques for current injection including sliding mode control, model predictive control, repetitive control, kalman filter based H infinity control and one cycle control. [136–140]. In [141] Arunsankar and Srinath proposed a hybrid control strategy combining EGOA and ANN known as EGOANN to inject the corrective current at PCC. The author proved by simulation result that the harmonic distortion can be reduced to an acceptable level due to the load change or parameter variation of the power system. Also, less computations make the proposed technique more effective and reduce the complexity of the algorithm. In [142] three techniques are compared for performance evaluation as current controllers and sliding mode control is proved as the best technique as a current controller. In [143] Arivarasu proposes a non-linear function based closed loop control strategy for three-phase SAPF and LC passive filter to reduce harmonics, improve power factor and boost the dynamic performance. In [144] an improved performance of active power filter was achieved with a predictive control scheme based on four leg VSI. This scheme allowed the compensation of unbalance in addition to harmonics mitigation. The controller also improved the current tracking capability and transient response of active power filter. In [145] Sreeraj proposed one cycle control method for compensating only harmonics components.

The device current rating and switching losses were reduced with the help of this method. In [146] the author proposed an improved deadbeat controller as current control technique with a two-step prediction method. It was able to lower the bad effects of current sampling error and improve the interference rejection capability of the control system. In [147] an adaptive control scheme was proposed for APF to improve the performance under various grid disturbances. This scheme achieved good results under variable grid frequencies and harmonically polluted grid voltage. In [148] a fixed frequency sliding mode control was proposed for current injection in active power filter. A smoothing procedure was adopted to reduce the chattering problem. Chattering is a phenomenon of oscillaions having finite frequency and amplitude caused by high frequency switching of sliding mode controller. A prototype 6-kVA inverter was used to verify the performance of the proposed controller by presenting simulation and experimental results. In [149] a modified model predictive controller with fixed switching frequency was presented for current injection of APF. The high current ripple of the conventional MPC was reduced by using a modulation strategy based on cost function without affecting the dynamic performance. In [150] H-infinity based controller was suggested for controlling the current to be injected. The proposed strategy gave a stable performance with ability to reject disturbances. The author also proved the robustness of technique against parameter variation and grid disturbances. In [151] an adaptive sliding mode current control with fixed frequency was applied to control injection current of SAPF in single phase systems. The author proved that the proposed control technique worked efficiently and robustly for all sorts of grid disturbances. The current controller consisted of two branches to separately control fundamental and harmonic currents. Furthermore, the tracking error of the fundamental current was eliminated effectively.

From the literature review it is observed that implementaion of hysteresis control is very easy but it has no limit on the switching frequency. Deadbeat control has the disadvantage of implementation complexity. Repetitive control method has the stability problems. The sliding mode control is a better solution as a current injection controller but the sliding surface should be properly designed to get a

good performance.

2.5 DC Link Voltage Control

An efficient and reliable control technique for this purpose is required in order to inject the current accurately. In [152] the conditions for stabilizing the voltage of DC link capacitor were defined and the effects of the fundamental sequence components on input active power of the inverter were explained in detail. The technique was implemented in two parts. The first part maintained the actual voltage of the DC link capacitor at the required level and in the second part its balance was attained by controlling the output negative sequence current.

Zainuri proposed a new strategy by adopting self-charging algorithm that could cancel the error between actual and reference value in steps [153]. This method was not affected by changes in non-linear load during dynamic operations. In [154] the author proposed a novel recurrent probabilistic fuzzy neural network for such control that was able to maintain the DC link voltage during changes in non-linear load. Yap Hoon in [155] presented a method known as inverted error deviation for this purpose. The dynamic response and accuracy of the conventional algorithm was improved considerably with the new approach. The proposed algorithm was also tested by varying the load. DC link capacitor considerations have been studied for multi phase voltage source inverters in [156]. In [157] a voltage controller (VC) was used to measure only V_{dc} and not sensing all the DC link side currents like the conventional methods to maintain it at the reference level. The 3P4W SAPF was investigated for DC-link voltage control strategy [158]. Rinat R. Nasyrov and Raseel I. Aljendy in [159] presented the work for compensating harmonics through active power filter. They employed Hybrid Fuzzy-PI and PSO-PI controllers under distorted grid conditions and proved the effectiveness of the control techniques for regulating the DC link voltage. The PI control technique worked on the error among actual and reference values.

PI control has been widely used but it needs a precise mahemaical model to get the integral and proportional gains. Self charging algorithm used for this purpose

has the drawback of fluctuations and imbalance of the DC link voltage. Fuzzy logic control has the drawback of poor performance during dynamic operations. .

2.6 Research Gap Analysis

Review of literature suggests that a number of studies have been carried out to study the issues in power quality and harmonics has been recognized as the major power quality problem [1, 3, 4]. There has been a rapid increase in consumers preference towards good power quality and energy saving. The role of SAPF in mitigation of current harmonics has been deeply studied. Moreover, most of these studies have been mainly undertaken to understand the working principle of SAPF and control strategies used in development of active power filters [50, 51, 54, 57, 59]. The Scopes of most of the existing studies are limited to either reference current generation or current injection part of active power filtering. Moreover, there are no or very few studies on the synchronization of shunt active power filters. This feature plays an important role in the generation of reference current and becomes more valuable under adverse grid conditions. Therefore, in the light of previous discussion, a hypothesis for the research is build which stated that, "Shunt Active Power Filter synchronized with the grid voltage may shows better performance than its counterpart in the phase of introduced disturbances".

Moreover the study and literature review reveales that existing techniques for reference current generation are not very effective under the effects of grid disturbances. The reason for that is the use of a conventional PLL technique like SRF-PLL for estimation of frequency and phase inside the algorithm used for reference current generation. Literature study reveals that SRF-PLL is not very effective under the effects of grid voltage disturbances [79–81, 85, 86, 93, 94, 97, 98]. Thus there is a necessary need to address the problem of synchronization of shunt active power filters.

Finally, Therefore, there is a need for a comprehensive and robust technique to fix the problem of reference current generation under distorted grid conditions. This will result in better harmonics compensation capability and robustness of shunt

active power filter under the effects of grid disturbances. Thus the statement of problem would be

"To evaluate Shunt Active Power Filter for the task of harmonics mitigation under various grid disturbances using synchronization feature".

Contributions will include:

- Evaluation of PLL techniques for estimation of frequency and phase under the effects of frequency drift, phase angle variation and presence of DC offset.
- Developing a modified synchronous reference frame theory for reference current generation by implementing CDSC-PLL instead of the conventional PLL to improve its accuracy under grid disturbances.
- Evaluation of SAPF under various grid disturbances using the modified SRF theory.

2.7 Summary

This chapter presents the findings and contributions made by researchers in past for developing different control strategies of active power filters. Some of the recently proposed solutions are also discussed. The control strategies used in active power filtering are analyzed through a deep literature review. Literature review is categorized to address the important parts of active power filter and a better insight of the various control strategies. The useful features of these techniques are identified and further improvements in these techniques from different aspects are analyzed. At the end of literature survey research gap analysis is presented to identify the shortcommings of the techniques not addressed previously.

In the next chapter reference current generation techniques for active power filter will be discussed in detail.

Chapter 3

Reference Current Generation

3.1 Introduction

The reference current has a vital role to play in active power filtering. The accurate generation of reference current is the first main target in active power filtering and is a key to attain superior performance of the filter in reducing harmonic distortion. The techniques used for this purpose are generally categorized in two domains as shown in Fig. 3.1. In this section a brief overview of various reference current generation techniques is presented. A mathematical model of SAPF is developed to simplify the analysis of these techniques.

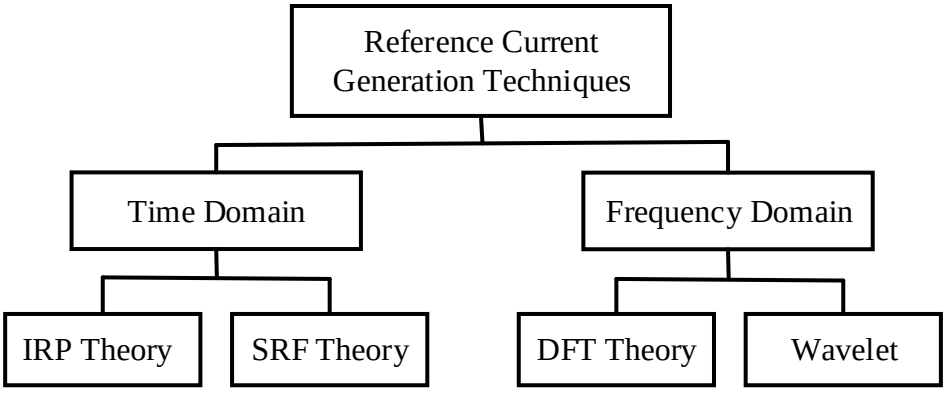

FIGURE 3.1: Types of Reference Current Generation Techniques

3.2 Mathematical Model of SAPF

The analytical behavior of SAPF can be successfully understood by modelling the three phase source with filter installed in parallel to the distribution load. The basic structure of SAPF connected to a 3P3W system is shown in Fig. 3.2.

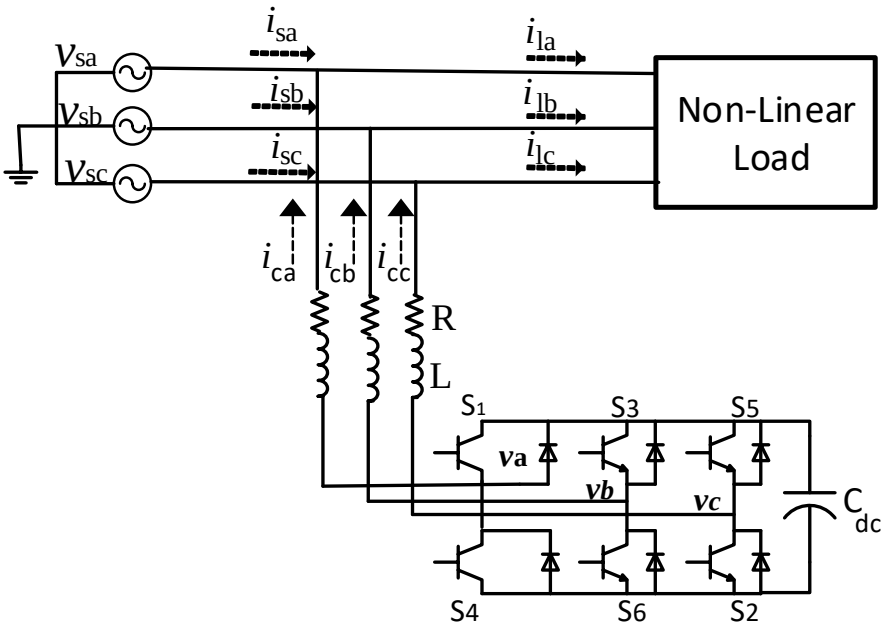

FIGURE 3.2: Basic Structure of SAPF

The three phase source voltages are represented by v_{sa}, v_{sb} and v_{sc}. Whereas i_{ca}, i_{cb} and i_{cc} represents the compensating currents actually injected. It is represented in abc frame using Eq. (3.1)

$$\left\{\begin{array}{c} L\frac{d}{dt}i_{ca} = v_{sa} - Ri_{ca} - v_a \\ L\frac{d}{dt}i_{cb} = v_{sb} - Ri_{cb} - v_b \\ L\frac{d}{dt}i_{cc} \ = v_{sc} - Ri_{cc} - v_c \\ C_{dc}\frac{d}{dt}v_{dc} = f_a i_{ca} + f_b i_{cb} + f_c i_{cc} \end{array}\right\} \tag{3.1}$$

Where f_a, f_b, and f_c are switching functions. Inductance and resistance of the filter are denoted by L and R respectively. C_{dc} is the capacitance at the DC link. The above equation can be written in matrix form using Eq. (3.2).

$$\frac{d}{dt}\begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & 0 \\ 0 & -\frac{R}{L} & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & 0 \\ \frac{f_a}{C_{dc}} & \frac{f_b}{C_{dc}} & \frac{f_c}{C_{dc}} & 0 \end{bmatrix} \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \\ v_{dc} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{sa} - v_a \\ v_{sb} - v_b \\ v_{sc} - v_c \\ 0 \end{bmatrix} \tag{3.2}$$

The transformation matrix required for conversion from *abc* to an arbitrary rotating *dq0* reference frame is given by Eq. (3.3). This transformation is helpful in reducing the control complexity.

$$T = \frac{2}{3}\begin{bmatrix} cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ sin\theta & sin(\theta - \frac{2\pi}{3}) & sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.3}$$

For simplicity a 3P3W system is considered, thus the addition of three-phase voltages and currents results in zero as shown in Eq. (3.4).

$$\begin{aligned} i_{sa} + i_{sb} + i_{sc} &= 0 \\ v_{sa} + v_{sb} + v_{sc} &= 0 \end{aligned} \tag{3.4}$$

Eq. (3.5) represents the currents in *dq* frame.

$$\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{f_d}{L} \\ -\omega & -\frac{R}{L} & -\frac{f_q}{L} \\ \frac{f_d}{C_{dc}} & \frac{f_q}{C_{dc}} & 0 \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_d \\ v_q \\ 0 \end{bmatrix} \tag{3.5}$$

Where the switching state functions of the system in *dq* reference frame are denoted by f_d and f_q and ω is the supply angular frequency. Eq. (3.5) can be re-written to get Eq. (3.6).

$$\left\{ \begin{array}{c} L\frac{d}{dt}i_{cd} = v_d - Ri_{cd} + \omega L i_{cq} - f_d.v_{dc} \\ L\frac{d}{dt}i_{cq} = v_q - Ri_{cq} - \omega L i_{cd} - f_q.v_{dc} \\ C_{dc}\frac{d}{dt}v_{dc} = f_d\ i_{cd} + f_q\ i_{cq} \end{array} \right\} \tag{3.6}$$

3.3 Instantaneous Reactive Power Theory

Akagi et al. introduced the instantaneous reactive power theory (IRP) in 1984 and is also known as p-q theory. This theory is very likely used for reference current generation in active power filters. In most cases the theory used in commercial APFs is dependent on IRP theory. This theory has the advantages of easy implementation and outstanding performance in steady state condition. Some of the disadvantages of IRP theory include requirement for a lot of voltage and current transducers, poor compensation in case of un-symmetrical voltages and slow response to transient changes in load. Fig. 3.3 shows the block diagram of p-q theory.

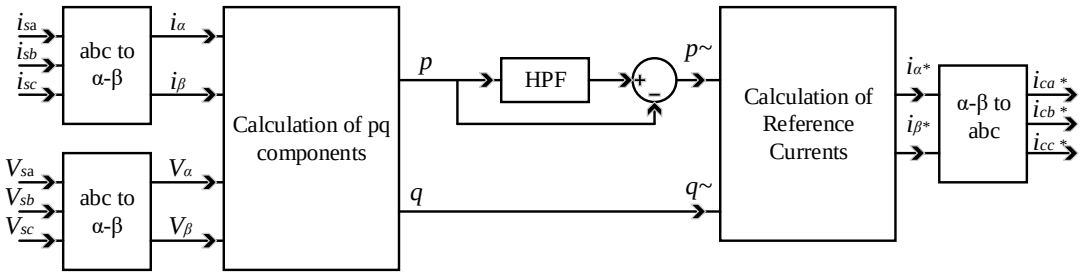

FIGURE 3.3: Block Diagram of p-q Theory

In this theory co-ordinate transformation is performed to get the currents and voltages in $\alpha\beta$ reference frame. This transformation is done by using Eq. (3.7) and Eq. (3.8) [160].

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{3.7}$$

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{3.8}$$

The instantaneous real and imaginary power components are obtained from Eq. (3.9).

$$\begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{3.9}$$

The zero sequence power only exists in three phase systems with a neutral wire. The zero sequence power and current are not present in a 3P3W system as shown in Eq. (3.10).

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.10}$$

Both AC and DC components are present in the above expression as can be seen in Eq. (3.11) and Eq. (3.12).

$$p = \tilde{p} + \overline{p} \tag{3.11}$$

$$q = \tilde{q} + \ \overline{q} \tag{3.12}$$

A high pass filter is used to extract the harmonic componens from the p and q signals. In the next step the reference current in $\alpha\beta$ co-ordinates is calculated by Eq. (3.13).

$$\begin{bmatrix} i_\alpha * \\ i_\beta * \end{bmatrix} = \frac{1}{{v_\alpha}^2 + \ {v_\beta}^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} * \begin{bmatrix} p \\ q \end{bmatrix} \tag{3.13}$$

In the final step the reference current in *abc* co-ordinates is calculated by using Eq. (3.14).

$$\begin{bmatrix} i_{ca}* \\ i_{cb}* \\ i_{cc}* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} * \begin{bmatrix} i_0* \\ i_\alpha* \\ i_\beta* \end{bmatrix} \tag{3.14}$$

3.4 Synchronous Reference Frame Theory

It is another time domain method for generation of reference current. This theory is commonly used due to simplicity and easy implementation. The real currents in synchronous reference frame are obtained by performing co-ordinate transformation. This method also requires a PLL to estimate frequency and phase of the grid voltage thus synchronizing it with the ac mains voltage. This technique is also known as d-q theory. The fundamental component is extracted by using a low-pass filter. The performance of this method is best under normal grid conditions but the presence of grid disturbances affects the accuracy of PLL circuitry used by this theory. Thus the reference current obtained is also not accurate. This theory also requires a lot of voltage and current transducers.

Fig. 3.4 shows the block diagram of d-q theory. The $sin\theta$ and $cos\theta$ represents the synchronized reference signals. Four transformation blocks are used to get the reference current. Harmonics current can be obtained by doing transformation from *abc* stationary reference frame to rotating *dq* frame. Finally the reference current is obtained by transforming back from *dq* to *abc* [161].

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{3.15}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} sin\,(\theta) & -cos\,(\theta) \\ cos\,(\theta) & sin\,(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha* \\ i_\beta* \end{bmatrix} \tag{3.16}$$

Where θ is the transformation angle and is given by Eq. (3.17).

$$\theta = \int_0^t \omega(t)dt + \theta_0 \tag{3.17}$$

Where $\omega = 2\pi f$ is the angular frequency of supply and θ_0 is the inintial value of phase.

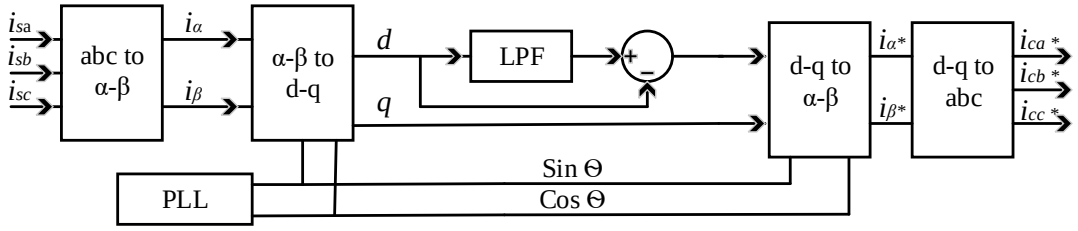

FIGURE 3.4: Block Diagram of SRF Theory

This equation contains both AC and DC components. The AC component contains harmonics and is blocked by a low pass filter so that output of the above equation which only contains DC component becomes harmonics free Eq. (3.18).

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \overline{i_{\mathrm{d}}} + \widetilde{i_{\mathrm{d}}} \\ \overline{i_q} + \widetilde{i_q} \end{bmatrix} \tag{3.18}$$

The reference currents in d-q frame are given by Eq. (3.19).

$$\left\{ \begin{array}{c} i_{dref} = -\widetilde{i_d} \\ i_{qref} = -(\overline{i_q} + \widetilde{i_d}) \end{array} \right\} \tag{3.19}$$

Eq. (3.20) and Eq. (3.21) are used to do the back transformation and obtaining the signal in abc stationery frame.

$$\begin{bmatrix} i_\alpha * \\ i_\beta * \end{bmatrix} = \begin{bmatrix} sin\,(\theta) & -cos\,(\theta) \\ cos\,(\theta) & sin\,(\theta) \end{bmatrix} \begin{bmatrix} i_{dref} \\ i_{qref} \end{bmatrix} \tag{3.20}$$

$$\begin{bmatrix} i_{ca}* \\ i_{cb}* \\ i_{cc}* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{\alpha}* \\ i_{\beta}* \end{bmatrix} \tag{3.21}$$

3.5 Discrete Fourier Transform

The Discrete Fourier Transform method is a frequency-domain method that can be used to extract the harmonics if a regular pattern of current is available. In this method FFT algorithm is used to acquire the harmonics present in the load current. FFT is a powerful tool for harmonic analysis in active power filters. In this method voltage transducers are not required and also no PLL circuitry is required for estimation of frequency and phase. This technique has a drawback of slow dynamic response due to large amount of parallel computations and also it fails to generate the reference current precisely if noise is present in the current samples. The DFT technique is sensitive to frequency fluctuations and its performance will severely degrade under frequency drifts. The block diagram of this method is shown in Fig. 3.5. The three phase load currents are represented by i_{La}, i_{Lb} and i_{Lc} and the reference currents by $i_{ca}*$, $i_{cb}*$ and $i_{cc}*$ respectively.

In the Fourier analysis block frequency components of the load current are detected. In the second stage fundamental component is separated and the remaining frequency components are added to get the harmonics current waveform. In the final stage harmonics current waveform is 180° phase shifted to get the reference current. The DFT of an input sequence x(n) is given by Eq. (3.22).

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi k \frac{n}{N}} \tag{3.22}$$

The real and imaginary parts are calculated by Eq. (3.23) and Eq. (3.24).

$$RealPart = \sum_{n=0}^{N-1} x(n) \cos(2\pi k \frac{n}{N}) \tag{3.23}$$

$$ImaginarPart = \sum_{n=0}^{N-1} x(n) \sin(2\pi k \frac{n}{N}) \tag{3.24}$$

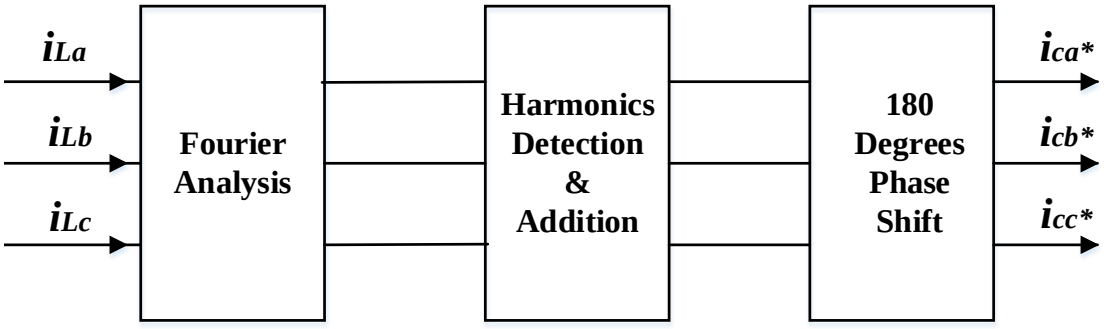

FIGURE 3.5: Block Diagram of DFT

3.6 Performance Evaluation

The three techniques overviewed in this chapter are evaluated for different loads under Matlab/Simulink environment. In the first step a non-linear load is connected to a three phase three wire system. The load current is measured and fed to the reference current generation block. In the second step reference current block extract the harmonics and generate it's anti phase waveform. In the final step this reference current is added to the load current to make it sinusoidal. THD of the waveform thus obtained confirms the accuracy of the technique used.

The simulink model used for simulation of reference current generation techniques is shown in Fig. 3.6 . The voltage and distorted current signals are given as input to the transformation blocks. The accuracy of the reference current is evaluated by adding this current to the distorted source current. The sum of these two waveforms should produce a pure sinusoidal waveform.

Table 3.1 shows the parameters of three different loads and the respective THD values of the distorted source current. These loads are used for evaluating the reference current generation techniques.

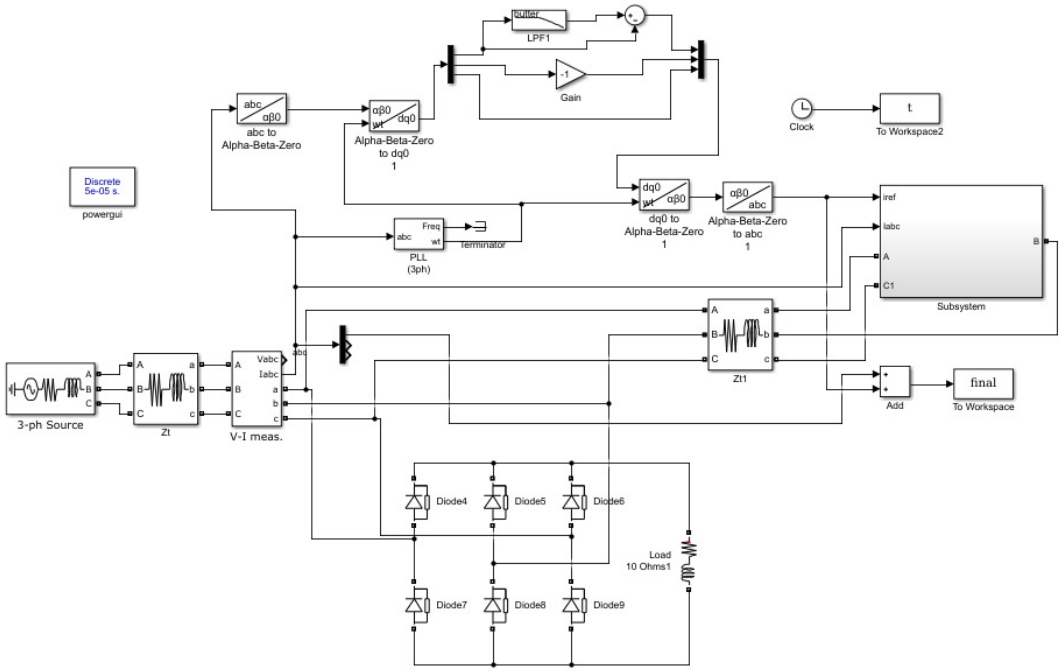

FIGURE 3.6: Simulink Model for Reference Current Generation

TABLE 3.1: Load Parameters.

Simulation Case	**THD before compensation**	**Output Loads**
I	30.18%	R=10 Ω
II	35.63%	R=10 Ω , L=10 mH
III	53.08%	R=10 Ω, L=10 mH, C=200uF

3.6.1 Case 1

In this case only resistor is used as output load for simulation. Fig. 3.7 represents the load current waveform and the plot showing its THD is given in Fig. 3.8. Reference current is generated first by using the p-q technique discussed above and is shown in Fig. 3.9. Techniques presented in this section are evaluated only by adding the reference current and the load curent. The resultant waveform should have sinusoidal waveshape to prove the accuracy of the implemented technique. Furthermore, a low value of THD will also confirm the effectiveness of the applied

technique as shown for case 1 in Fig. 3.10.

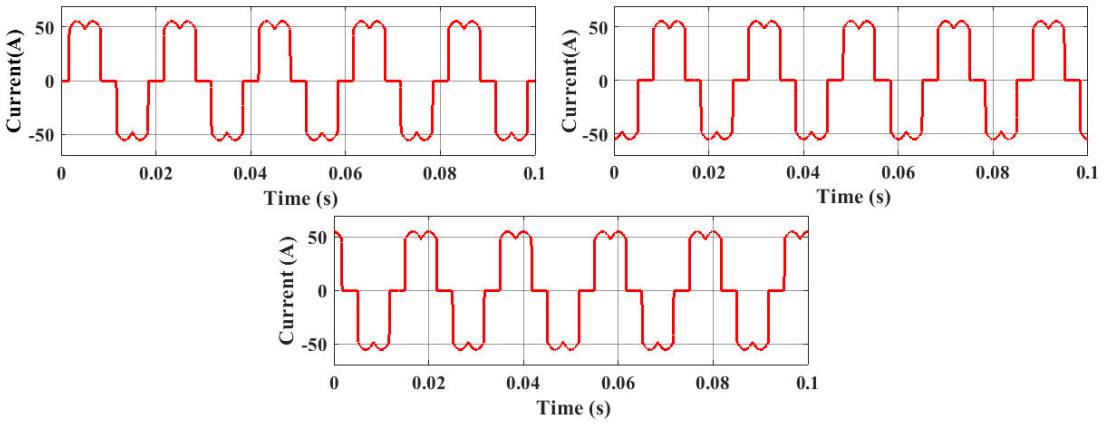

FIGURE 3.7: Three Phase Load Current Waveform for case 1

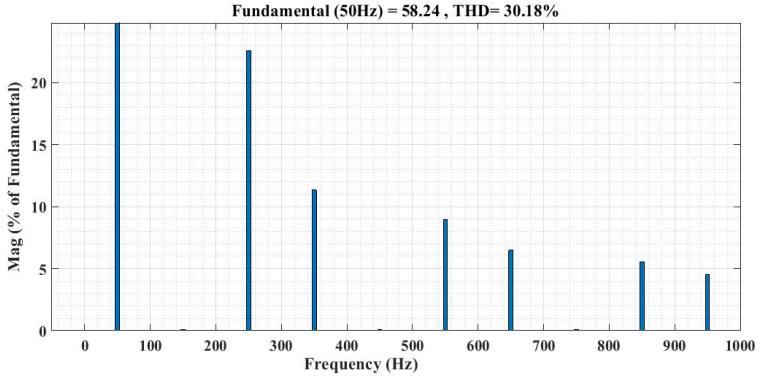

FIGURE 3.8: THD of load current (phase A)

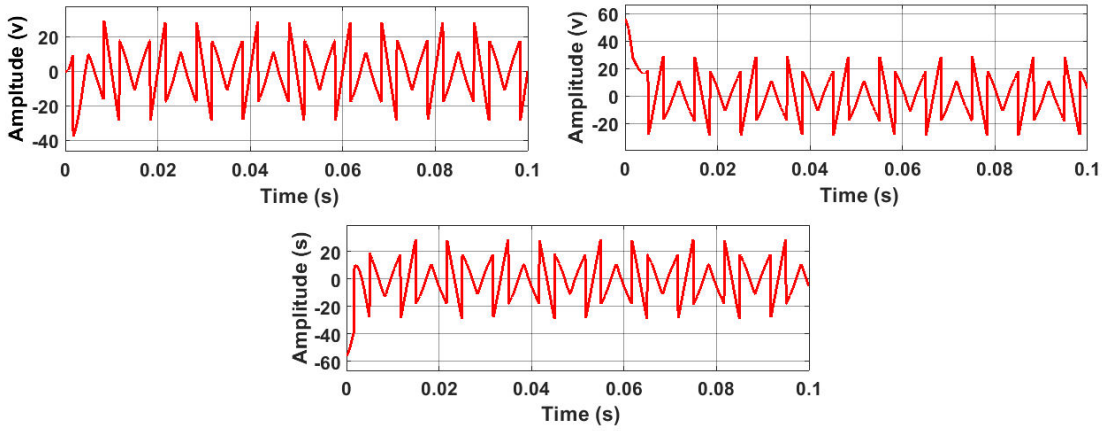

FIGURE 3.9: p-q theory based reference current for case 1

Another technique discussed in the section that is the d-q theory is tested in simulation and the waveform obtained is shown in Fig. 3.11 and the corresponding THD plot of the compensated current waveform is shown in Fig. 3.12.

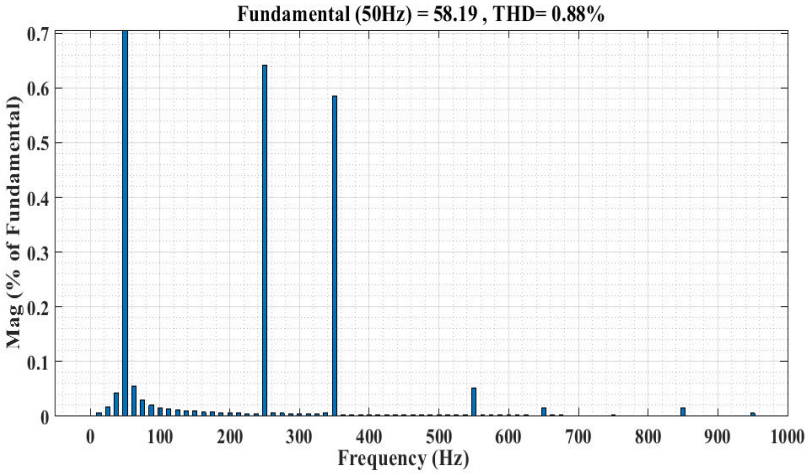

FIGURE 3.10: THD result for p-q theory (case 1)

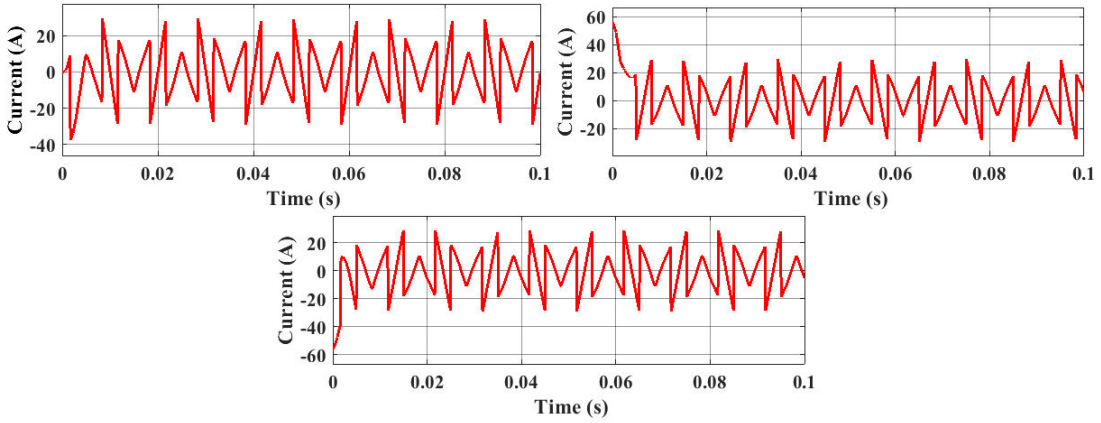

FIGURE 3.11: d-q theory based reference current for case 1

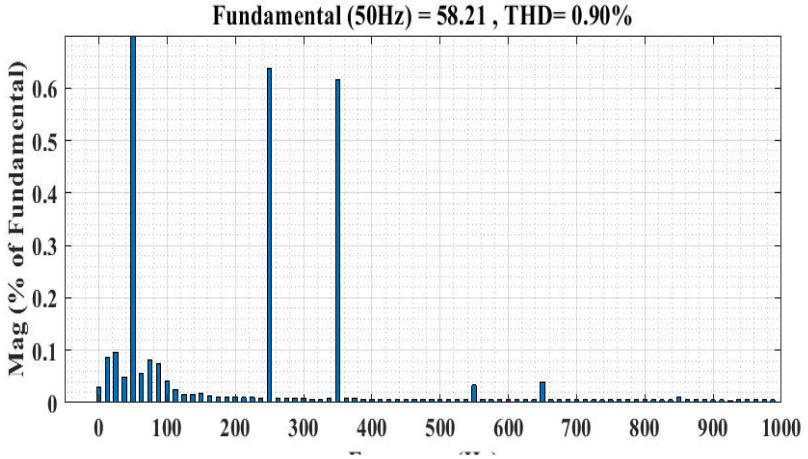

FIGURE 3.12: THD result for d-q theory (case 1)

Finally DFT method is applied to generate the reference current for resistive load and is shown in Fig. 3.13. The THD result can be seen in Fig. 3.14.

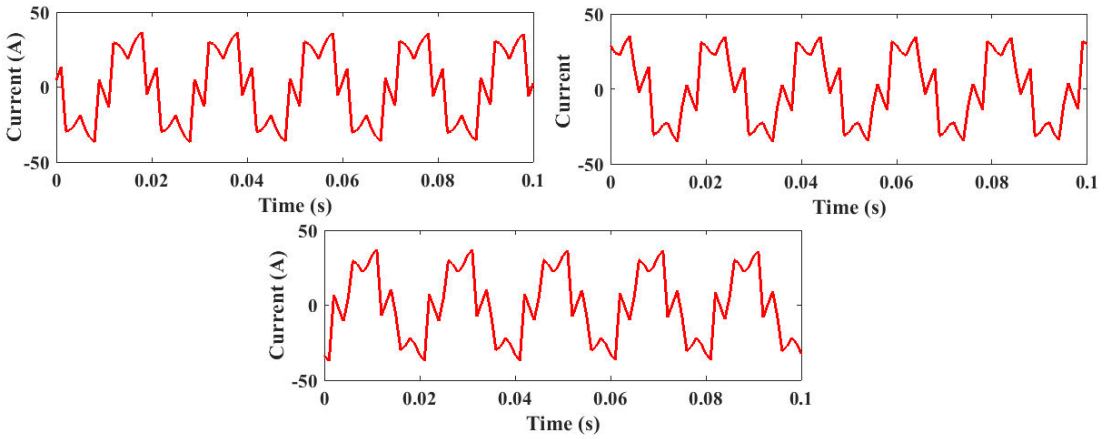

FIGURE 3.13: DFT based reference current for case 1

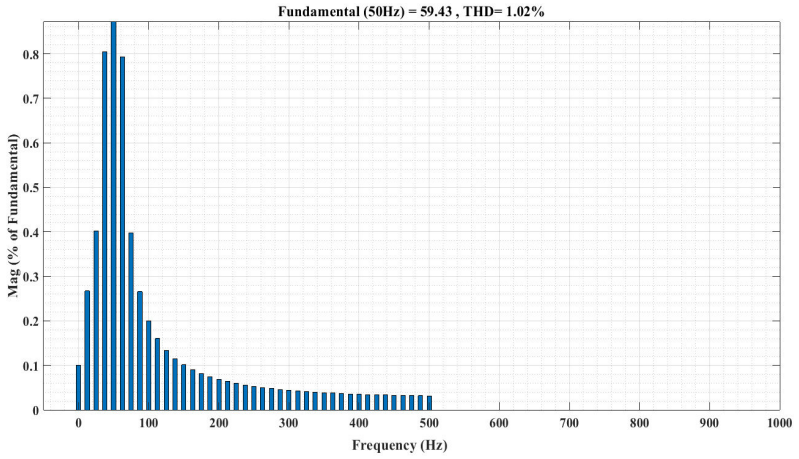

FIGURE 3.14: THD result for DFT technique (case 1)

3.6.2 Case 2

In this case an RL load is used for simulation and the resultant waveform for this load is shown in Fig. 3.15. The harmonic distortion present in the load current is represented by THD plot of Fig. 3.16. Case 2 of the load parameters is repeatedly simulated for each technique as done in first case. The reference current waveform obtained after applying p-q theory is shown in Fig. 3.17. This waveform is again added to the load current waveform to make it sinusoidal and the reduced level of harmonics distortion can be verified from the THD plot of Fig. 3.18.

The reference current obtained after applying d-q theory for RL load is shown in Fig. 3.19 and the reduced THD of the current waveform obtained after addition of referrence current and load current is shown in Fig. 3.20.

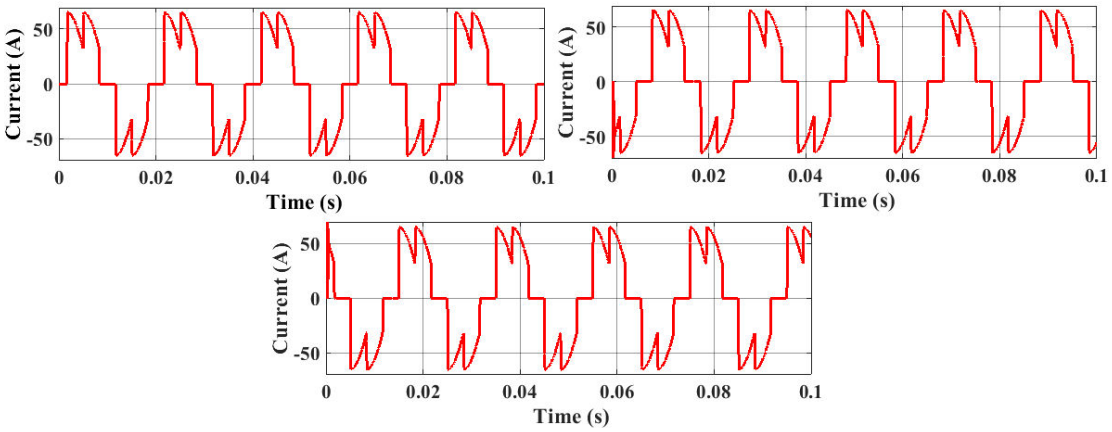

FIGURE 3.15: Three phase Load current waveform for case 2

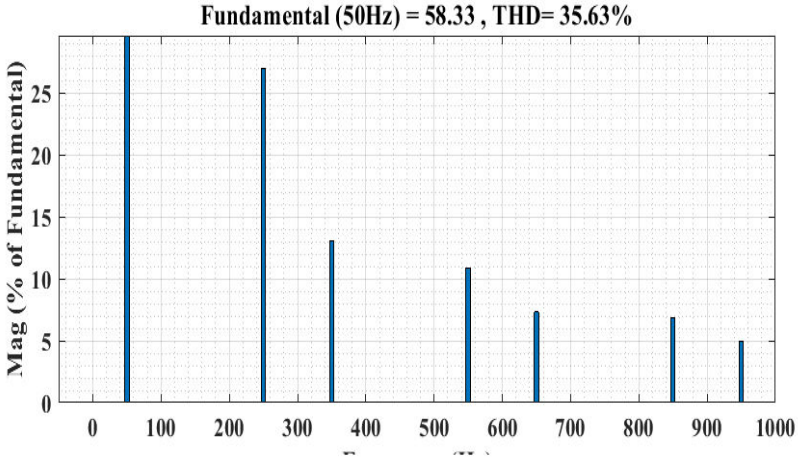

FIGURE 3.16: THD of load current for case 2

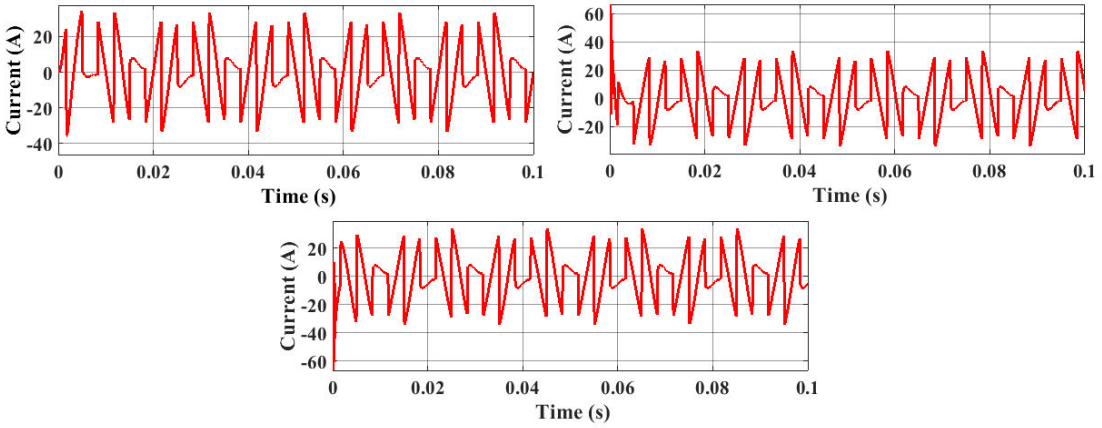

FIGURE 3.17: p-q theory based reference current for case 2

For case 2 the last simulation result is obtained by implementing DFT technique and the resultant waveform is shown in Fig. 3.21. The reduced THD level of the resultant current can be seen in Fig. 3.22.

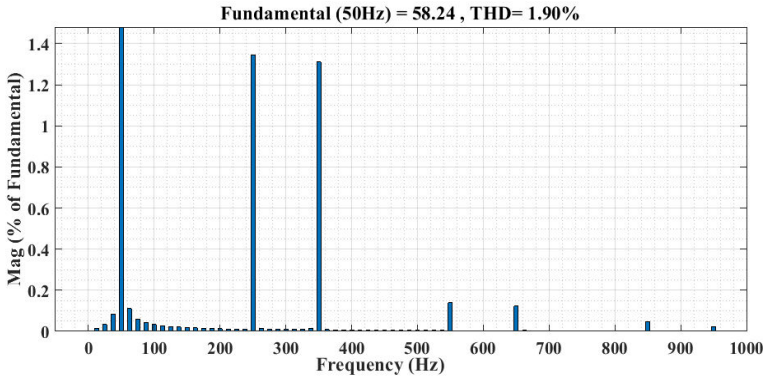

FIGURE 3.18: THD result of p-q theory (case 2)

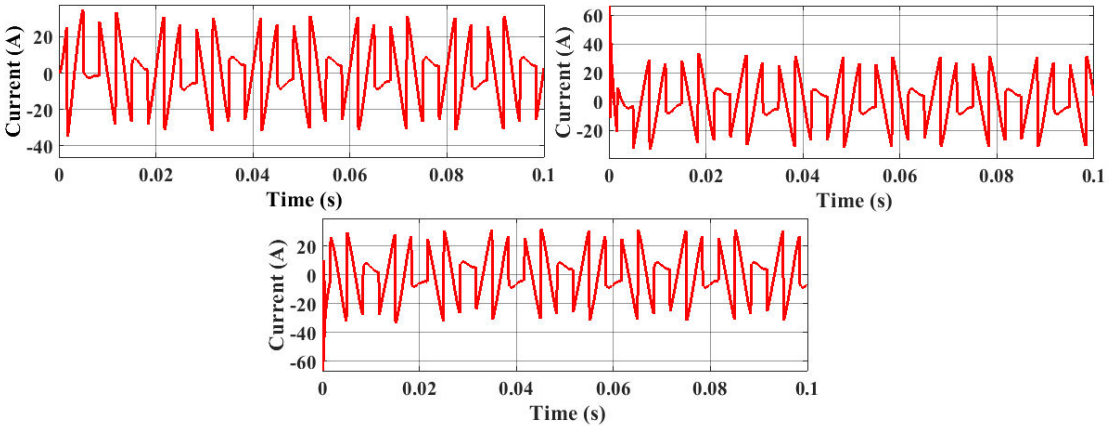

FIGURE 3.19: d-q theory based reference current for case 2

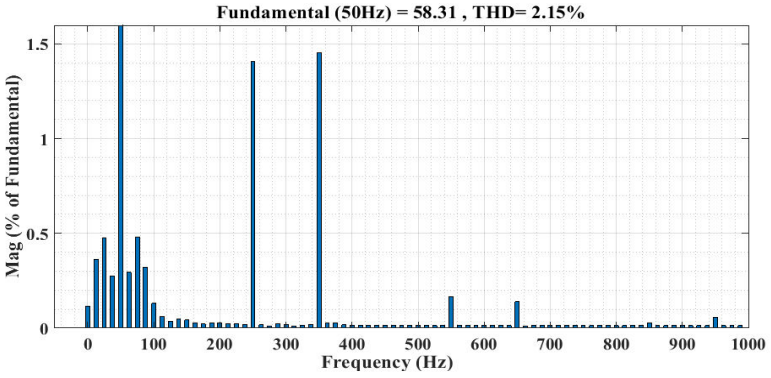

FIGURE 3.20: THD result of d-q theory (case 2)

3.6.3 Case 3

In the third case an RLC load is used. The load current waveform for this case is shown in Fig. 3.23 and its respective THD plot can be seen in Fig. 3.24. The circuit is simulated again by first using p-q technique. Fig. 3.25 displays the generated reference current. This current waveform is again added to the load

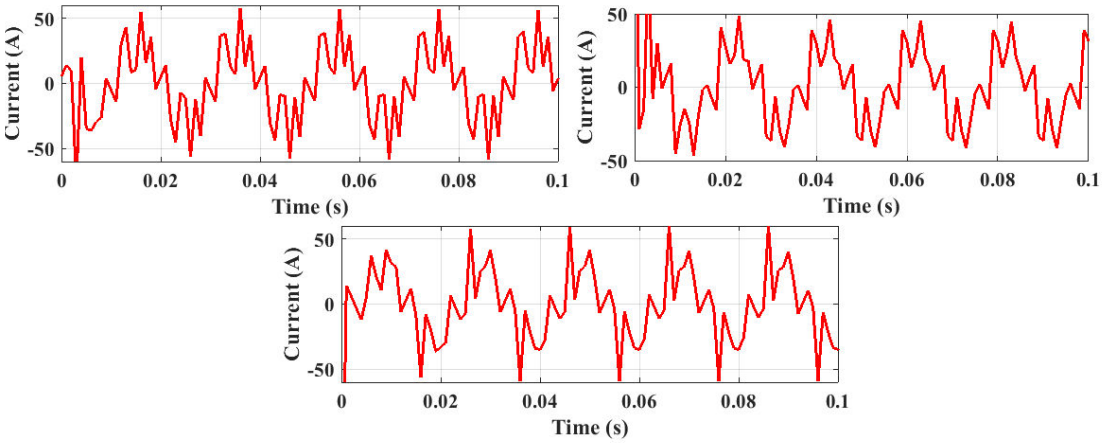

FIGURE 3.21: DFT based reference current for case 2

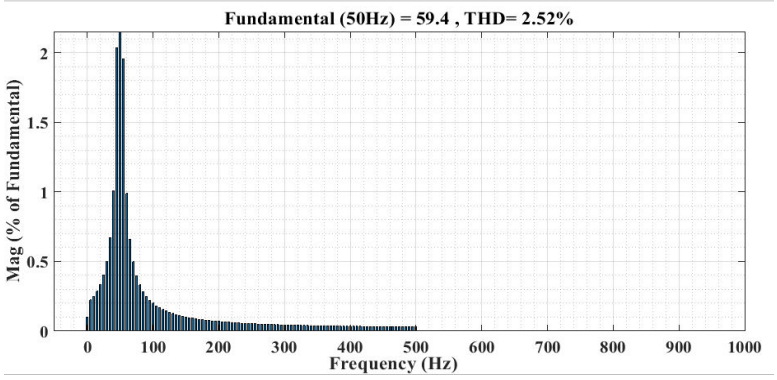

FIGURE 3.22: THD result of DFT (case 2)

current waveform to make it sinusoidal. THD of the resulting waveform is shown in Fig. 3.26.

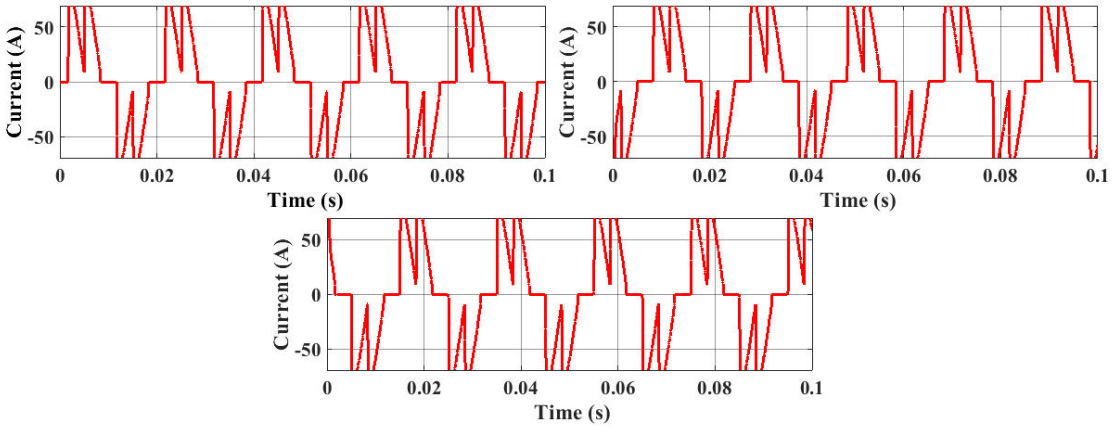

FIGURE 3.23: Three phase load current for case 3

Fig. 3.27 represents the waveform of reference current obtained using d-q method and the reduced THD after compensation is shown in Fig. 3.28.

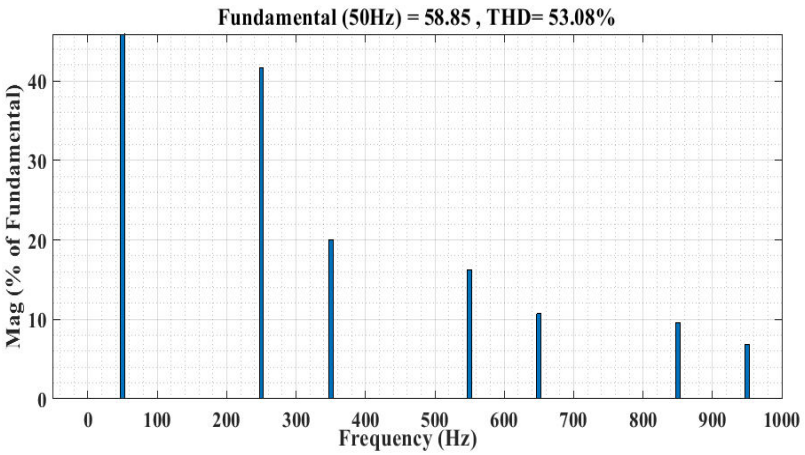

FIGURE 3.24: THD after compensation (p-q theory) for case 3

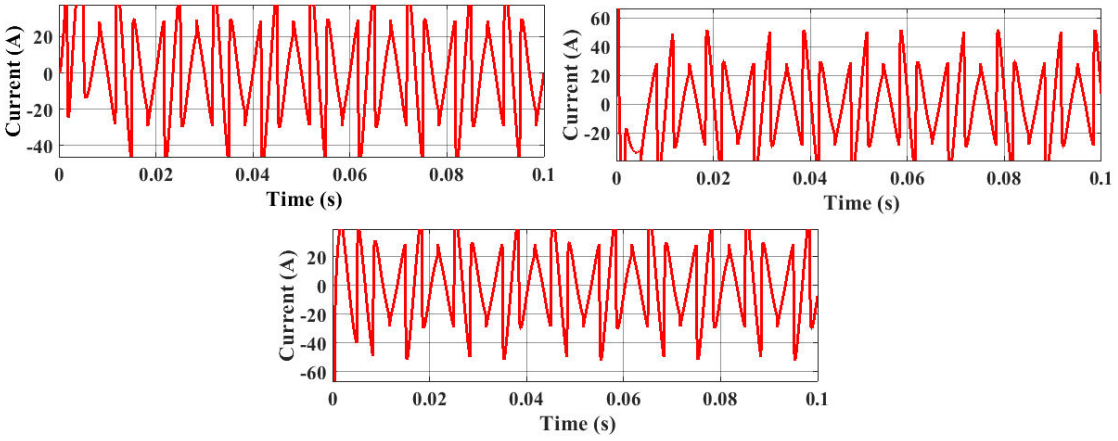

FIGURE 3.25: p-q theory based reference current for case 3

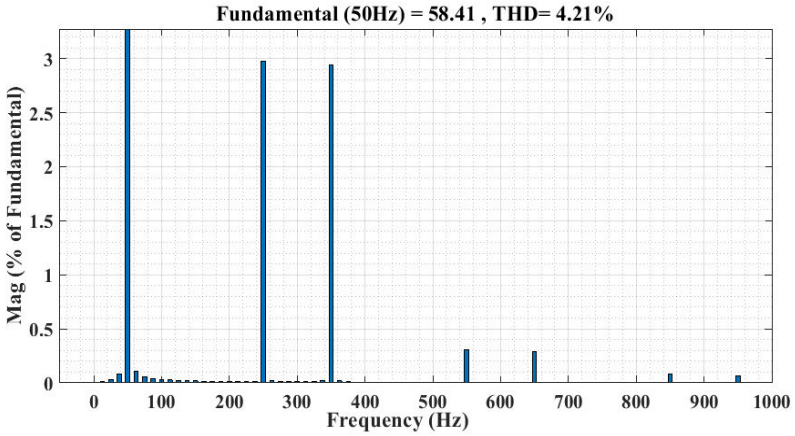

FIGURE 3.26: THD result of p-q theory (case 3)

Finall the DFT technique is applied to get the reference current waveform shown in Fig. 3.29. THD of the load current waveform obtained after addition of the reference current is shown in Fig. 3.30.

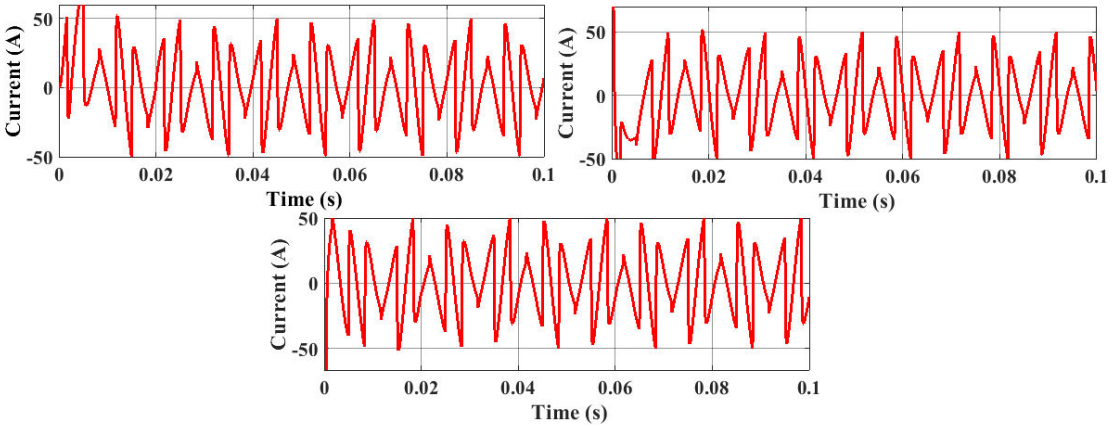

FIGURE 3.27: d-q theory based reference current for case 3

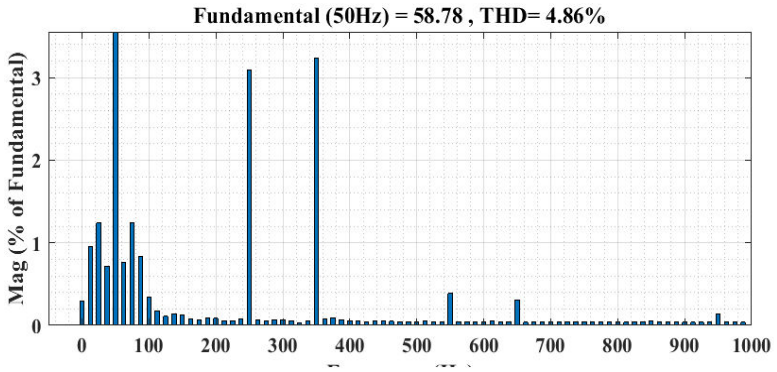

FIGURE 3.28: THD result of d-q theory (case 3)

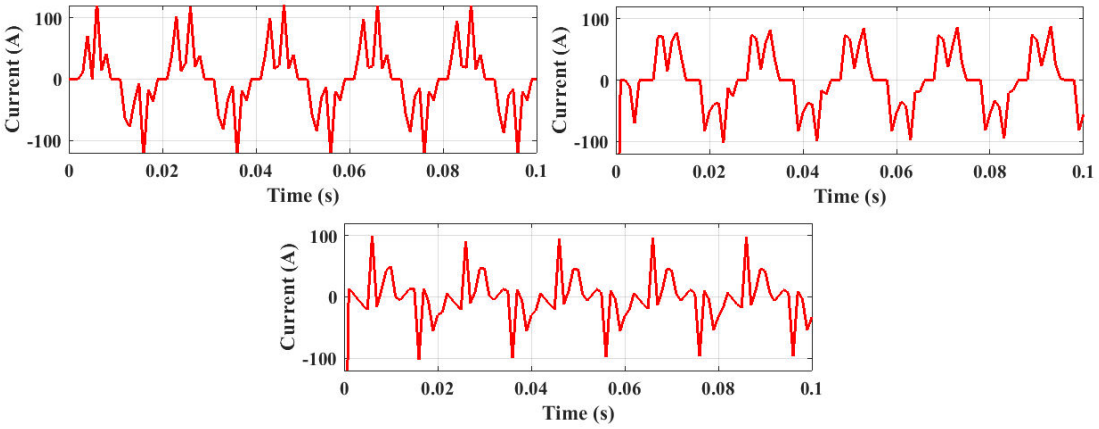

FIGURE 3.29: DFT based reference current for case 3

3.7 Results

The results obtained for the three methods are summarized in Table 3.2. Although the obtained results verify the effectiveness of all the three techniques under three cases of simulation but the effect of grid disturbances on the performance of these

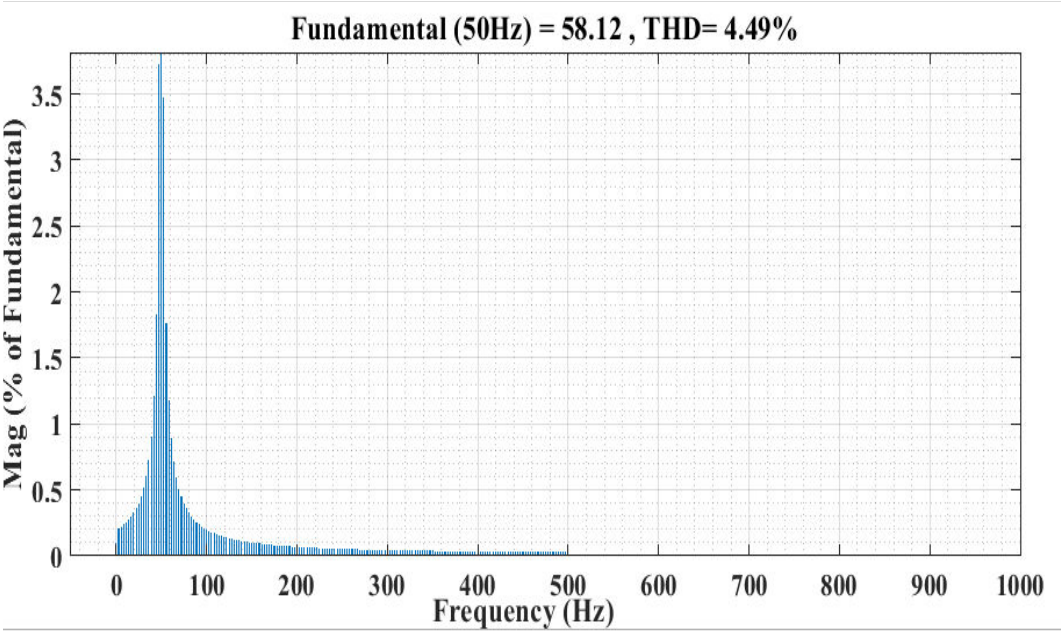

FIGURE 3.30: THD result of DFT (case 3)

TABLE 3.2: THD Results.

Simulation Case	**THD before compensation**	**THD after compensation**		
		p-q	d-q	DFT
I	30.18%	0.88%	0.9%	1.02%
II	35.63%	1.90%	2.15%	2.52%
III	53.08%	4.21%	4.86%	4.49%

techniques is not taken into account. In chapter 5 the effects of grid disturbances will also be considered for performance evaluation. The modified SRF theory is also simulated here for RL load and results are compared with some previous research articles like [60] that uses SRF theory for reference current generation and RL load is connected across the three phase bridge rectifier. THD of the load current was reduced from 18.93% to 0.95%. In [143] a control based on a non-linear function is implemented for SAPF and THD of the load current was reduced from 18.2% to 1.32%. These results are shown in Table 3.3. It is proved that the proposed technique has better results in terms of THD reduction as compared to given references.

TABLE 3.3: Comparison with Previous Work

Technique	**THD before Compensation**	**THD after Compensation**
[60] using SRF technique	18.93%	0.95%
[143] using DQ reference frame	18.2%	1.32%
Proposed Technique	30.18%	0.9%

3.8 Summary

In this chapter the concept of reference current in active power filtering is presented. Both time domain and frequency domain techniques are studied and simulations are also performed to evaluate these techniques for different loads. A mathematical model of SAPF is developed initially to simplify the theoretical analysis of discussed techniques.

Time domain techniques have been proved to have good performance in terms of harmonics reduction and dynamic response. The synchronous reference frame theory (d-q) uses a conventional PLL circuit to estimate frequency and phase. Under normal grid conditions the role of PLL in reference current estimation is not very important but the existence of grid disturbances like frequency drift, phase angle jump and dc offset badly affects the generation of reference current. In the next chapter the control strategies used for current injection are studied and evaluated for performance.

Chapter 4

Current Injection Control

4.1 Introduction

After the successful generation of reference current, it must be injected precisely at PCC to complete the process of active power filtering. This will make the distorted source current sinusoidal. The job of current injection controller is to force the actual compensating current to follow the reference current by generating gate pulses of VSI. Thus the performance of SAPF is highly dependent on the controller used for current injection. The process of current injection is also dependent on the regulation of DC link voltage and therefore, it is explained before introducing the current injection techniques. The techniques over viewed will also be evaluated for performance under various loads.

4.2 DC Link Voltage Control

In SAPF, the extracted harmonic current with opposite phase is injected at PCC to ensure correction of the distorted source current. DC-link capacitor and VSI are the main parts of APF power stage design. This configuration of power stage is considered as a low cost and efficient solution. The current injection through VSI is accomplished by using the stored energy of DC-link capacitor. A part of the

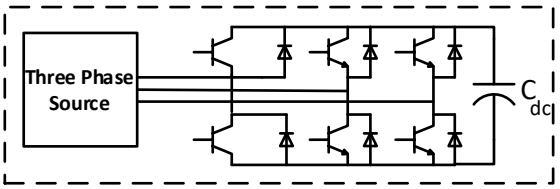

FIGURE 4.1: DC Link Capacitor connected to VSI.

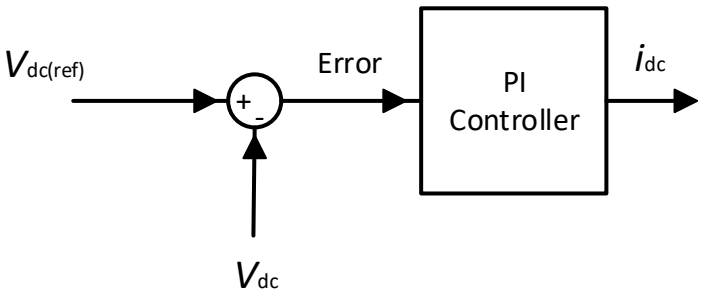

FIGURE 4.2: DC link voltage controller.

APF structure showing the DC link capacitor connected across the VSI is shown in Fig. 4.1.

The PI control technique is adopted here for regulation which processes the error between the actual and reference voltage. This concept is displayed in Fig. 4.2.

The flow of active power must be controlled. Injection currents can only be accurately generated by keeping the DC-link voltage of SAPF at required value, thus improving the mitigation performance of SAPF. This is achieved by adding a PI controller branch to the d axis in dq frame, thus controlling the active current component. This small amount of active current is regulated by the current controller to keep the DC link capacitor voltage constant. For this purpose, the actual DC link voltage is detected and is fed to the PI controller along with the reference value.

The voltage regulation process is completed by keeping the real power drawn by SAPF equal to losses occurred due to switching of IGBT's . This is achieved by adjusting the magnitude of reference current appropriately through the control of i_{dc} which is generated by the PI controller after processing the error. This process

will make the SAPF to draw an accurate amount of real power to compensate its potential losses.

The capacitor energy is represented by Eq. (4.1).

$$E = \frac{1}{2} C_{dc} \; {v_{dc}}^2 \tag{4.1}$$

The DC link capacitor will be charged from the same supply that powers the load. The capacitor needs to be charged to a higher voltage magnitude than the maximum peak of the supply voltage. Thus it is charged to a pre-set value selected as a reference to ensure correct operation of the filter. The way the capacitor is charged is similar to a boost circuit. The VSC circuit uses inductor to boost up the voltage.

The fundamental component of the output voltage of VSI must be higher than the peak value of supply voltage to ensure reactive power compensation by APF. The appropriate size of the capacitor could be determined from Eq. (4.2) and the power (Q) across the capacitor can be calculated using Eq. (4.3) [162]. If an electrolytic capacitor is used, value of capacitance should be greater than 2000uf due to its current ripple rating. The capacitance value should be selected to reduce the voltage ripple less than 0.5% in a conventional design [163]. Mathematical representation of DC link capacitance is given below:

$$i_f = C_{dc} \frac{dv_{dc}}{dt} \tag{4.2}$$

$$Q = i_f \; v_{dc} \tag{4.3}$$

Putting value of i_f to get Eq. (4.4)

$$Q = (C_{dc} \frac{dv_{dc}}{dt}) \; v_{dc} \tag{4.4}$$

Eq. (4.4) can be rearranged to find C_{dc} using Eq. (4.5)

$$C_{dc} = \frac{Q}{(\frac{dv_{dc}}{dt}) \; v_{dc}} \tag{4.5}$$

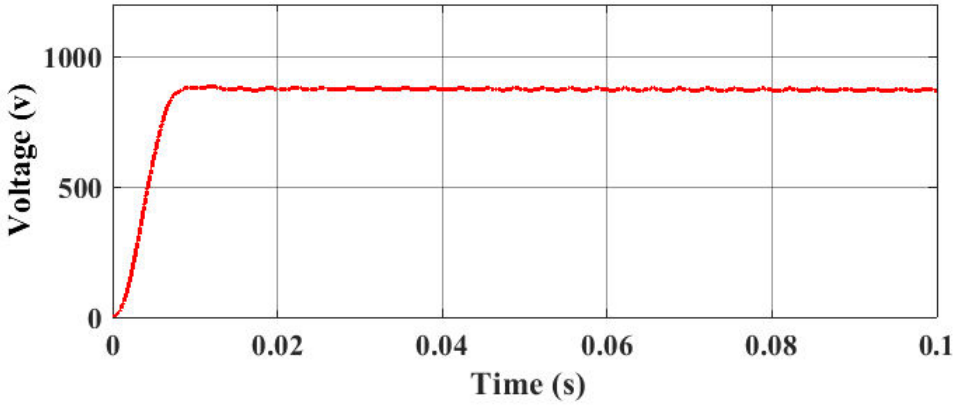

FIGURE 4.3: DC link voltage plot.

The voltage error E_r and the DC charging current i_{dc} can be obtained by using Eq. (4.6) and Eq. (4.7) thus giving summary of the control approach.

$$Er = v_{dc(ref)} - v_{dc} \tag{4.6}$$

$$i_{dc} = Er(Kp + Ki \int dt) \tag{4.7}$$

The idea is to maintain a power balance that is accomplished by making the real power of supply to be equal to the sum of real power of load and losses of inverter. SAPF draws a real power throughout its switching operation and needs to be controlled in order to regulate the DC link voltage. Thus it is made equal to its switching losses to complete the regulation process. The process involves adjusting the magnitude of the reference current, so that the SAPF can draw a precise amount of real power to compensate its potential losses. The output of PI controller is proportional to the instantaneous power balance changes. In order to ensure accurate injection of current the minimum DC bus voltage should be more than double of the peak of the phase voltage of the system. The reference DC link voltage is set as 800v and after the implementation of PI controller the plot of DC link voltage is shown in Fig. 4.3.

The small amount of real power flowing into the dc capacitor is adjusted to regulate the DC link voltage, thus conduction and switching losses are compensated. The electrolytic capacitor value is appropriately selected to avoid the transient changes

in the dc voltage. The transient changes in the instantaneous power causes voltage fluctuations. Thus the choice of proper capacitor value is also important for controlling the amplitude of these voltage fluctuations.

4.3 Single Band Hysteresis Current Control

The most common method used for current injection in APF is Single-band hysteresis current control. In this method the actual current is limited within a band to follow the reference current. Two boundaries equally displaced from the reference are set in order to limit the actual current. A fixed hysteresis band is set and the controller senses the error between actual current and reference current and comparing it with the set band to generate gating signals of VSI. This technique has the benefits of simplicity, good accuracy and robustness. Fig. 4.4 shows the basic idea of hysteresis current control in which two levels of hysteresis function are shown. The hysteresis technique is applied to each phase separately. The band is set with a lower and upper limit. Simultaneous switch on of switches of any leg of the inverter is not allowed by the controller to prevent short circuit across the dc link voltage supply. Similarly, the simultaneous switch off of switches of any leg of the inverter may result in undefined states. When the actual current increases than the reference current and reaches the upper band, the current should be decreased. Similarly, when the actual current becomes less than the reference current and reaches the lower band limit, the current should be increased. Consequently, the current is retained within the hysteresis band to follow the reference current. Taking into consideration the gating signal combinations, eight standard switching states are thus obtained as shown in Table 4.1. The currents for all the three phases are injected at the PCC according to the respective reference currents by using switching states of Table 4.1. The sum of injected currents of all the phases will be zero at any point as shown in Eq. (4.8) [164].

$$i_{ca} + i_{cb} + i_{cc} = 0 \tag{4.8}$$

TABLE 4.1: Standard switching states for VSI.

State	**State No**	**Switch states**	$\boldsymbol{v}_{ab}$	$\boldsymbol{v}_{bc}$	$\boldsymbol{v}_{ca}$	$\boldsymbol{i}_{ca}$	$\boldsymbol{i}_{cb}$	$\boldsymbol{i}_{cc}$
S1,S2 and S6 = 1 S4,S5 and S3 = 0	1	100	v_{dc}	0	-v_{dc}	i_{dc}	- $i_{ca/2}$	- $i_{ca/2}$
S2,S3 and S1 = 1 S5,S6 and S4 = 0	2	110	0	v_{dc}	-v_{dc}	$i_{dc/2}$	$i_{dc/2}$	- i_{dc}
S3,S4 and S2 = 1 S6,S1 and S5 = 0	3	010	-v_{dc}	v_{dc}	0	- $i_{cb/2}$	i_{dc}	- $i_{cb/2}$
S4,S5 and S3 = 1 S1,S2 and S6 = 0	4	011	-v_{dc}	0	v_{dc}	- i_{dc}	$i_{dc/2}$	$i_{dc/2}$
S5,S6 and S4 = 1 S2,S3 and S1 = 0	5	001	0	-v_{dc}	v_{dc}	- $i_{cb/2}$	- $i_{cb/2}$	i_{dc}
S6,S1 and S5 = 1 S3,S4 and S2 = 0	6	101	v_{dc}	-v_{dc}	0	$i_{dc/2}$	- i_{dc}	$i_{dc/2}$
S1,S3 and S5 = 1 S4,S6 and S2 = 0	7	111	0	0	0	0	0	0
S4,S6 and S2 = 1 S1,S3 and S5 = 0	8	000	0	0	0	0	0	0

The injected currents for all the three phases at any instant using PWM technique, will be represented mathematically by Eq. (4.9), Eq. (4.10) and Eq. (4.11).

$$i_{ca}=\frac{v_{dc}\sqrt{k_a}-v_{sa}\angle\theta}{\sqrt{R^2+(\omega L)^2}} \tag{4.9}$$

$$i_{cb}=\frac{v_{dc}\sqrt{k_b}-v_{sb}\angle\theta}{\sqrt{R^2+(\omega L)^2}} \tag{4.10}$$

$$i_{cc}=\frac{v_{dc}\sqrt{k_c}-v_{sc}\angle\theta}{\sqrt{R^2+(\omega L)^2}} \tag{4.11}$$

Where k_a, k_b and k_c represents the duty cycle of PWM for the three phases. The values of injected currents will be different from the standard table in order to follow the reference current. Fig. 4.5 represents the injected currents with

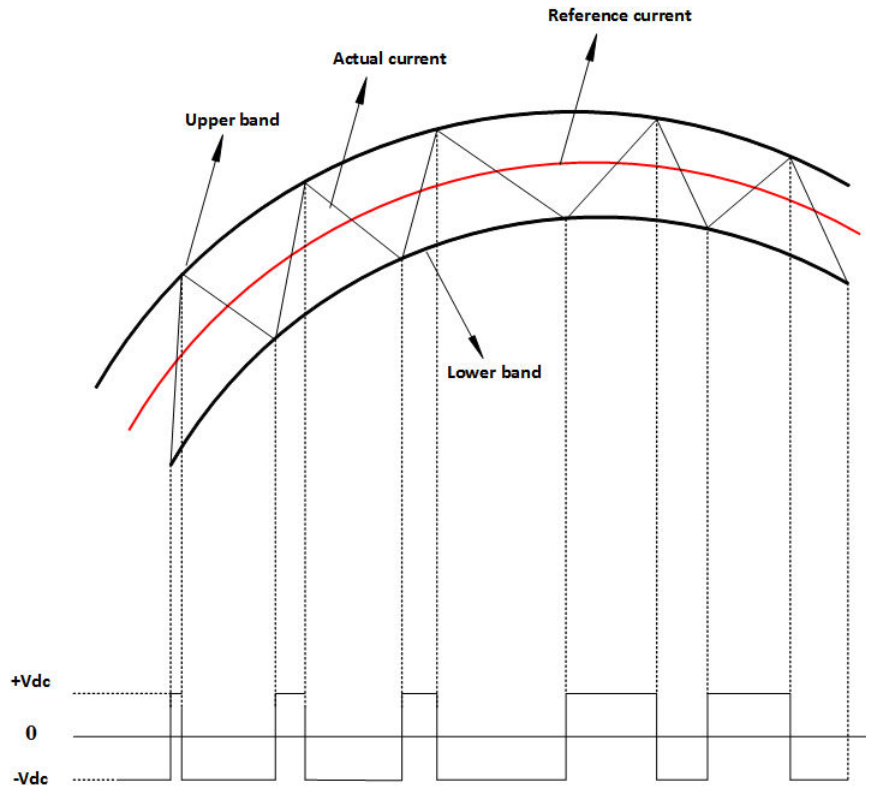

FIGURE 4.4: Hysteresis switching (SBHCC)

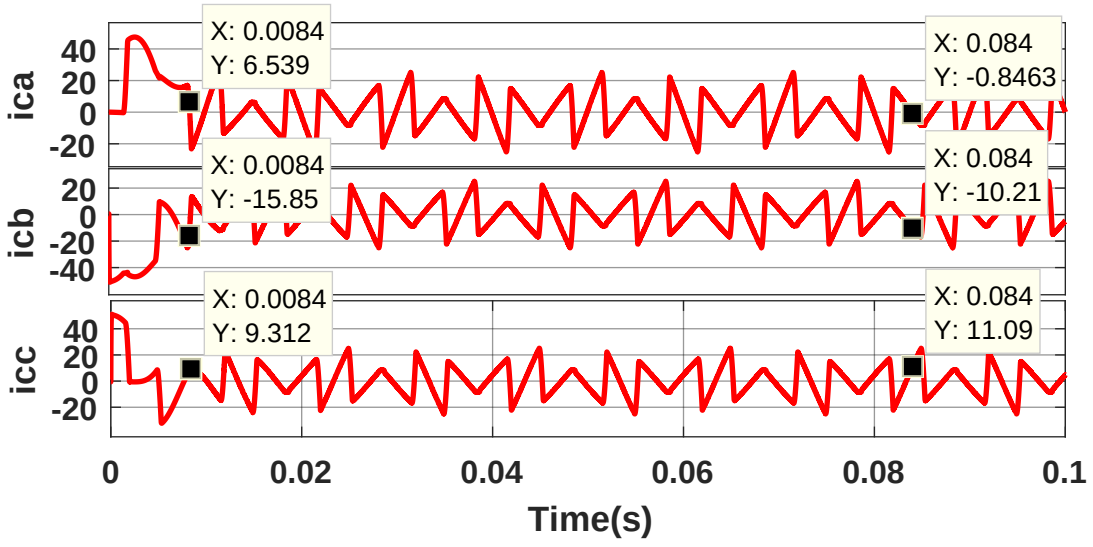

FIGURE 4.5: Three phase injected currents.

TABLE 4.2: Calculated injected currents

Injected currents	**Marker 1**	**Marker 2**
i_{ca}	+6.539	-0.8463
i_{cb}	-15.85	-10.21
i_{cc}	+9.312	+11.09
$i_{ca}+i_{cb}+i_{cc}$	0	0

markers and values are given in Table 4.2. The switch on time for phase A can be calculated by Eq. (4.12)

$$T_{on} = \frac{2hL}{V_{dc} - V_s} \tag{4.12}$$

Similarly, the switch off time is given by Eq. (4.13).

$$T_{off} = \frac{2hL}{V_{dc} + V_s} \tag{4.13}$$

The switching period in case of SBHCC is computed by Eq. (4.14) and Eq. (4.15).

$$T_{s1} = T_{on} + T_{off} \tag{4.14}$$

$$T_{s1} = \frac{4V_{dc}hL}{\left({V_{dc}}^2 - {V_s}^2\right)} \tag{4.15}$$

Finally, the switching frequency is determined by Eq. (4.16).

$$f_{s1} = \frac{\left({V_{dc}}^2 - {V_s}^2\right)}{4V_{dc}hL} \tag{4.16}$$

Where

f_{s1} = Switching frequency

V_{dc} = DC link voltage

L = Output load inductor

V_s = Supply voltage

h = Hysteresis band.

4.4 Double Band Hysteresis Current Control

In this control technique the hysteresis band is divided into two parts. One part is implemented for positive error that is the actual current is either equal to or greater than the reference current and the second part is implemented for negative error that is the actual current is less than the reference current.

Fig. 4.6 shows the basic idea of DBHCC in which a little difference exists with reference to SBHCC. The operation of the double-band hysteresis control directly depends on the error. The upper switch for any phase leg of the inverter is turned ON and OFF during a half-cycle meant for positive error while the lower switch remains continuously OFF during that period. Similarly, for the second half-cycle meant for negative error, an opposite phenomenen as compared to first half cycle is addopted for the lower and upper switch. Such type of switching will result in a lower value of average switching frequency as compared to the SBHCC scheme without changing the parameters. In this case the switch ON time is given by Eq. (4.17).

$$T_{on} = \frac{hL}{V_{dc} - V_s} \tag{4.17}$$

Similarly, the switch off time is given by Eq. (4.18).

$$T_{off} = \frac{hL}{V_s} \tag{4.18}$$

The switching period in the half cycle is computed by Eq. (4.19) and Eq. (4.20).

$$T_{s2} = T_{on} + T_{off} \tag{4.19}$$

$$T_{s2} = \frac{V_{dc} hL}{(V_{dc} - V_s)\, V_s} \tag{4.20}$$

The switching period in one cycle is computed by Eq. (4.21).

$$T_{s2} = \frac{2V_{dc} hL}{(V_{dc} - V_s)\, V_s} \tag{4.21}$$

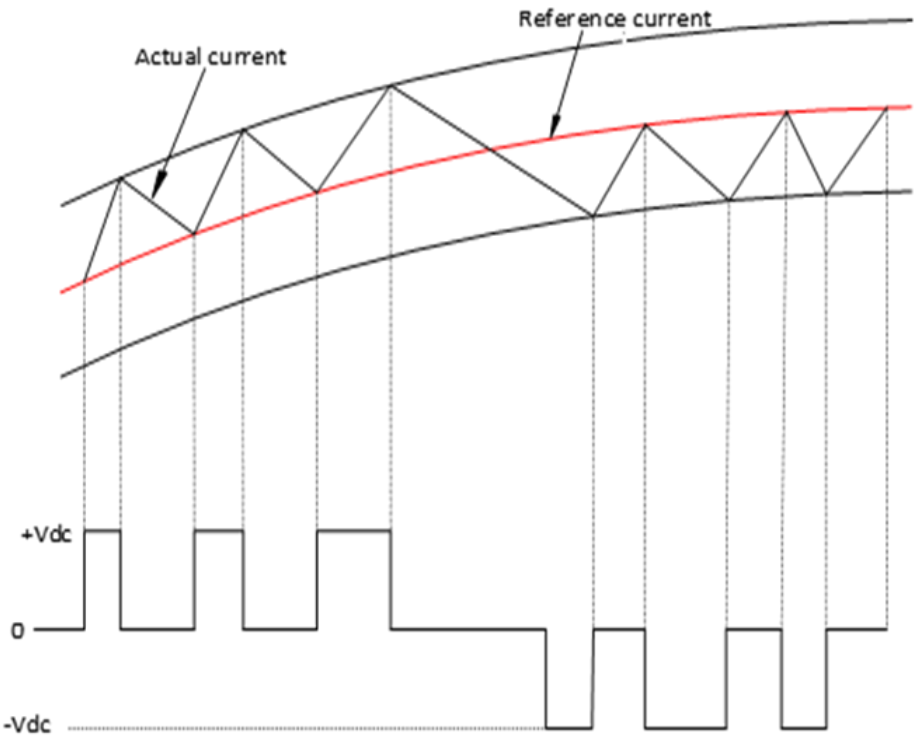

FIGURE 4.6: Hysteresis switching (DBHCC)

TABLE 4.3: Calculated Switching frequencies

Hysteresis band (h)	**SBHCC f_{s1}(kHz)**	**DBHCC f_{s2}(kHz)**
0.1	86.04	55.41
0.2	43.20	27.70
0.3	28.68	18.47
0.4	21.51	13.85
0.5	17.20	11.08

Finally, the switching frequency is determined by Eq. (4.22)

$$f_{s2} = \frac{(V_{dc} - V_s)\, V_s}{2V_{dc}hL} \tag{4.22}$$

The calculated switching frequencies of both SBHCC and DBHCC for different values of hysteresis band are shown in Table 4.3 and we can see that for all values of hysteresis band the DBHCC scheme has lesser switching frequency.

4.5 Sliding Mode Control

"Sliding mode control is a nonlinear control method which changes the dynamics of a nonlinear system by application of a discontinuous control". Since the APF system is a nonlinear system, SMC method is known to be a best method to generate switching pulses for VSI. In this section SMC will be applied to control the injection current.

"The sliding mode control is the motion of state variables under the sliding surface. The state variables of the system can converge to the equilibrium point in steady state condition".

After the creation of sliding surface, the trajectories are enforced to reach sliding surface in finite time and stay there for the rest of time. After reaching the sliding surface the system dynamics are unaffected by circuit parameters and only depend on the selected sliding surface.

SMC can be designed basically in two steps. In first step a suitable sliding surface is designed and the second step includes the formulation of a control law to bring the system trajectories on the sliding surface and make them stay there. For the APF, control input is represented by U and it has two components, a continuous component U_{eq} and the discontinuous one U_n as shown in Eq. (4.23).

$$U = U_{eq} + U_n \tag{4.23}$$

The function of the discontinuous component is to bring the system on sliding surface and the continuous component ensures the system to be there. In *d-q* frame the control can be expressed by Eq. (4.24).

$$U_{dq} = U_{eq,dq} + U_{n,dq} \tag{4.24}$$

Where

$$U_{dq} = \begin{Bmatrix} U_d \\ U_q \end{Bmatrix}, U_{eq,dq} = \begin{Bmatrix} U_{eq,d} \\ U_{eq,q} \end{Bmatrix} and \;\; U_{n,dq} = \begin{Bmatrix} U_{n,d} \\ U_{n,q} \end{Bmatrix}$$

4.5.1 Sliding Surface Design

In general form the sliding surface can be written as Eq. (4.25).

$$S = K\left(x - x^*\right) \tag{4.25}$$

Where

$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix}, \; x^* = \begin{bmatrix} {x_1}^* \\ {x_2}^* \\ {x_3}^* \end{bmatrix} = \begin{bmatrix} {i_{cd}}^* \\ {i_{cq}}^* \\ {v_{dc}}^* \end{bmatrix} \; and \; K = \begin{bmatrix} k_{ic} & 0 & k_{vd} \\ 0 & k_{ic} & k_{vq} \end{bmatrix}$$

The sliding surface on *d-q* frame is given by Eq. (4.26) while U_{nd} and U_{nq} are given by Eq. (4.27).

$$S = \begin{bmatrix} S_d \\ S_q \end{bmatrix} = \begin{bmatrix} k_{ic}\left(i_{cd} - {i_{cd}}^*\right) + k_{vd}(v_{dc} - {v_{dc}}^*) \\ k_{ic}\left(i_{cq} - {i_{cq}}^*\right) + k_{vq}(v_{dc} - {v_{dc}}^*) \end{bmatrix} \tag{4.26}$$

$$Un, d = \begin{cases} -sgn\left(S_d\right), & S_d \neq 0 \\ 0 \quad , & S_d = 0 \end{cases}$$

$$Un, q = \begin{cases} -sgn\left(S_q\right), & S_q \neq 0 \\ 0 \quad , & S_q = 0 \end{cases} \tag{4.27}$$

The mathematical model described in section 3 is used to develop the equivalent control on *d-q* frame. Eq. (4.28) represents the general form of state variable model of SAPF.

$$\dot{x} \; = Ax + B\left(x\right)u + G \tag{4.28}$$

Where A, B and G are obtained as shown in Eq. (4.29).

$$\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{R}{L} & \omega & 0 \\ -\omega & -\frac{R}{L} & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{[A]} \begin{bmatrix} i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{v_{dc}}{L} & 0 \\ 0 & \frac{v_{dc}}{L} \\ -\frac{i_{cd}}{C_{dc}} & \frac{i_{cq}}{C_{dc}} \end{bmatrix}}_{[B]} \begin{bmatrix} f_d \\ f_q \end{bmatrix} + \underbrace{\begin{bmatrix} -\frac{v_d}{L} \\ 0 \\ 0 \end{bmatrix}}_{[G]} \tag{4.29}$$

The equivalent control can be found by setting the derivative of the sliding surface to zero and substituting U= U_{eq} to get Eq. (4.30)

$$\left.\begin{array}{c} \dot{S} = K\left(\dot{x} - \dot{x^*}\right) = 0 \\ 0 = K\left(Ax + B\left(x\right)U_{eq} + G\right) - K\dot{x^*} \\ \left(KB\left(x\right)\right)^{-1}.K\left(\dot{x^*} - Ax - G\right) = \left(KB\left(x\right)\right)^{-1}.KB(x)U_{eq} \\ U_{eq} = \left(KB\left(x\right)\right)^{-1}.K\left(\dot{x^*} - Ax - G\right) \end{array}\right\} \tag{4.30}$$

4.5.2 Stability Analysis

The stability analyses are performed to ensure that the system trajectory reaches the equilibrium point (EP) and settles there. This is true for a stable system but for the unstable system the trajectory does not settle at the EP but crosses it and moves toward infinity. In this section stability analysis of SMC are performed by adopting a Lyapunov function as a candidate function as shown in Eq. (4.31)

$$V = \frac{1}{2}S^2 \tag{4.31}$$

The time derivative of Eq. (4.31) is written Eq. (4.32).

$$\dot{V} = S\dot{S} \tag{4.32}$$

Eq. (4.33) describes the general condition of SMC.

$$\dot{V} = S\dot{S} < 0 \tag{4.33}$$

The time derivative of Eq. (4.25) results in Eq. (4.34).

$$\dot{S} = K\left(Ax + B\left(x\right)\left(U_{eq,dq} - sgn\left(S_{dq}\right)\right) + G - \dot{x^*}\right) \tag{4.34}$$

Eq. (4.34) can be simplified by making an assumption that no external disturbances are present and initial values are set to zero. Thus Eq. (4.35) is obtained.

$$\dot{S} = KB\left(x\right).\left(-sgn\left(s\right)\right) \tag{4.35}$$

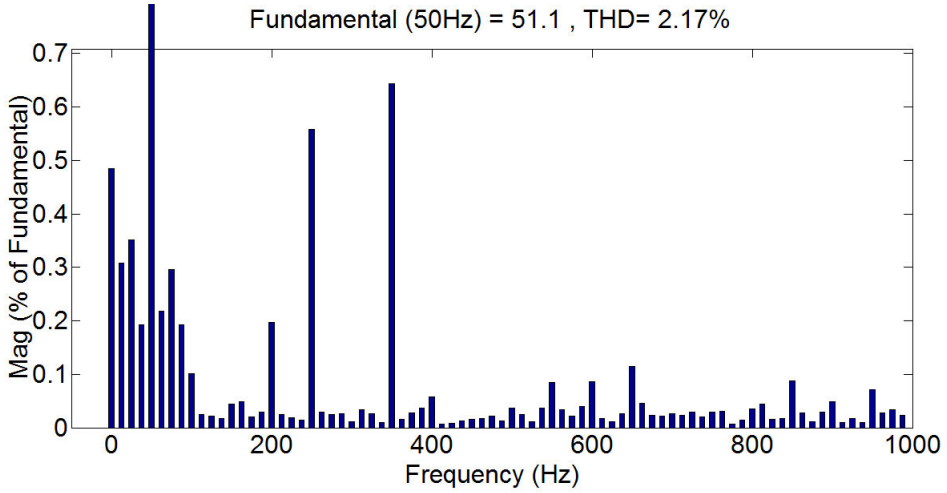

FIGURE 4.7: THD using SBHCC (case 1).

The sliding mode gains can be selected by putting Eq. (4.26) and Eq. (4.35) into Eq. (4.33) as shown Eq. (4.36).

$$\frac{L}{C_{dc}}.\left(k_{vd}+k_{vq}\right).\left(|i_{cd}|+|i_{cq}|\right) < \ k_{ic}v_{dc} \tag{4.36}$$

Where k_{ic} is the current gain, k_{vd} and k_{vq} are the voltage gains in dq frame as described by gain matrix given in Eq. (4.25).

4.6 Performance Evaluation of Current Injection Techniques

The techniques overviewed in the begining of this chapter are evaluated under three different loads. The simulation parameters are the same as used for evaluation of reference current generation techniques in chapter 3. In the first case only resistive load is used and the reference current is injected using the three techniques. The corresponding THD after compensation is shown in Fig. 4.7, Fig. 4.8 and Fig. 4.9. In the second case RC load is used for simulation and the current is injected again using the three techniques. The achieved results in terms of THD reduction are shown in Fig. 4.11, Fig. 4.12 and Fig. 4.13. Finally, for case 3 a capacitor is

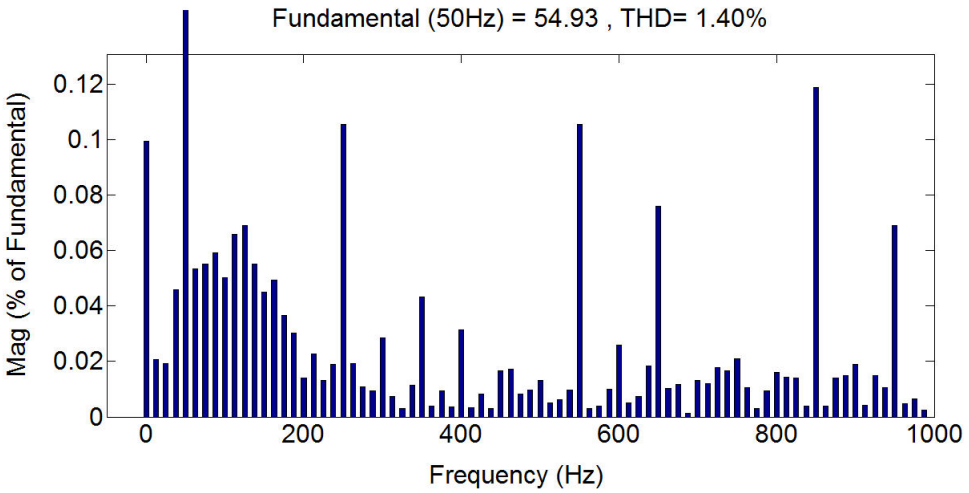

FIGURE 4.8: THD using DBHCC (case 1).

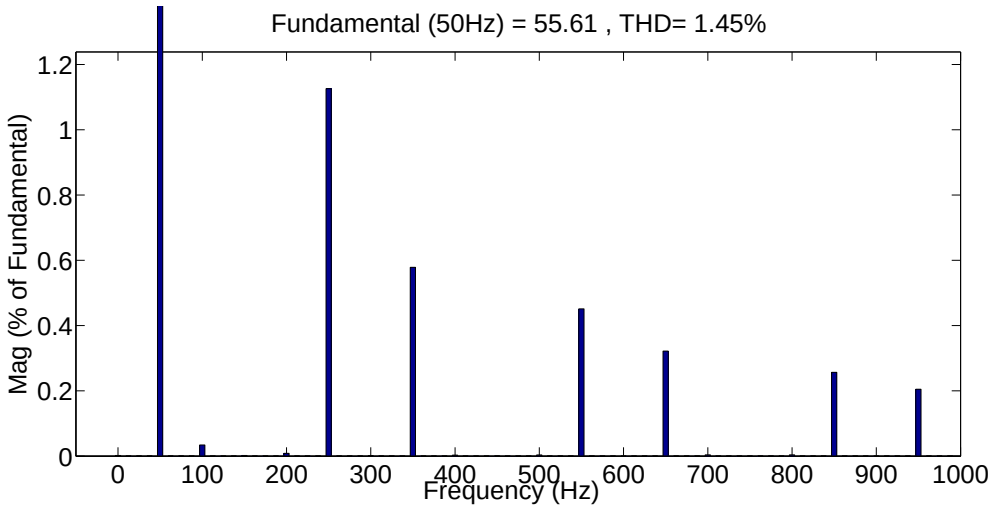

FIGURE 4.9: THD using SMC (case 1).

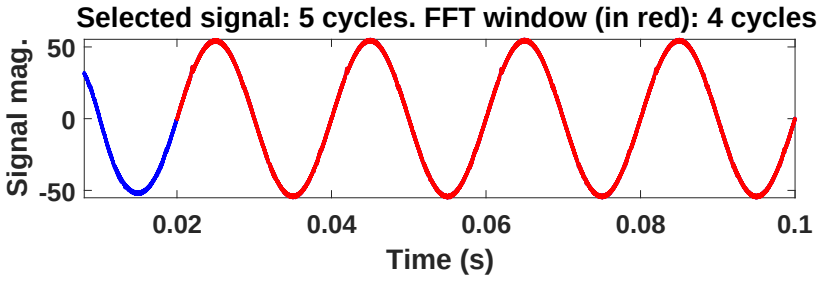

FIGURE 4.10: Source current after compensation (case 1).

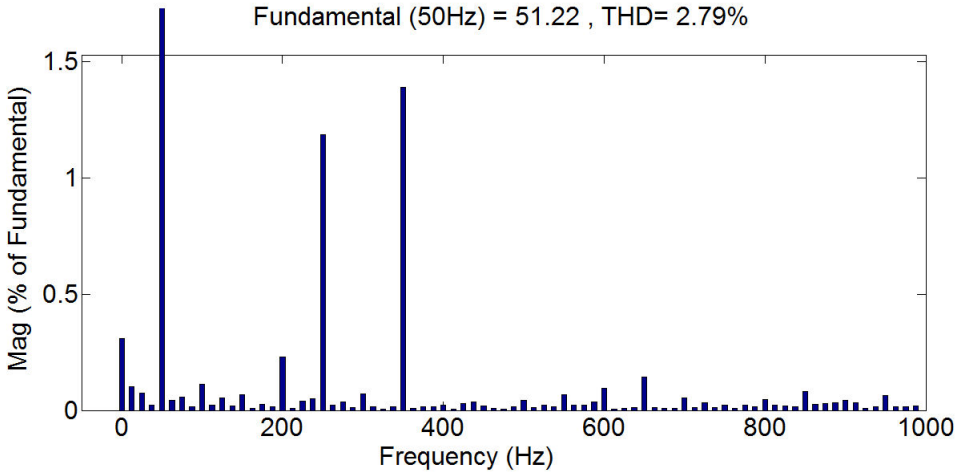

FIGURE 4.11: THD using SBHCC (case 2).

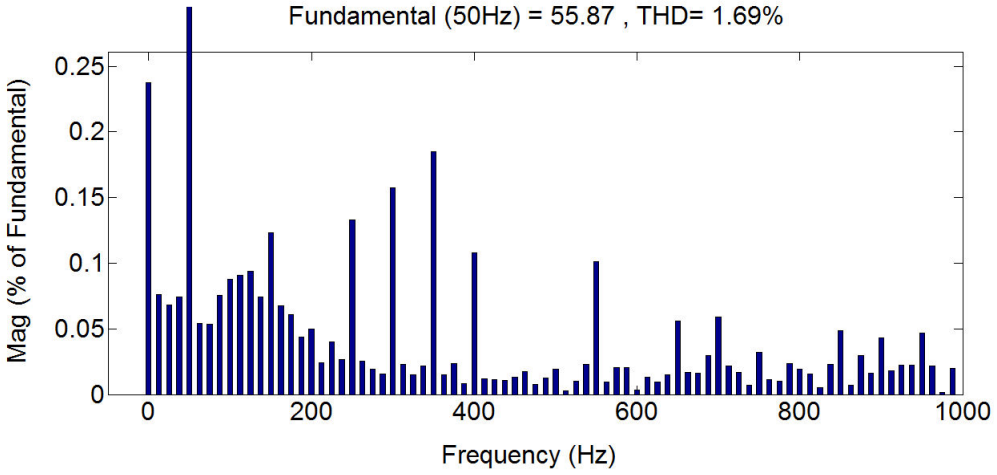

FIGURE 4.12: THD using DBHCC (case 2).

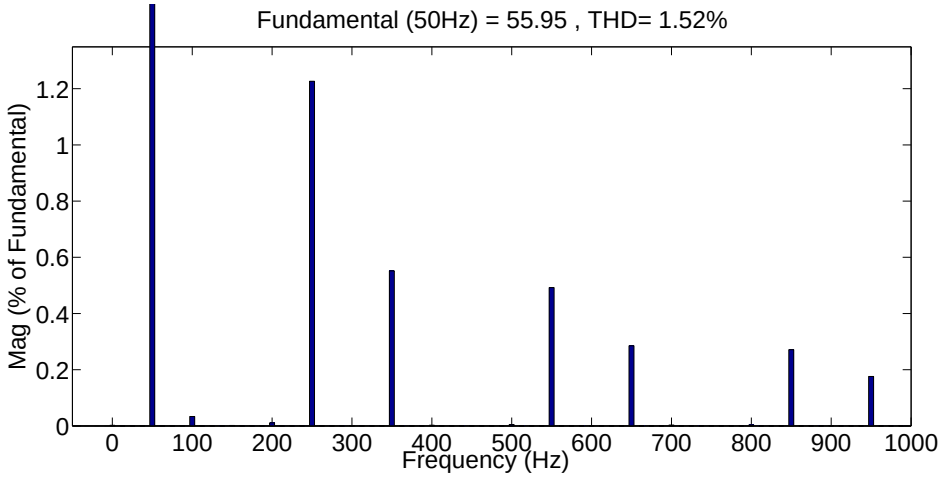

FIGURE 4.13: THD using SMC (case 2).

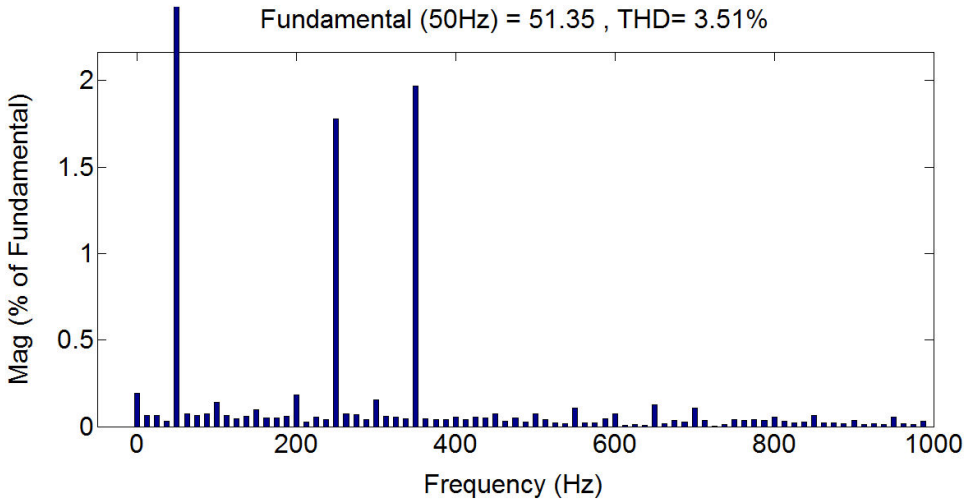

FIGURE 4.14: THD using SBHCC (case 3).

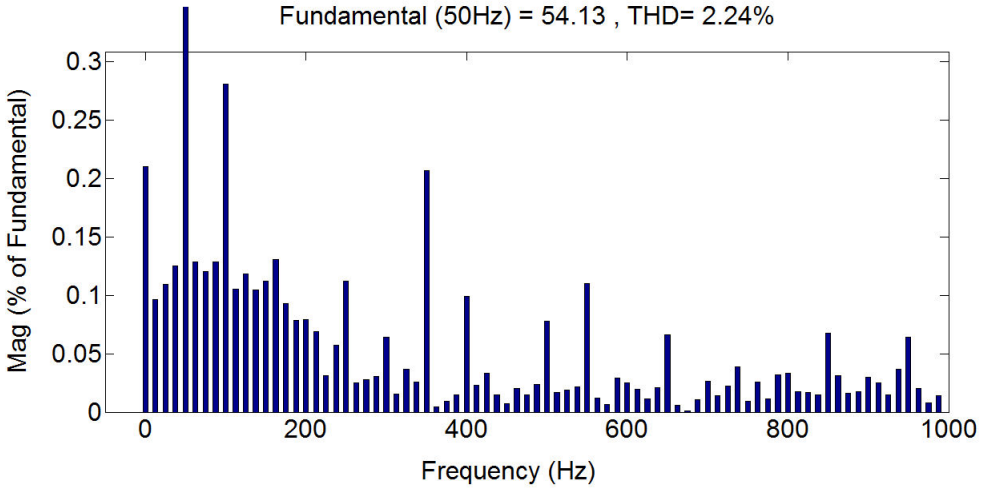

FIGURE 4.15: THD using DBHCC (case 3).

connected across the resistor to evaluate the control strategy. The THD plots for all the control strategies under observation are shown in Fig. 4.14, Fig. 4.15 and Fig. 4.16.

The results achieved during simulation are summarized in Table 4.4.

4.7 Summary

In this chapter the current injection part of active power filter has been studied in detail. DC link voltage control, a part of injection process is also explained.

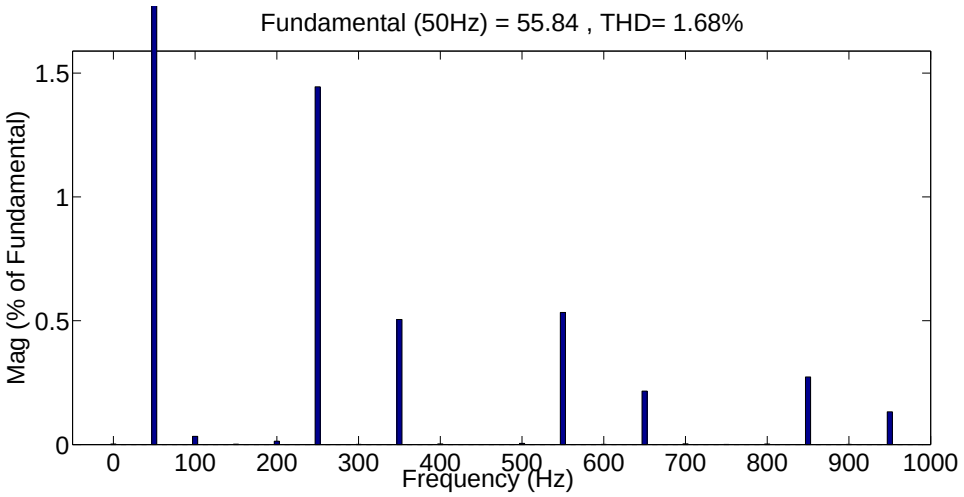

FIGURE 4.16: THD using SMC (case 3).

TABLE 4.4: Performance Parameters

Load	**THD before compensation**	**THD after compensation**		
		SBHCC	DBHCC	SMC
Case 1	30.18%	2.17%	1.40%	1.45%
Case 2	35.63%	2.79%	1.69%	1.52%
Case 3	53.08%	3.51%	2.24%	1.68%

Three control techniques are overviewed and their performance is compared under various loads. The sliding mode control has been proved as better technique for current injection at PCC.

In the next chapter synchronization techniques will be analyzed under various grid disturbances and the impact of these techniques on the synchronization of active power filter will be examined.

Chapter 5

Synchronization of Active Power Filter

Some of the techniques used for reference current generation like SRF theory require precise information of the voltage phase and frequency for accurate estimation of reference current. It is easier to estimate frequency and phase under normal grid conditions but it is a challenging job under adverse grid conditions. For this purpose, phase locked loop (PLL) techniques are used. This chapter initially presents the overview of both conventional techniques like synchronous reference frame PLL and some advance PLL techniques including moving average filter based PLL and cascaded delayed signal cancellation PLL. These PLL techniques will be analyzed in terms of dynamic behavior under both normal and adverse grid conditions.

In the second part SAPF is evaluated both with and without the synchronization feature. The dynamic behavior and preciseness of SAPF is highly dependent on the algorithm used for reference current generation. Traditionally time domain techniques are most widely used for this purpose. The p-q theory does not require information of the voltage phase as apposed to SRF theory. SRF theory is known to have more advantages in terms of harmonics selectivity. This theory uses the conventional PLL to estimate frequency and phase that works well under normal

grid conditions but its performance is greatly affected due to the presence of distortions in the grid voltage. In the later part of this chapter modified SRF theory will be applied for reference current generation and the overall control strategy of SAPF will be tested to verify its effectiveness.

5.1 Phase Locked Loop Techniques

Phase-locked loops (PLLs) are commonly applied for synchronization of power converters with the grid voltage. A basic PLL is composed of three parts including phase detector, loop filter and a voltage controlled oscillator. The phase detector makes a comparison between the frequency of the input signal and feedback output of VCO to generate error voltage which is a DC voltage. This signal is passed through LPF to eliminate the high frequency noise. The input and output frequency are compared and adjusted through feedback loop by the VCO until both are equal. A brief discussion of some PLL techniques is given here.

5.1.1 Synchronous Reference Frame PLL

SRF-PLL is the most commonly used PLL technique for getting the information about frequency and phase. This approach has the benefit of simple implementation and quick response in case of normal grid conditions [165, 166]. The SRF-PLL configuration is shown in Fig. 5.1. Co-ordinate transformation is implemented to get the voltage components in *d-q* frame. The proportional integral controller is used to ensure that $v_d = 0$ in the steady state and the grid voltage vector is perfectly aligned along the q-axis. Frequency of the grid voltage is estimated by adding the nominal frequency and output of the PI controller. This signal is integrated to get the phase angle. The unit vectors $\sin\theta$ and $\cos\theta$, ω (estimated frequency) and θ (estimated phase) are the outputs of the SRF-PLL.

The three-phase voltage signals v_{sa}, v_{sb} and v_{sc} are connected to the input of the first block of PLL where Clarks transformation is applied to transform the signal from *abc* frame into $\alpha\beta$ frame as shown in Eq. (5.1).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{5.1}$$

The voltages in d-q frame are obtained by Park transformation with the help of Eq. (5.2).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} sin\,(\theta) & -cos\,(\theta) \\ cos\,(\theta) & sin\,(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{5.2}$$

The q-axis component is the voltage of interest as it provides the phase error information and is given by Eq. (5.3).

$$v_q = v_\alpha cos\,(\theta) + v_\beta sin\,(\theta) \tag{5.3}$$

The estimated frequency ω is given by Eq. (5.4).

$$\omega = k_p v_q + k_i \int v_q dt + \omega_n \tag{5.4}$$

Where ω_n is the nominal value of the grid frequency, k_p and k_i represents the proportional and integral gains.

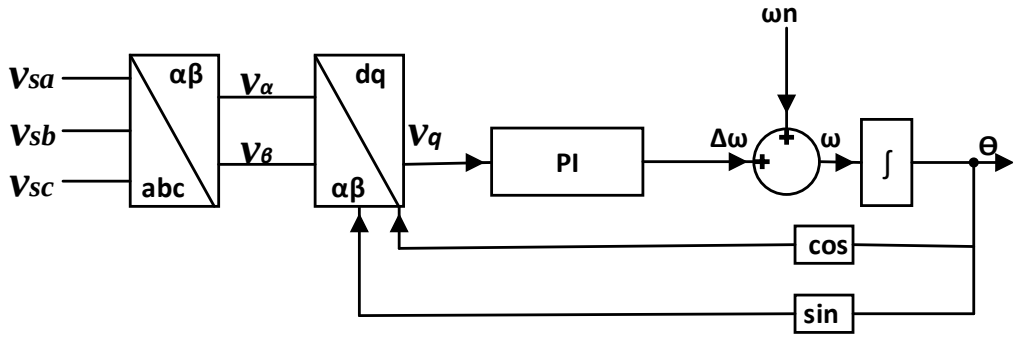

FIGURE 5.1: Structure of SRF-PLL

5.2 Moving Average Filter PLL

The harmonic filtering capability and response speed of SRF-PLL is decreased for adverse grid conditions [167]. The phase estimation of SRF-PLL can be improved by lowering the bandwidth but this will result in a slow dynamic response. Researchers have worked out to enhance the efficiency of SRF-PLL under grid disturbances by applying different modifications. Moving average filter PLL is a good solution for adverse grid conditions. It is a linear-phase filter that allows the dc component to pass through but frequency components of integer multiples of $1/T_w$ in Hertz are completely blocked. The MAF technique is the most broadly used technique as this filter has significant advantages including easy implementation, complete rejection of low order harmonics and low computational burden. But the response slows down in the presence of MAF in the closed loop of PLL. The schematic diagram of MAF-PLL is shown in Fig. 5.2. The three phase voltage signals are the input to the PLL and are converted to two phase stationary reference frame signals in $\alpha\beta$ coordinates. In the next step coordinates in dq rotating reference frame are obtained. A moving average filter is used as a pre-filtering stage to overcome the issues of conventional SRF-PLL. The proportional integral controller is used as in the case of SRF-PLL to ensure that $v_d = 0$ in the steady state and the grid voltage vector is perfectly aligned along the q-axis. Frequency of the grid voltage is estimated by adding the nominal frequency and output of the PI controller. This signal is integrated to estimate the phase angle θ. This phase angle is used as a feedback for park's transformation.

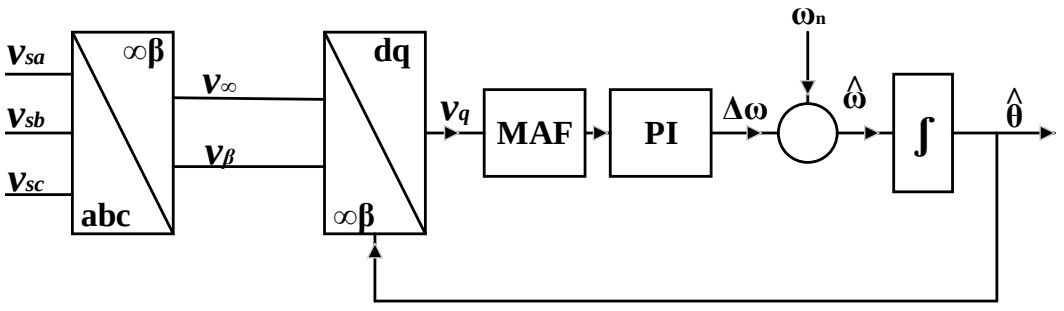

FIGURE 5.2: Schematic diagram of MAF-PLL

Eq. (5.5) and Eq. (5.6) are used for describing the MAF.

$$Y(t) = \frac{1}{T_w} \int_{t-Tw}^{t} X(\tau)\, d\tau \tag{5.5}$$

$$Y(k) = \frac{1}{N} \sum_{n=0}^{N-1} X(k-n) \tag{5.6}$$

Where T_w represents the MAF window length. In Laplace domain the MAF is described as

$$MAF_G(s) = \frac{Y(s)}{X(s)} = \frac{1 - e^{-T_w s}}{T_w s} \tag{5.7}$$

It can be seen from Eq. (5.7) that MAF can reach the steady-state condition in a time equal to width of window. Therefore, the transient response of MAF will be slower if the window width is larger. Furthermore, the open-loop bandwidth of MAF-PLL will also become smaller in size. According to Padė approximation the delay time of Eq. (5.7) can be approximated as shown in Eq. (5.8).

$$e^{-T_w s} \approx \frac{1 - (-T_w s/2)}{T_w s + (-T_w s/2)} \tag{5.8}$$

The insertion of Eq. (5.8) in Eq. (5.7) results in

$$MAF_G(s) \approx \frac{1}{1 + (T_w s/2} \tag{5.9}$$

Substituting $s{=}j\omega$ in Eq. (5.9) to get Eq. (5.10) which represents the magnitude and phase margin of MAF.

$$|MAF_G(j\omega)| = \left| \frac{\sin(\omega T_w/2)}{\omega T_w/2} \right| \angle - \omega T_w/2 \tag{5.10}$$

The MAF-PLL can effectively block the grid disturbances, but its transient response becomes slow. This behaviour of MAF can be understood with the help of open loop bode plot shown in Fig. 5.3 for different window lengths. Selection of T_w needs to be done carefully because for different values of T_w the behaviour of MAF is changed. Thus the design of MAF-PLL for different orders of harmonics is highly dependent on the selection of T_w. For example, T_w should be selected to 1/6 cycle for the harmonics order 5, 7, 11, 13. . etc. For triplen harmonics (3, 9, 27. . .) the bandwidth must be selected to 1/2 cycle and for even harmonics (2, 4, 6. . .) the bandwidth must be selected to 1 cycle.

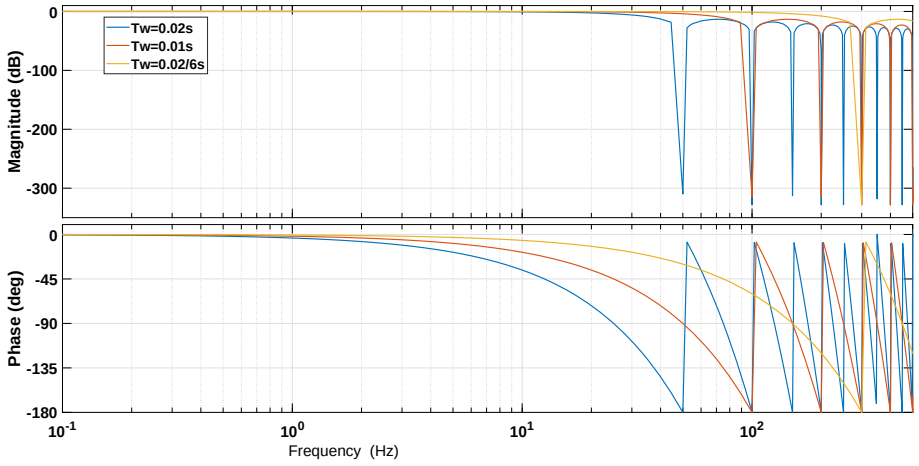

FIGURE 5.3: Bode diagram of MAF

5.2.1 Small Signal Model

For simplifying the stability analysis and dynamic performance study, small signal model of MAF-PLL is developed. A set of three equations is used to represent input voltages of MAF-PLL that is Eq. (5.11), Eq. (5.12) and Eq. (5.13).

$$v_{sa} = \sum ih \left[V_{ih}^{+} cos\left(\theta_{ih}^{+}\right) + V_{ih}^{-} cos\left(\theta_{ih}^{-}\right) \right] \tag{5.11}$$

$$v_{sb} = \sum ih \left[V_{ih}^{+} cos\left(\theta_{ih}^{+} - \frac{2\pi}{3}\right) + V_{ih}^{-} cos\left(\theta_{ih}^{-} + \frac{2\pi}{3}\right) \right] \tag{5.12}$$

$$v_{sc} = \sum ih \left[V_{ih}^{+} cos \left(\theta_{ih}^{+} + \frac{2\pi}{3} \right) + V_{ih}^{-} cos \left(\theta_{ih}^{-} - \frac{2\pi}{3} \right) \right] \tag{5.13}$$

Where V_{ih}^{+} (V_{ih}^{-}) and θ_{ih}^{+} (θ_{ih}^{-}) are the amplitude and phase angle of the interharmonics component of the input voltages. Clark's transformation is applied to yield Eq. (5.14) and Eq. (5.15).

$$v_{\alpha}(t) = \sum_{ih} \left[V_{ih}^{+} cos \left(\theta_{ih}^{+} \right) + V_{ih}^{-} cos \left(\theta_{ih}^{-} \right) \right] \tag{5.14}$$

$$v_{\beta}(t) = \sum_{ih} \left[V_{ih}^{+} cos \left(\theta_{ih}^{+} \right) - V_{ih}^{-} cos \left(\theta_{ih}^{-} \right) \right] \tag{5.15}$$

The q-axis component is attained using Parks transformation by Eq. (5.16).

$$v_{q}(t) = \sum ih \left[V_{ih}^{+} sin \left(\theta_{ih}^{+} - \hat{\theta} \right) + V_{ih}^{-} sin \left(\theta_{ih}^{-} + \hat{\theta} \right) \right] \tag{5.16}$$

Under a quasi-locked state Eq. (5.16) can be approximated by Eq. (5.17).

$$v_{q}(t) \approx V_{1} \left(\theta - \hat{\theta} \right) + f\left(2\omega, 4\omega, 6\omega, \dots\right) \tag{5.17}$$

Where f (2ω, 4ω, 6ω. . .) represents the disturbance. Using Eq. (5.17) and Fig. 5.2 the small signal model of MAF-PLL is developed as shown in Fig. 5.4.

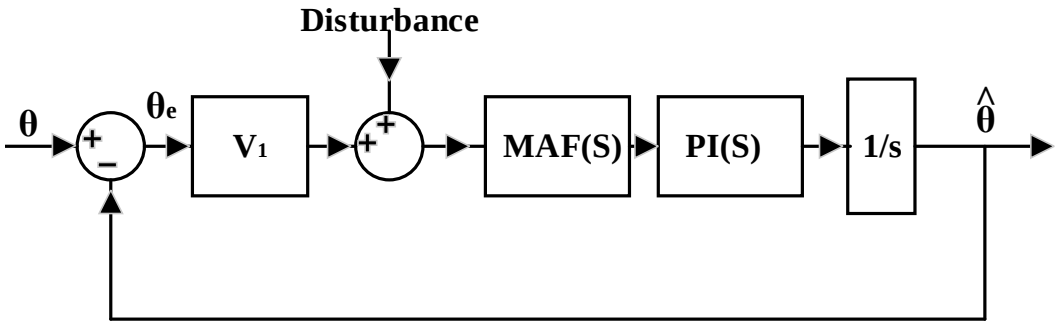

FIGURE 5.4: Small signal model of MAF

5.3 Cascaded Delayed Signal Cancellation PLL

The performance of PLL in distorted grid conditions can be improved by adopting a delayed signal cancellation (DSC) technique. The positive and negative sequence components of the grid voltage in a stationary $\alpha\beta$ reference frame and a quarter cycle delay is introduced in the voltage vector.

In this method the signal is cancelled by adding it to its time-delayed opposite phase version [168, 169]. Usually, the addition of two signals can result in their cancellation if they have same magnitude and opposite phase. Thus this scheme can also be applied for cancellation of harmonics. For this purpose a phase shift of 180° is introduced in the harmonics signal through time delay. Further adding the input signal and the time-delayed harmonics signal cancels the harmonics present in the signal. After the addition of two signals of the same magnitude the DC gain of the input signal is also doubled, therefore, it must be divided by 2. The general expression of the single block of DSC operator is shown in Eq. (5.18).

$$y(t) = \frac{1}{2}\left[x\left(t\right) + x\left(t - \frac{T}{m}\right)\right] \tag{5.18}$$

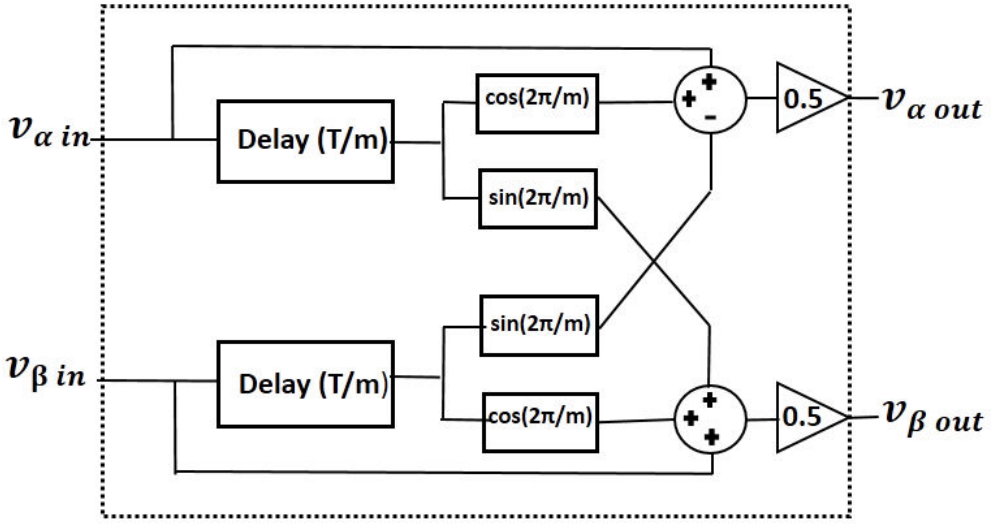

FIGURE 5.5: Single DSC module

$$v_{\alpha\beta\ out} = \frac{1}{2}[v_{\alpha\beta in}\left(t\right) + e^{\frac{j2\pi}{m}} v_{\alpha\beta\ in}\left(t - \frac{T}{m}\right)] \tag{5.19}$$

The Laplace transform of Eq. (5.19) results in Eq. (5.20).

$$v_{\alpha\beta\ out}(s) = \frac{1}{2}[1 + e^{\frac{j2\pi}{m}} e^{\frac{-T}{m}s}]\ v_{\alpha\beta\ in}(s) \tag{5.20}$$

Where

$$\frac{1}{2}\left[1 + e^{\frac{j2\pi}{m}} e^{\frac{-T}{m}s}\right] = \alpha\beta\text{DSC}_m(s) \tag{5.21}$$

Substituting s=jω in Eq. (5.21) and simplifying the mathematical equations, the magnitude and phase angle can be obtained by Eq. (5.22).

$$\alpha\beta\text{DSC}_m(j\omega) = \left|\cos(\frac{\omega T}{2m} - \frac{\pi}{m})\right| \angle(\frac{\omega T}{2m} - \frac{\pi}{m}) \tag{5.22}$$

Frequency response of DSC operator for m=4 and T=0.02s is shown in Fig. 5.6. The $\alpha\beta$DSC4 allows the positive sequence components to pass through and blocks the negative sequence component and reject harmonics of the order h = 4k-1 (k=1, 2, 3). However, harmonics of the order h=4k+1 are not eliminated.

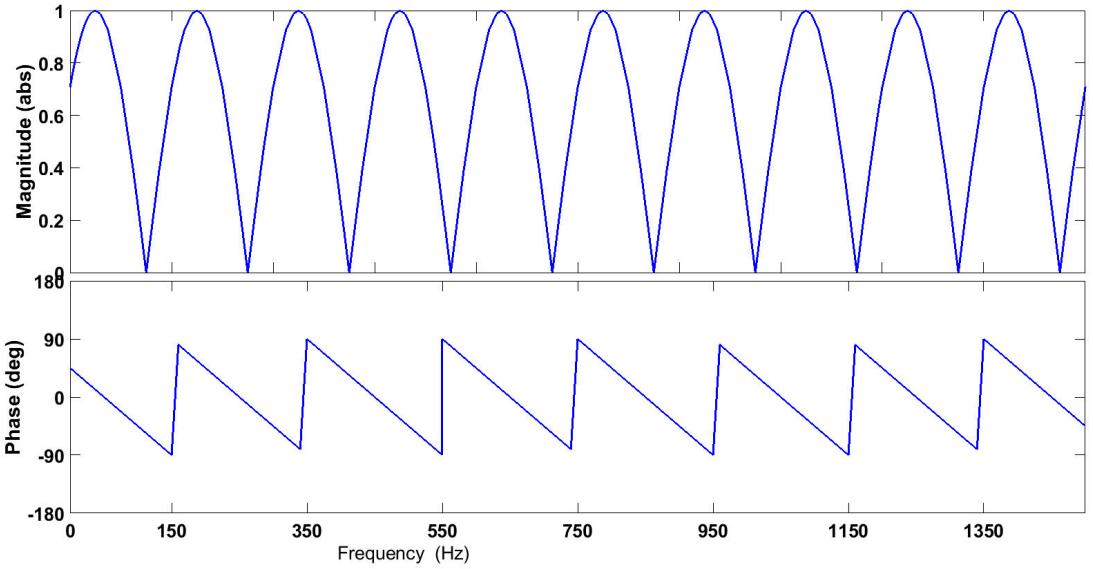

FIGURE 5.6: Frequency response of DSC4 operator

The DSC operator can be cascaded to cancel wide range of harmonics. The cascaded delayed signal cancellation (CDSC) filter is very flexible as it combines a

number of DSC blocks in series to adjust the delay time. The k cascaded $\alpha\beta$DSC operator with delay factors m_1, m_2, m_3, . . .m_k can be approximated by Eq. (5.23)

$$\alpha\beta\text{DSC}_{m_1,\ m_2,\ \ m_3,\ \ldots,m_k}\ \ (s) = \prod_{i=1}^{k} \alpha\beta\text{DSC}_{m_i}(s) \tag{5.23}$$

In our case single DSC module with delay factor m= 2, 4, 8, 16 and 32 respectively are cascaded as shown in 5.7. The resultant operator $\alpha\beta$DSC2,4,8,16,32 is described in s-domain as:

$$\alpha\beta\text{DSC}_{2,4,\ 8,16,32}\ \ (s) = \prod_{m=2,4,8,16,32} \alpha\beta\text{DSC}_{m}(s) \tag{5.24}$$

Each DSC is configured to eliminate certain harmonics, and the CDSC collectively eliminates all undesired harmonics resting in the input. The cascading of DSC blocks results in elimination of all dominant harmonics. The transfer function $\alpha\beta$DSCm as shown in Eq. (5.21)can be re-written as

$$\alpha\beta\text{DSC}_m(s) = \frac{1}{2}[1 + e^{-(\frac{sT}{m} - \frac{j2\pi}{m})}] \tag{5.25}$$

Using Padė approximation the delay term of Eq. (5.25) can be approximated Eq. (5.26)

$$e^{-(\frac{sT}{m} - \frac{j2\pi}{m})} = \frac{1 - (\frac{sT}{2m} - \frac{j\pi}{m})}{1 + (\frac{sT}{2m} - \frac{j\pi}{m})} \tag{5.26}$$

Thus the transfer function $\alpha\beta\text{DSC}_m$ can be approximated as

$$\alpha\beta\text{DSC}_m(s) \approx \frac{1}{1 + \frac{T}{2m}(s - \frac{j2\pi}{T})} \tag{5.27}$$

Where $2\pi/\text{T} = \omega_n$ is the nominal value of grid frequency. The transfer function of two cascaded $\alpha\beta$DSC operators with delay factors m_1 and m_2 can be written as

$$\alpha\beta\text{DSC}_{m_1,\ m_2}(s) = \alpha\beta\text{DSC}_{m_1}(s)\,\alpha\beta\text{DSC}_{\ m_2}(s) \tag{5.28}$$

$$\begin{aligned}\alpha\beta\text{DSC}_{m_1,\ m_2}(s) &\approx \frac{1}{1+\frac{T}{2m_1}(s-j\omega_n)}\frac{1}{1+\frac{T}{2\ m_2}(s-j\omega_n)} \\ &= \frac{1}{1+\frac{T}{2}\left(\frac{1}{m_1}+\frac{1}{m_2}\right)(s-j\omega_n)+\frac{T^2}{4m_1m_2}(s-j\omega_n)^2}\end{aligned} \tag{5.29}$$

Eq. (5.29) can be simplified further by neglecting the its second term.

$$\alpha\beta\text{DSC}_{m_1,\ m_2}(s) \approx \frac{1}{1+\frac{T}{2}\left(\frac{1}{m_1}+\frac{1}{m_2}\right)(s-j\omega_n)} \tag{5.30}$$

Similarly the transfer function for k cascaded operators with delay factor m_i (i=1, 2, 3,, k) can be approximated by

$$\alpha\beta\text{DSC}_{m_1,\ m_2,\ \ m_3,\ ....,m_k}\ \ (s) = \frac{1}{1+\frac{T}{2}\sum_{i=1}^{k}\left(\frac{1}{m_i}\right)(s-j\omega_n)} \tag{5.31}$$

Using Eq. (5.31) the transfer function for $\alpha\beta DSC_{2,4,8,16,32}$ operator is given by Eq. (5.32).

$$\alpha\beta\text{DSC}_{2,4,8,16,32}(s) = \frac{1}{1+\frac{31T}{64}(s-j\omega_n)} \tag{5.32}$$

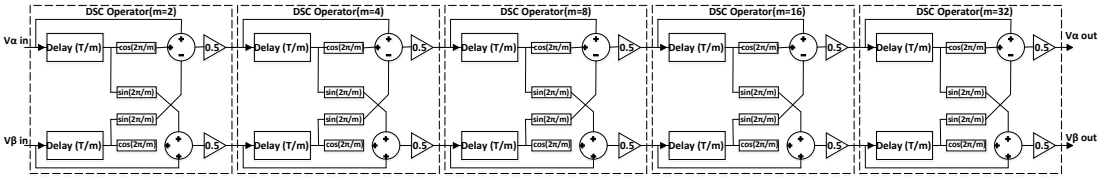

FIGURE 5.7: Structure of CDSC

The CDSC-PLL control block is shown in Fig. 5.8 which includes a delay operator as compared to SRF-PLL. The delayed signal cancellation is applied to

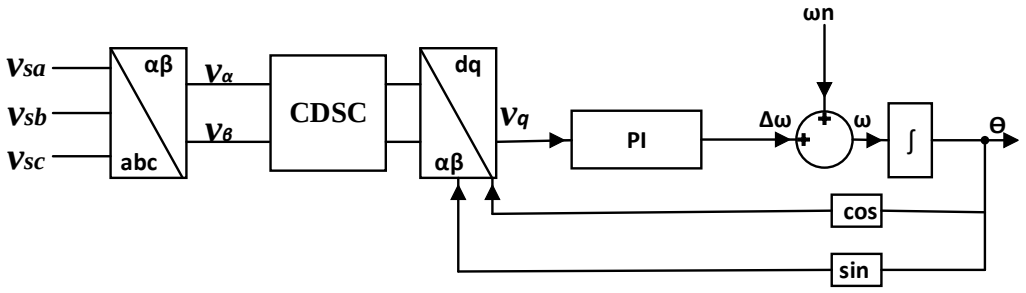

FIGURE 5.8: Block diagram of CDSC-PLL

$\alpha\beta$ co-ordinates of the voltage signals. After the implementation of CDSC block the voltage signals are again transformed from $\alpha\beta$ co-ordinates to *d-q* co-ordinates.

The three PLL techniques over viewed above are evaluated in the presence of different grid conditions. The comparison between these three techniques is performed under Matlab/Simulink environment. The nominal grid frequency is set to 50 Hz. Three test cases are considered for performance evaluation. These test cases are selected on the basis of possible disturbances that can occur in the grid voltage. The main parameters for evaluation/comparison are the dynamic response and filtering capability.

Test Case 1: In this test the grid voltage undergoes a +1 Hz frequency step change. The performance index taken in this case is 2% settling time i.e., the time after which the estimated frequency reaches and remains within 0.02x1 Hz = 0.02 Hz. The frequency overshoot and peak phase error is also calculated for performance evaluation.

Test Case 2: A phase angle jump of +40° is added at 0.1s to further evaluate the techniques. The 2% settling time i.e., the time after which the phase error reaches and remains within 0.02x40° = 0.8° is the main performance index in this test. The phase overshoot and peak frequency error are also calculated for performance evaluation.

Test Case 3: In this test the grid voltage is contaminated with the dc offset ($v_{a,dc}$= -0.1 pu, $v_{b,dc}$= 0.1 pu, $v_{c,dc}$= 0.05 pu). The 2% settling time

in case of frequency estimation and phase error approaching to zero degrees is calculated. The overshoot in frequency and phase is also considered to evaluate the performance of PLL techniques.

The grid voltages under three test conditions are shown in Fig. 5.9. Frequency drift is shown in part a, phase jump in the grid voltage is shown in part b and part c shows the presence of DC offset in the three phase grid voltages. The results thus obtained under harmonics free grid voltage for the PLL techniques under three test conditions are shown in Fig. 5.10. In each part frequency estimation and phase error are plotted separately for each test condition. It is observed that how quickly and accurately a PLL technique estimates frequency in case of a step change. Furthermore in case of a phase angle jump the PLL techniques are evaluated for quickly reducing the phasae error to zero.

Table 5.1 shows the results of PLL techniques for harmonics free grid voltage under three test conditions. This table shows the settling time for each technique in case of frequency and phase change. In addition to this overshoot in frequency and phase and peak error in frequency and phase are also given to evaluate the accuracy of techniques.

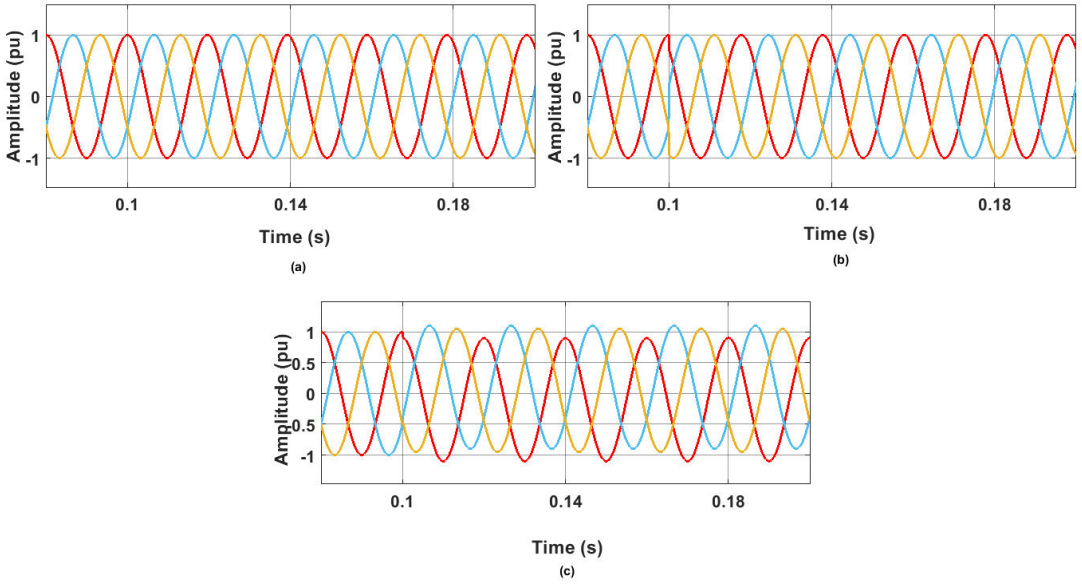

FIGURE 5.9: Grid voltage test conditions (a) Frequency jump, (b) Phase jump, (c) Presence of dc offset

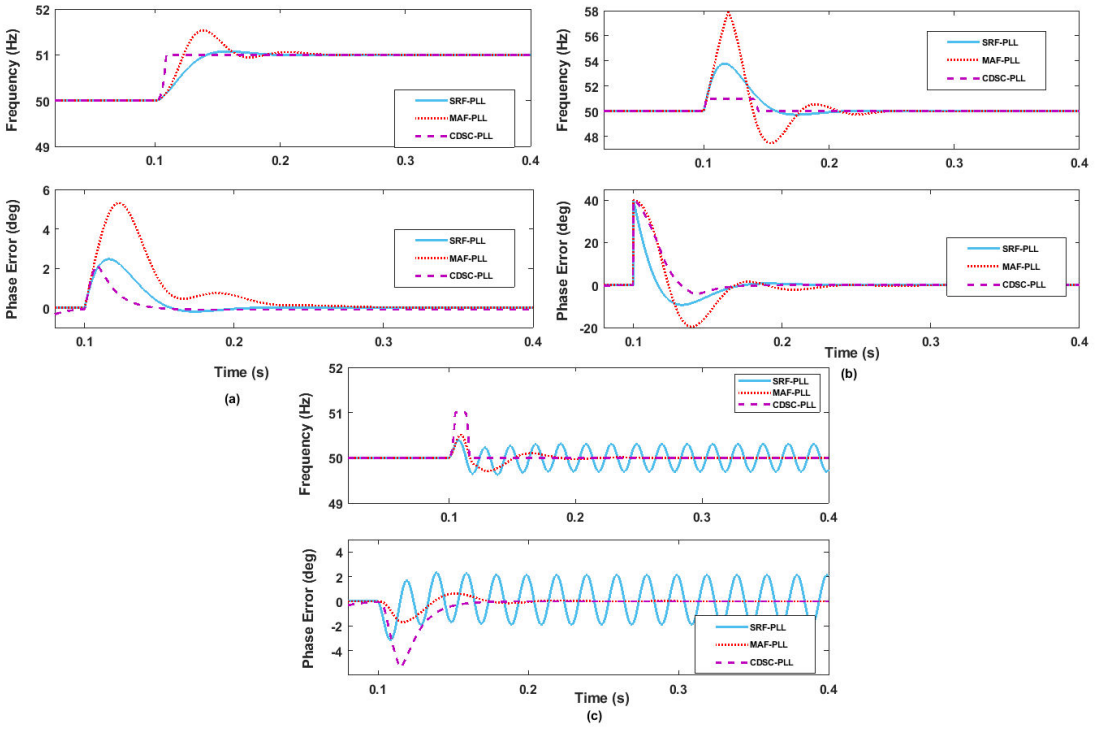

FIGURE 5.10: Harmonics free grid voltage under (a) Frequency jump, (b) Phase jump, (c) Presence of dc offset

TABLE 5.1: Summary of results (harmonics free grid voltage)

Test Case	**SRF-PLL**	**MAF-PLL**	**CDSC-PLL**
Frequency Jump of +1 Hz			
2% Settling Time	82.735 ms	64.716 ms	9.573 ms
Frequency Overshoot	1.07 Hz	0.53 Hz	0 Hz
Peak Phase Error	2.46°	5.3°	2.14°
Phase Angle Jump of +40°			
2% Settling Time	124 ms	128.3 ms	65.4 ms
Phase Overshoot	9.32°	19.61°	4.08°
Peak Frequency Error	3.69 Hz	7.84 Hz	1 Hz
Presence of dc Offset			
2% Settling Time Frequency		82.716 ms	16.63 ms
2% Settling Time Phase		97.6 ms	68.3 ms
Frequency Overshoot	3.82 Hz	0.5 Hz	1 Hz
Phase Overshoot	3.129°	1.697°	5.38°

It is observed from the simulation results that for test case 1 CDSC-PLL takes less than a half cycle to settle down in estimating the frequency, whereas SRF-PLL and MAF-PLL settle to frequency jump in more than four cycles and three cycles respectively. The frequency overshoot and peak phase error of CDSC-PLL is also less than the other two techniques. When a phase angle jump is added, the performance of CDSC-PLL is again better among the three techniques in terms of settling time. The phase overshoot and peak frequency error is again less than the other techniques. For further evaluation, dc offset is added as per test case 3. In this case the CDSC-PLL has better dynamic response but the overshoot in frequency and phase of CDSC-PLL is larger than SRF-PLL and MAF-PLL. In this case the performance of SRF-PLL is greatly affected as it fails to settle down to a change in frequency and phase.

The three tests are performed again by adding harmonics of the order 5, 7, 11, 13. to the grid voltages and their parameters are listed in Table 5.2. The three phase grid voltages contaminated with harmonics of the order 5, 7, 11, 13. are shown in Fig.4.11. The simulation results for the PLL techniques in three test cases are shown in Fig. 5.12. When a frequency jump is added at 0.1s the CDSC-PLL again give a quick response in estimating the grid frequency and phase but the filtering capability of SRF-PLL is reduced as compared to other techniques. The MAF-PLL shows a very slow response in estimation of frequency and phase. The addition of phase jump and dc offset to the grid voltage results in almost the same behaviour in terms of dynamic response as in the case of harmonics free voltages but in this case ripples appear in the response of SRF-PLL. The SRF-PLL has failed to estimate frequency and phase in the presense of dc offset. The simulation results obtained in this case are shown in Table 5.3.

The simulink model presented here can be tested for any pattern of harmonics like even harmonics, triplen harmonics and interharmonics. Also the amplitude of these harmonics can also be adjusted to see the behaviour of PLL techniques. Moreover, the disturbances can be added at any instant of time during the simulation both independently and collectively. Thus the model can be used for evaluation of PLL techniques under wide range of harmonics.

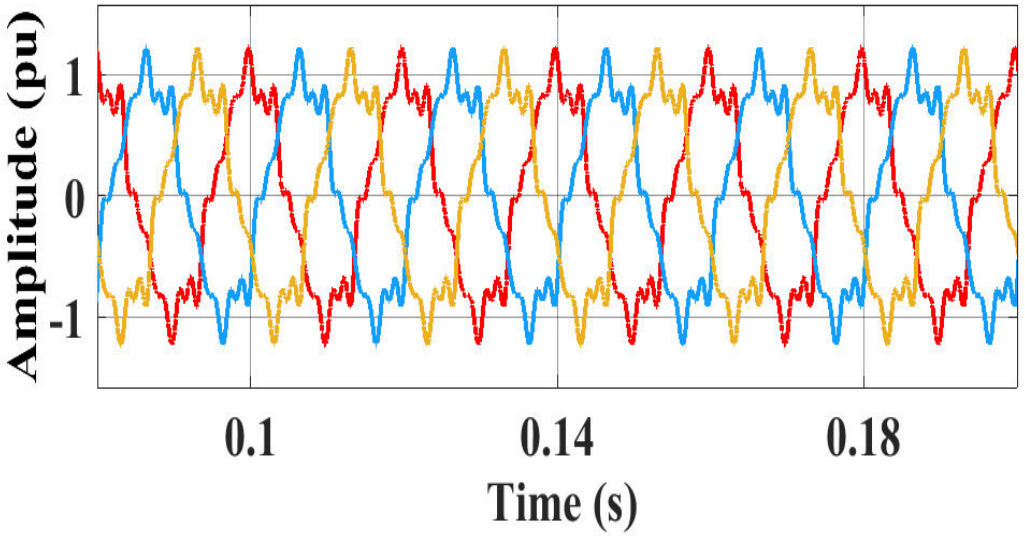

FIGURE 5.11: Grid voltage contaminated with harmonics (5,7,11,13)

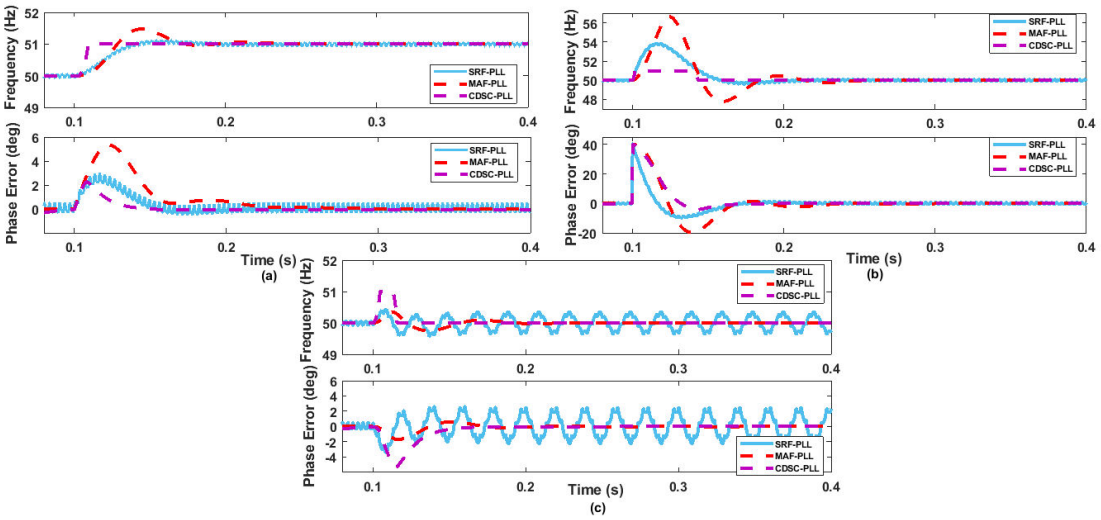

FIGURE 5.12: Grid voltage contaminated with harmonics (5,7,11,13) under (a) Frequency jump, (b) Phase jump, (c) Presense of dc offset

TABLE 5.2: Parameters of Harmonics (5,7,11,13)

Voltage Component	**Amplitude (pu)**
Fundamental positive sequence	1
Harmonic order (5)	0.1
Harmonic order (7)	0.1
Harmonic order (11)	0.1
Harmonic order (13)	0.05

TABLE 5.3: Summary of results (harmonics order 5,7,11,13)

Test Case	**SRF-PLL**	**MAF-PLL**	**CDSC-PLL**
Frequency Jump of +1 Hz			
2% Settling Time	84.837 ms	70.97 ms	10.315 ms
Frequency Overshoot	1.11 Hz	0.48 Hz	0 Hz
Peak Phase Error	2.89°	5.312°	2.19°
Phase Angle Jump of +40°			
2% Settling Time	141.2 ms	137.3 ms	68.86 ms
Phase Overshoot	9.64°	19.56°	4.14°
Peak Frequency Error	3.87 Hz	6.62 Hz	1 Hz
Presence of dc Offset			
2% Settling Time Frequency	–	88.09 ms	16.87 ms
2% Settling Time Phase		99.84 ms	69.26 ms
Frequency Overshoot	3.87 Hz	0.35 Hz	1 Hz
Phase Overshoot	2.65°	1.698°	5.24°

The three tests are performed again by adding interharmonics to the grid voltage. As stated earlier interharmonics are the harmonics with frequencies that are not integer multiples of fundamental. The parameters of interharmonics are listed in Table 5.4. It can be seen that low values are selected for amplitude of interharmonics as generally interharmonics have low amplitudes in real life. The three phase grid voltages contaminated with interharmonics are shown in Fig. 5.13.

TABLE 5.4: Parameters of Interharmonics

Voltage Component	**Amplitude (pu)**
Fundamental positive sequence	1
Harmonic order (5.5)	0.04
Harmonic order (7.5)	0.04
Harmonic order (11.5)	0.03
Harmonic order (13.5)	0.03

TABLE 5.5: Summary of results (Interharmonics)

Test Case	**SRF-PLL**	**MAF-PLL**	**CDSC-PLL**
Frequency Jump of +1 Hz			
2% Settling Time	83.89 ms	71.35 ms	10.152 ms
Frequency Overshoot	1.08 Hz	0.47 Hz	0 Hz
Peak Phase Error	2.55°	5.31°	2.25°
Phase Angle Jump of +40°			
2% Settling Time	73.49 ms	142.83 ms	64.3 ms
Phase Overshoot	9.148°	19.61°	4.33°
Peak Frequency Error	3.86 Hz	5.66 Hz	1 Hz
Presence of dc Offset			
2% Settling Time Frequency	–	56.12 ms	16.3 ms
2% Settling Time Phase	–	97.8 ms	59.38 ms
Frequency Overshoot	0.39 Hz	0.35 Hz	1 Hz
Phase Overshoot	6.345°	1.708°	5.48°

When a frequency jump is added at 0.1s the CDSC-PLL again give a quick response in estimating the grid frequency and phase but the filtering capability of SRF-PLL and CDSC-PLL is reduced as compared to MAF-PLL as indicated in the zoomed view. The MAF-PLL shows a very slow response in estimation of frequency and phase. The addition of phase jump and dc offset to the grid voltage results in almost the same behaviour in terms of dynamic response as in the case of harmonics free voltages but in this case ripples appear in the response of SRF-PLL and CDSC-PLL. Also SRF-PLL is not able to estimate the frequency and phase in the presence of dc offset.

The peak frequency and phase error in this case is also less for CDSC-PLL as compared to other techniques. Similarly overshoot in frequency and phase is small for CDSC-PLL in comparison to SRF-PLL and MAF-PLL. Simulation results obtained in this case are shown in Table 5.5 and graphical results for the PLL techniques in three test cases are shown in Fig. 5.14.

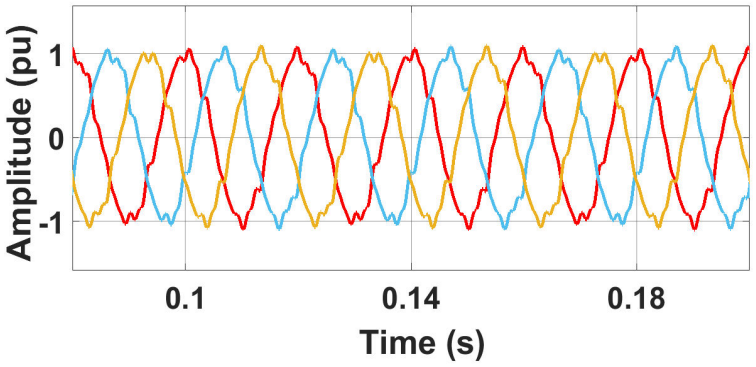

FIGURE 5.13: Interharmonics in grid voltage.

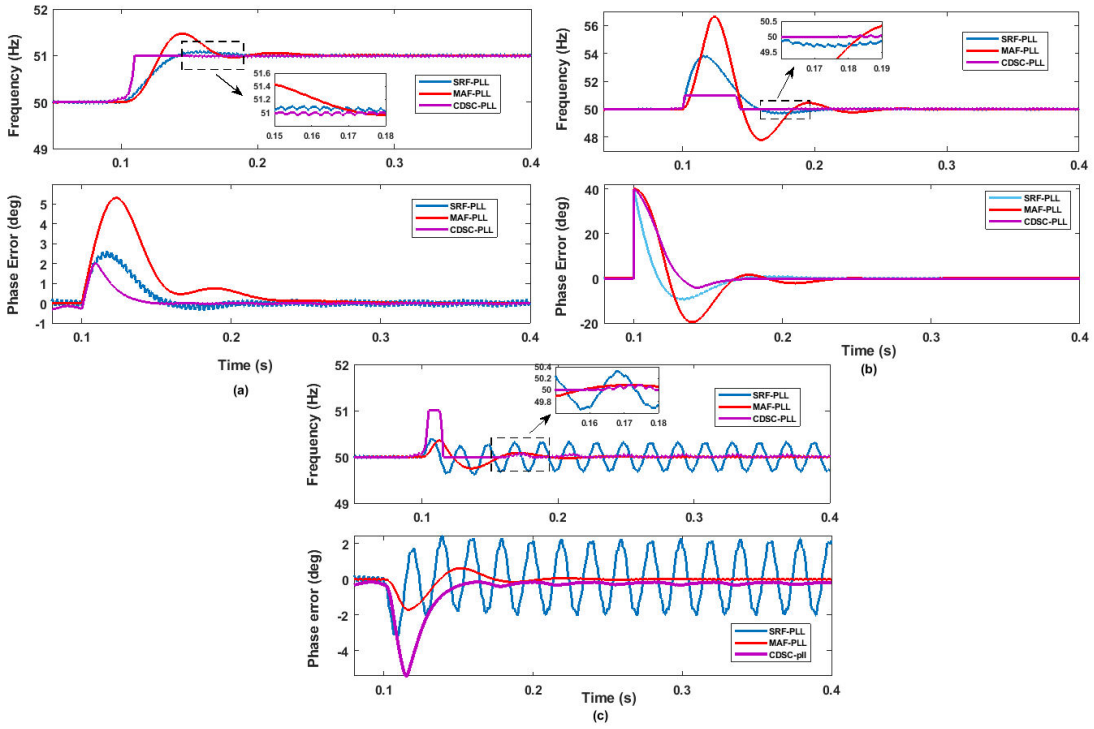

FIGURE 5.14: Distorted grid voltage (Interharmonics) under (a) Frequency jump, (b) Phase jump, (c) Presence of dc offset.

5.4 Performance Evaluation of SAPF

In this section the shunt active power filter is evaluated both with and without the synchronization feature. The dynamic behavior and preciseness of SAPF is highly dependent on the algorithm used for reference current generation. Traditionally time domain techniques are most widely used for this purpose. The p-q theory does not require information of the voltage phase but the synchronous reference

frame theory (d-q) is dependent on frequency and phase information. SRF theory uses the conventional PLL to estimate frequency and phase that works well under normal grid conditions but its performance is degraded by grid disturbances.

5.5 Testing Criteria

The main objective is to mitigate current harmonics present in the system due to the connection of non-linear loads. The problem is that the presence of grid disturbances results in inaccurate estimation of frequency and phase which further afffects the accuracy of reference current generation technique.
In order to achieve the objective a modified synchronous reference frame trheory has been developed by making changes in its frequency and phase estimation part. The conventional theory uses SRF-PLL but here CDSC-PLL is used for frequency and phase estimaation.
The CDSC-PLL has been tested for performance evaluation under the effects of grid disturbances. The modified synchronous reference frame theory has also been tested under frequency drift, phase angle variation and presence of DC offset. SAPF has been evaluated first without the synchronization feature and further tested using the modified control strategy to differentiate the working of SAPF under grid disturbances.

5.5.1 IEEE Benchmark System

The IEEE benchmark system of [170] is used to generate different loading scenarios. The benchmark system for active power filter consists of a power electronic circuit and a digital controller. A three phase bridge rectifier is used as a non-linear load and an RL load is connected across the bridge rectifier. Different load combinations are selected for evaluation purpose as used by some IEEE journals like [171] and [25] and are shown in Table 5.6.

5.5.2 Simulation Results

The main parameter for performance evaluation/comparison used here is the THD value of the compensated source current. For the purpose of investigating the importance of synchronization of active power filters, the SAPF is simulated first by generating the reference current using SRF theory. I. The disturbances in the grid like frequency drift, phase angle jump and presence of DC offset do not increase the harmonics in a signal but affect the estimation of frequency and phase which in turn affects the extraction of reference current and has been proved by simulating SAPF under grid disturbances. For the second case modified SRF theory is used to generate the reference current with cascaded delayed signal cancellation technique implemented for phase and frequency estimation. In the first part of this chapter the cascaded delayed signal cancellation technique has been proved to perform well to estimate the frequency and phase under adverse grid conditions. This technique has shown a great accuracy and fast dynamic response under the effects of frequency drift, phase angle variation and presence of dc offset. The reference current is generated by using both the techniques under normal and adverse grid conditions. For testing under adverse grid conditions a frequency drift, dc offset and phase angle variation is created in the source voltage using a programmable voltage source.

5.5.2.1 Simulink Models

The Simulink model of SAPF is shown in Fig. 5.15. In this model a three phase non-linear load is connected to a three phase AC source and SAPF is connected at the point of common coupling. The reference current block, synchronization block and current injection controller are build as sub systems. In the first step reference current is generated and in the second step this current is fed to the current injection controller to generate gate pulses of VSI. This process results in a harmonics free source current. PI control is implemented for regulation of DC link voltage.

In Fig. 5.16 simulink model of CDSC-PLL shows five single DSC blocks cascaded. Voltage in abc coordinates is converted to $\alpha\beta$ coordinates and are fed to CDSC block. The output of CDSC block is connected to the park's transformation block to get the dq components of voltage.
Modified synchronous reference frame theory is shown in Fig. 5.17. A three phase non-linear load is connected to a three phase AC source and distorted source current is fed to the transformation block of SRF theory. In the conventional theory SRF-PLL is used for estimation of frequency and phase. Modification is made by using CDSC-PLL structure inside the synchronous reference frame theory and is highlighted in the model. Three phase source voltage is firt converted from abc reference frame to $\alpha\beta$ frame and then connected to the CDSC-PLL block to estimate frequency and phase and give this information to the transformation block to generate the dq components. Inverse transformation is used to get the reference current in abc coordinates.
Fig. 5.18 shows the simulink model of SRF-PLL. Three phase voltage components in abc frame are converted to $\alpha\beta$ frame and further converted to dq components by the park's transformation block. Frequency of the grid voltage is estimated by adding the nominal frequency and output of the PI controller. This signal is integrated to get the phase angle. Simulation parameters are summarized in Table 5.6.

For case 1 of simulation an RL load is connected across the three phase bridge rectifier the resulting current waveform is shown in Fig. 5.19. Fig. 5.20 shows the reference current for all the three phases generated by using modified SRF theory. After the injection of this reference current we get a sinusoidal current waveform and is shown in Fig. 5.21.

For the second case of simulation another RL load with different values is connected to the source and the resulting waveform is shown in Fig. 5.22. Simulations are repeated using the modified control strategy and the corresponding reference current for load 2 is shown in Fig. 5.23. Furthermore Fig. 5.24 shows the compensated source current waveform. Finally Load 3 is connected to the three-phase AC source and the resulting waveforms are shown in Fig. 5.25, Fig. 5.26 and

TABLE 5.6: Simulation Parameters

Elements	**Parameter**	**Value**
AC Source	RMS line-line supply voltage	380 V
	Supply frequency	50 Hz
SAPF	Dc link voltage reference	800 V
	Dc link capacitor C_{dc}	2200 F
	Filter inductance	18 mH
Non-linear load	Three-phase diode rectifier	———
	Load 1	460 Ω, 10 mH
	Load 2	360 Ω, 15 mH
	Load 3	30 Ω, 18 mH, 200 uF

TABLE 5.7: THD of Load Currents

Load	**% THD**
Load 1	27.45
Load 2	30.61
Load 3	35.06

Fig. 5.27. The parameters of load are shown in Table 5.6 and their corresponding THD values are shown in Table 5.7. Load 1 is just an RL load connected across the three phase bridge rectifier. Load 2 is the same combination but with larger values and load 3 is a cobination of R, L and C connected across the three phase bridge rectifier. The aim is to evaluate the SAPF under variable loads and various grid disturbances to validate its effectiveness. The grid disturbances can be added using a programmable three phase voltage source which provides the option of adding step change of frequency, phase and amplitude.

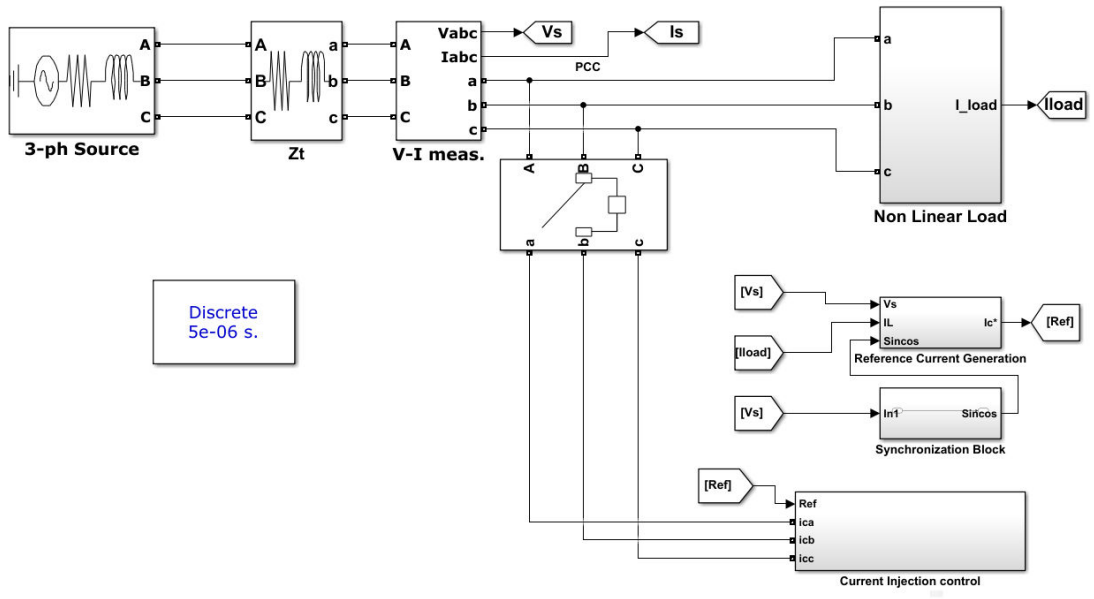

FIGURE 5.15: Simulink Model of SAPF

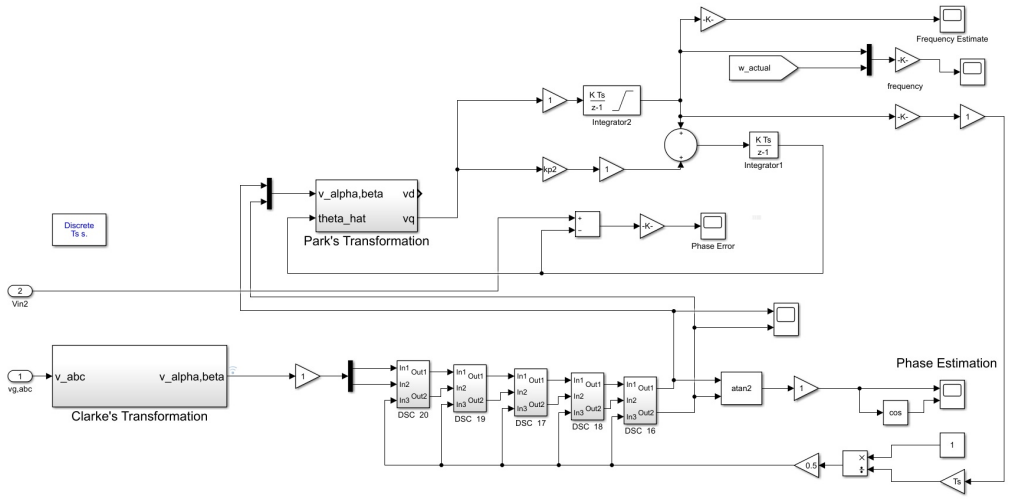

FIGURE 5.16: Simulink Model of CDSC-PLL.

.

5.6 Analysis of Results

The results thus achieved after implementation of both configurations of SAPF are summarized in Table 5.8. Disturbances in the grid are created through a programmable voltage source such as + 3Hz drift in frequency, +10° phase angle jump and dc offset. SAPF is first simulated by implementing the pq theory for

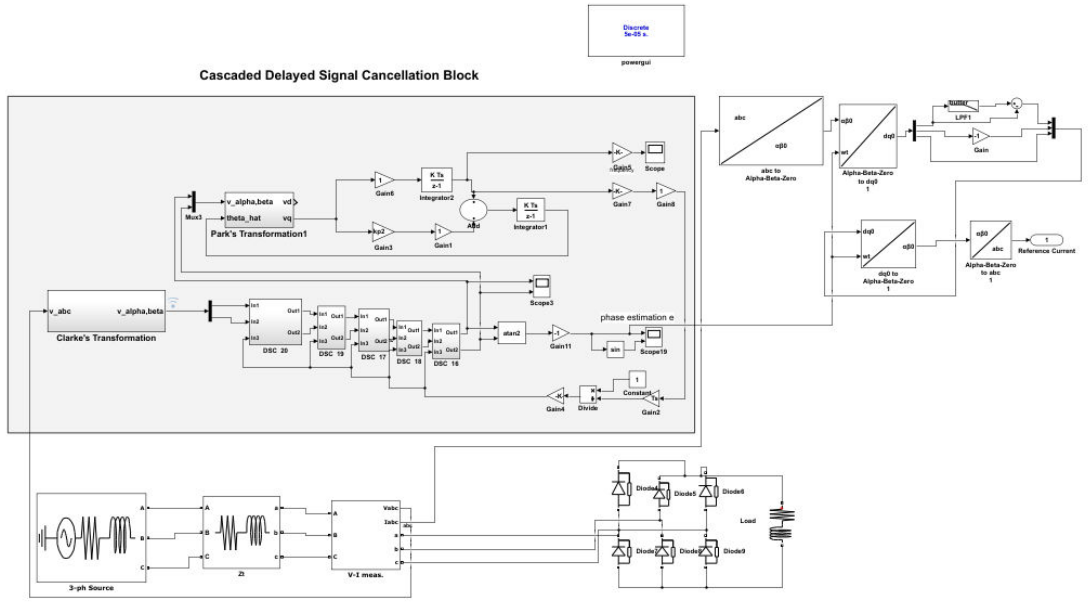

FIGURE 5.17: Simulink Model of Modified Synchronous Reference Frame Theory.

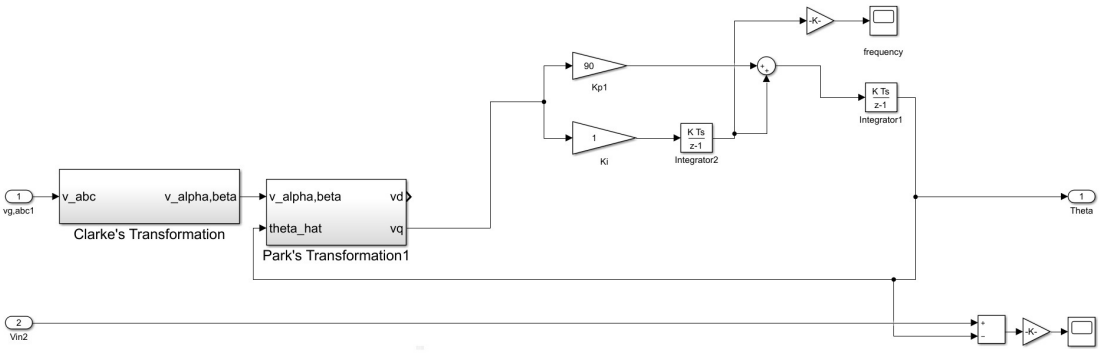

FIGURE 5.18: Simulink Model of SRF-PLL.

reference current generation and evaluating it under both normal and adverse grid conditions. Under disturbance free grid voltage THD of the source current reduces to a value under the limits of IEEE-519 standard for different loading scenarios. Simulations are carried out again under the effects of frequency drift, phase angle jump and presence of DC offset and the results in all three cases of load show that THD of the compensated source current increases considerably.

In the next phase SAPF has been simulated using the modified control strategy for reference current generation under both grid voltage scenarios. The shunt active power filter has been simulated for all the three load cases and it is concluded that

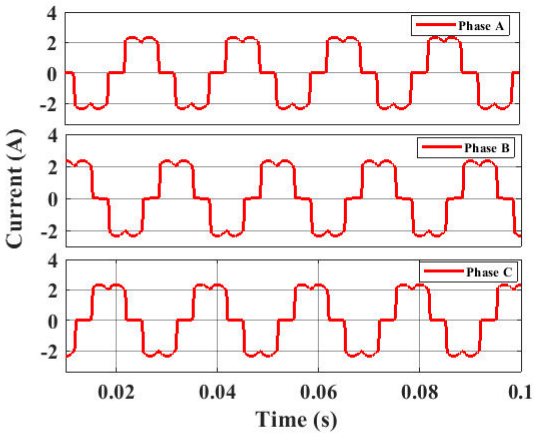

FIGURE 5.19: Current Waveform for Load 1.

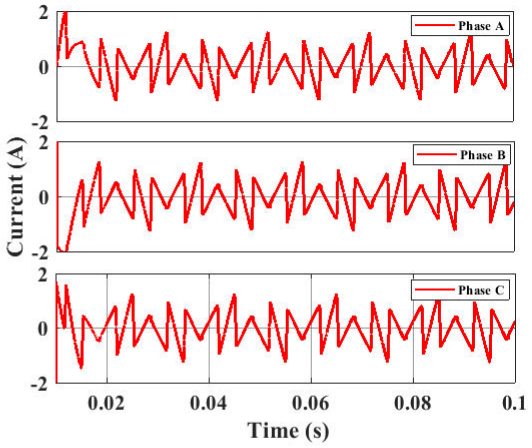

FIGURE 5.20: Reference Current Waveform for Load 1.

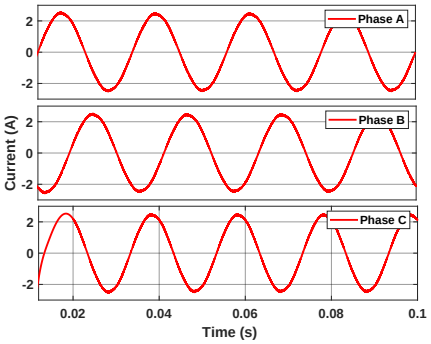

FIGURE 5.21: Source Current Waveform for Load 1.

performance of SAPF does not degrade under grid disturbances and THD of the source current is reduced to a value well within IEEE-519 standard. Finally for validation of results the proposed technique is compared with some previous work

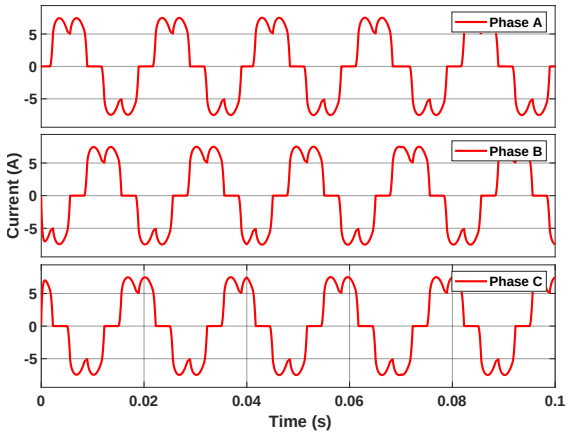

FIGURE 5.22: Current Waveform for Load 2.

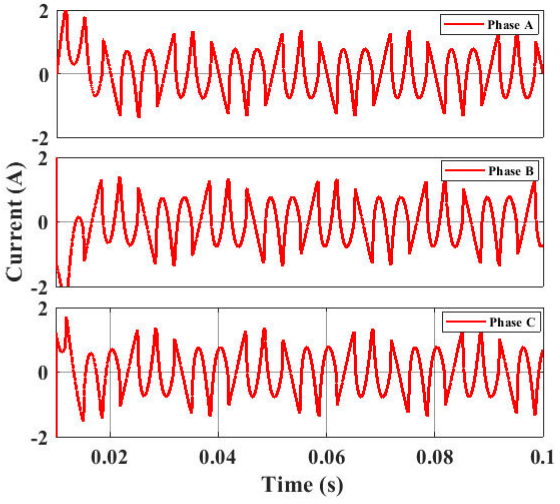

FIGURE 5.23: Reference Current Waveform for Load 2.

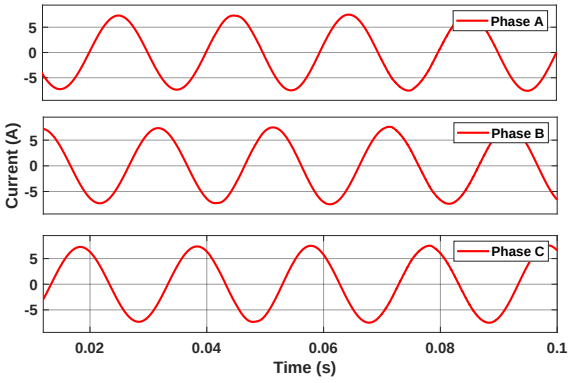

FIGURE 5.24: Source Current Waveform for Load 2.

and is shown in 5.9 and it is verified that the proposed work is better in terms of THD reduction than the compared work.

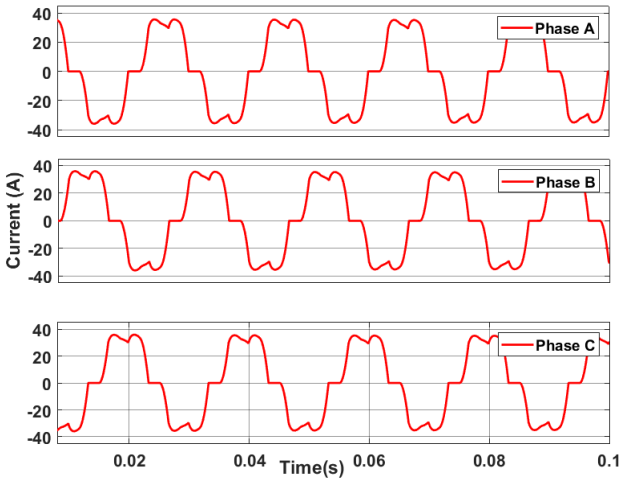

FIGURE 5.25: Current Waveform for Load 3.

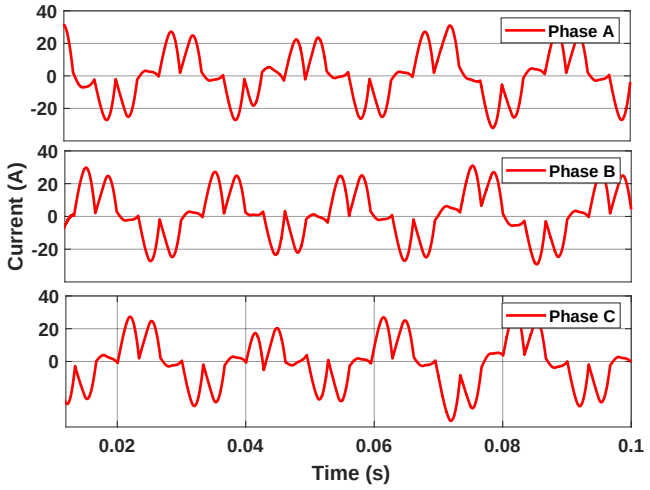

FIGURE 5.26: Reference Current Waveform for Load 3.

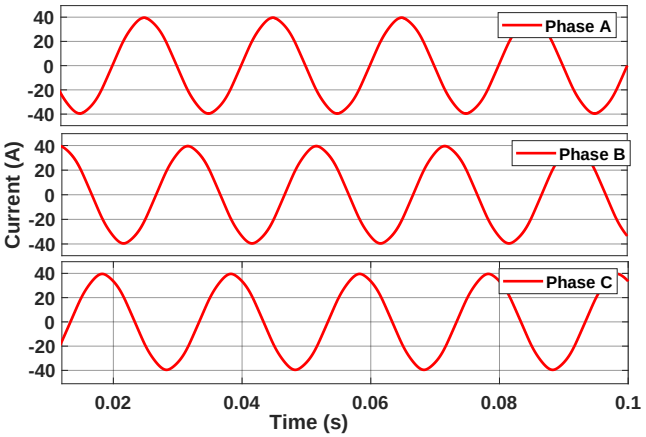

FIGURE 5.27: Source Current Waveform for Load 3.

TABLE 5.8: Summary of Results

Test Case	**Compensated % THD without synchroniztion feature**			**Compensated % THD with synchroniztion feature**		
	Load 1	**Load 2**	**Load 3**	**Load 1**	**Load 2**	**Load 3**
Normal Grid condition	3.63	5.01	6.21	1.47	1.65	1.89
Frequency jump of +3 Hz	5.99	7.28	8.81	1.70	1.84	2.01
Pretense of DC offset	9.44	17.16	19.67	3.13	4.84	4.91
Phase angle jump of $+10^{\circ}$	9.70	18.21	20.31	2.92	2.97	3.11

TABLE 5.9: Comparison with Previous Work

Technique	**THD before Compensation**	**THD after Compensation**
[61] using ANN and SRF technique for RL Load	27.02%	2.39%
[172] using SRF technique for RL Load	16.6%	2.54%
Proposed Technique for RL Load	27.45%	1.47%

5.7 Summary

In initial part of this chapter a brief overview of phase locked loop techniques is presented. Three techniques have been compared for performance evaluation under adverse grid conditions including SRF-PLL, MAF-PLL and CDSC-PLL. In the later part SAPF is investigated for its synchronization feature. Modified synchronous reference frame theory is applied for reference current generation . The modification is made by using CDSC-PLL technique for estimation of frequency and phase instead of the conventional PLL technique. The results are compared with the pq theory based SAPF. It is observed that both configurations worked well under normal grid conditions but in the presence of grid disturbances, the proposed strategy of SAPF has shown much better performance.

Chapter 6

Conclusion and Future Work

In this chapter conclusion of the research work is presented. Furthermore, some future recommendations are also stated to extend the present work.

6.1 Conclusion

This thesis works on the mitigation of current harmonics due to the presence of non-linear loads under distorted grid conditions using shunt active power filter. Shunt active power filter is divided into two main parts, reference current generation and current injection. In this perspective different control strategies are being used to enhance the compensation performance of three phase shunt active power filter. A comprehensive review of these techniques is presented. Findings of the researchers and issues observed in different control techniques have been identified. Synchronization of active power filters and its importance for reference current generation has been deeply investigated and contributions are made in this part of active power filtering. Among the discussed techniques, d-q theory requires frequency and phase information for which it uses the conventional PLL technique. In this theory the accurate estimation of frequency and phase is very important for generation of precise reference current. Theoretically explained reference current generation techniques are being evaluated by adding the reference

current to the load current to get the sinusoidal waveform.

Three control techniques including single band hysteresis current control, double band hysteresis current control and sliding mode control are studied and evaluated for their current injection ability. Among the three techniques sliding mode control has been proved as the best technique for generating the gate pulses of voltage source inverter. Phase locked loop techniques are investigated for estimation of frequency and phase under various grid disturbances.

After the evaluation of PLL techniques it is proved that CDSC-PLL has best results in terms of settling time of 10.315 ms, peak phase error of 2.19 degrees and peak frequency error of 1 Hz.

A modified synchronous reference frame theory has been developed for generating the reference current. The conventional theory uses SRF-PLL for estimation of frequency and phase. It has been proved that in the presence of grid disturbances SRF-PLL has a settling time of 84.837 ms, peak phase error of 2.89 degrees and a peak frequency error of 3.87 Hz and in the presence of DC offset it is not even able to estimate frequency and phase. In the modified theory CDSC-PLL is used for estimation of frequency and phase. Shunt active power filter has been evaluated using the modified synchronous reference frame theory for reference current generation under a frequency drift of 3 Hz, phase angle jump of 10 degrees and a DC offset of 0.1 pu. These disturbances affects the generation of reference current as proved by the results of SRF theory. For validation of results the proposed control strategy has been compared with the SAPF using the pq theory for reference current generation. Both the strategies have been evaluated under both normal and adverse grid conditions. Results conclude that SAPF using the pq theory shows satisfactory performance under normal grid conditions but in the presence of grid disturbances THD of the compensated source current goes to a value of 20.31%. On the other hand the proposed technique shows better results in terms of THD reduction and achieves THD values of 2.01, 4.91 and 3.11 in the three cases of grid disturbances which comply with the IEEE-519 standard thus also proving robustness of SAPF. Results also proves the accuracy of modified theory in generating the reference current under the effects of grid disturbances.

6.2 Suggestions for Future Work

The research work presented in this dissertation has given a new perspective for future research in the field of shunt active power filtering. The following issues have been detected during this research work and are listed here as possible topics for future work in this area.

- The application of the proposed shunt active power filter system to diminish other power quality problems such as sags, swells and flickering may be investigated.
- This study can be extended to 3-phase 4-wire distribution systems.
- This research focuses on the fundamental theoretical problems rather than the hardware implementation. The proposed active filter could be experimentally verifed by developig prototype.
- The proposed work can be applied in applications that contain interharmonics, such as speed drives of shipboard power systems and grid connected PV inverters.
- The proposed work can also be applied for ripple factor reduction in HVDC systems with higher current and voltage ratings.

Bibliography

[1] A. E. Emanuel, "Summary of ieee standard 1459: definitions for the measurement of electric power quantities under sinusoidal, nonsinusoidal, balanced, or unbalanced conditions," *IEEE transactions on industry applications*, vol. 40, no. 3, pp. 869–876, 2004.

[2] V. Khadkikar, "Enhancing electric power quality using upqc: A comprehensive overview," *IEEE transactions on Power Electronics*, vol. 27, no. 5, pp. 2284–2297, 2011.

[3] S. Khan, B. Singh, and P. Makhija, "A review on power quality problems and its improvement techniques," in *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*.

[4] M. Sugirtha and P. Latha, "Analysis of power quality problems in grid connected wind power plant," in *2011 International Conference on Recent Advancements in Electrical, Electronics and Control Engineering*. IEEE, 2011, pp. 19–24.

[5] X. Liang, "Emerging power quality challenges due to integration of renewable energy sources," *IEEE Transactions on Industry Applications*, vol. 53, no. 2, pp. 855–866, 2016.

[6] T. S. Key, "Diagnosing power quality-related computer problems," *IEEE Transactions on Industry Applications*, no. 4, pp. 381–393, 1979.

[7] M. Morcos and J. Gomez, "Electric power quality-the strong connection with power electronics," *IEEE power and energy magazine*, vol. 1, no. 5, pp. 18–25, 2003.

[8] C. Henville, "Power quality impacts on protective relays-and vice versa," in *2001 Power Engineering Society Summer Meeting. Conference Proceedings (Cat. No. 01CH37262)*, vol. 1. IEEE, 2001, pp. 587–592.

[9] P. Esslinger and R. Witzmann, "Improving grid transmission capacity and voltage quality in low-voltage grids with a high proportion of distributed power plants," *Energy Procedia*, vol. 12, pp. 294–302, 2011.

[10] S. Santoso, E. J. Powers, W. M. Grady, and P. Hofmann, "Power quality assessment via wavelet transform analysis," *IEEE transactions on Power Delivery*, vol. 11, no. 2, pp. 924–930, 1996.

[11] M. Savaghebi, A. Jalilian, J. C. Vasquez, and J. M. Guerrero, "Secondary control for voltage quality enhancement in microgrids," *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 1893–1902, 2012.

[12] S. Chattopadhyay, M. Mitra, and S. Sengupta, "Electric power quality," in *Electric Power Quality*. Springer, 2011, pp. 5–12.

[13] M. H. Bollen and S. K. Rönnberg, "Primary and secondary harmonics emission; harmonic interaction-a set of definitions," in *2016 17th International Conference on Harmonics and Quality of Power (ICHQP)*. IEEE, 2016, pp. 703–708.

[14] S. Albatran, Y. Fu, and A. Albanna, "Comprehensive mathematical description and harmonic analysis of hybrid two-dimensional–three-dimensional space vector modulation," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3327–3336, 2013.

[15] J. L. Younker and R. Ehrlich, "Fourier biometrics: harmonic amplitudes as multivariate shape descriptors," *Systematic Biology*, vol. 26, no. 3, pp. 336–342, 1977.

[16] A. Kamenka, "Six tough topics about harmonic distortion and power quality indices in electric power systems."

[17] B. R. Khade and V. Virulkar, "Mitigation of harmonics in a neutral conductor for three-phase four-wire distribution system using series active power filter," in *2015 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*. IEEE, 2015, pp. 1–6.

[18] P. Enjeti, W. Shireen, P. Packebush, and I. Pitel, "Analysis and design of a new active power filter to cancel neutral current harmonics in three phase four wire electric distribution systems," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*. IEEE, 1993, pp. 939–946.

[19] J. P. Brozek, "The effects of harmonics on overcurrent protection devices," in *Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting*. IEEE, 1990, pp. 1965–1967.

[20] R. Abdikarimuly, Y. L. Familiant, A. Ruderman, and B. Reznikov, "Calculation of current total harmonic distortion for a single-phase multilevel inverter with lcl-filter," in *2016 IEEE international power electronics and motion control conference (PEMC)*. IEEE, 2016, pp. 63–68.

[21] R. Panigrahi, B. Subudhi, and P. C. Panda, "A robust lqg servo control strategy of shunt-active power filter for power quality enhancement," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2860–2869, 2015.

[22] J. Moravek, J. Drapela, V. Wasserbauer, and P. Mastny, "Power quality issues related to power flow control in systems with renewable energy micro sources," in *2016 17th International Scientific Conference on Electric Power Engineering (EPE)*. IEEE, 2016, pp. 1–6.

[23] A. Kalair, N. Abas, A. Kalair, Z. Saleem, and N. Khan, "Review of hpxkm bhg ucfybnbfu7nyt hbnnbarmonic analysis, modeling and mitigation techniques," *Renewable and Sustainable Energy Reviews*, vol. 78, pp. 1152–1187, 2017.

[24] A. Marzoughi, H. Imaneini, and A. Moeini, "An optimal selective harmonic mitigation technique for high power converters," *International Journal of Electrical Power & Energy Systems*, vol. 49, pp. 34–39, 2013.

[25] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler, and M. A. Aguirre, "Selective harmonic mitigation technique for cascaded h-bridge converters with non equal dc link voltages," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1963–1971, 2012.

[26] P. Pejovic, *Three-phase diode rectifiers with low harmonics: current injection methods*. Springer Science & Business Media, 2007.

[27] P. Salmeron and S. P. Litran, "Improvement of the electric power quality using series active and shunt passive filters," *IEEE transactions on power delivery*, vol. 25, no. 2, pp. 1058–1067, 2009.

[28] T. M. Undeland and W. P. Robbins, *Power electronics: converters, applications and design*. Wiley, 2003.

[29] W. M. Grady and S. Santoso, "Understanding power system harmonics," *IEEE Power Engineering Review*, vol. 21, no. 11, pp. 8–11, 2001.

[30] W. Galli, T. Skvarenina, B. Chowdhury, and H. Akagi, "Power quality and utility interface issues," *The Power Electronics Handbook*, pp. 1–48, 2002.

[31] A. M. Mohammed, "Analysis and simulation of shunt active power filter for harmonic cancellation of non linear loads," *Engineering and Technology Journal*, vol. 28, no. 16, pp. 5188–5199, 2010.

[32] A. Jacob, B. T. Abraham, N. Prakash, and R. Philip, "A review of active power filters in power system applications," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, vol. 3, no. 6, pp. 10 253–10 261, 2014.

[33] H. A. Kazem, "Harmonic mitigation techniques applied to power distribution networks," *Advances in power electronics*, vol. 2013, 2013.

[34] J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo, and M. A. Aguirre, "Selective harmonic mitigation technique for high-power converters," *IEEE Transactions on Industrial electronics*, vol. 57, no. 7, pp. 2315–2323, 2009.

[35] E. Hossain, M. R. Tür, S. Padmanaban, S. Ay, and I. Khan, "Analysis and mitigation of power quality issues in distributed generation systems using custom power devices," *Ieee Access*, vol. 6, pp. 16 816–16 833, 2018.

[36] G. C. de Miranda, H. F. Primo, H. T. Calenzani, and I. A. Camargos, "Harmonic mitigation techniques applied to industrial power systems: Real case study with measurements," in *2018 Simposio Brasileiro de Sistemas Eletricos (SBSE)*. IEEE, 2018, pp. 1–6.

[37] G. L. Skibinski, N. Guskov, and D. Zhou, "Cost effective multi-pulse transformer solutions for harmonic mitigation in ac drives," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.*, vol. 3. IEEE, 2003, pp. 1488–1497.

[38] G. M. Carvajal, G. O. Plata, W. G. Picon, and J. C. C. Velasco, "Investigation of phase shifting transformers in distribution systems for harmonics mitigation," in *2014 Clemson University Power Systems Conference*. IEEE, 2014, pp. 1–5.

[39] X. Liang and C. Andalib-Bin-Karim, "Harmonics and mitigation techniques through advanced control in grid-connected renewable energy sources: A review," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3100–3111, 2018.

[40] A. B. Nassif, W. Xu, and W. Freitas, "An investigation on the selection of filter topologies for passive filter applications," *IEEE transactions on Power Delivery*, vol. 24, no. 3, pp. 1710–1718, 2009.

[41] T. C. Sekar and B. J. Rabi, "A review and study of harmonic mitigation techniques," in *2012 International Conference on Emerging Trends in Electrical Engineering and Energy Management (ICETEEEM)*. IEEE, 2012, pp. 93–97.

[42] R. C. Fernandes, P. da Silva Oliveira, and F. J. M. de Seixas, "A family of autoconnected transformers for 12-and 18-pulse convertersgeneralization for delta and wye topologies," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 2065–2078, 2010.

[43] M. El-Habrouk, M. Darwish, and P. Mehta, "Active power filters: A review," *IEE Proceedings-Electric Power Applications*, vol. 147, no. 5, pp. 403–413, 2000.

[44] J. He, Y. W. Li, F. Blaabjerg, and X. Wang, "Active harmonic filtering using current-controlled, grid-connected dg units with closed-loop power control," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 642–653, 2013.

[45] H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous power theory and applications to power conditioning*. John Wiley & Sons, 2017.

[46] S. Inoue, T. Shimizu, and K. Wada, "Control methods and compensation characteristics of a series active filter for a neutral conductor," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 433–440, 2007.

[47] A. Emadi, A. Nasiri, and S. B. Bekiarov, *Uninterruptible power supplies and active filters*. CRC press, 2017.

[48] M. McGranaghan, "Active filter design and specification for control of harmonics in industrial and commercial facilities," *Knoxville TN, USA: Electrotek Concepts, Inc*, vol. 30, 2001.

[49] H. Akagi, "Active harmonic filters," *Proceedings of the IEEE*, vol. 93, no. 12, pp. 2128–2141, 2005.

[50] M. I. M. Montero, E. R. Cadaval, and F. B. Gonzalez, "Comparison of control strategies for shunt active power filters in three-phase four-wire systems," *IEEE transactions on power electronics*, vol. 22, no. 1, pp. 229–236, 2007.

[51] S. A. Gonzalez, R. Garcia-Retegui, and M. Benedetti, "Harmonic computation technique suitable for active power filters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2791–2796, 2007.

[52] K. Borisov, H. Ginn III, and G. Chen, "A computationally efficient rdft-based reference signal generator for active compensators," *IEEE Transactions on Power Delivery*, vol. 24, no. 4, pp. 2396–2404, 2009.

[53] S. U. Bhople and S. K. Rayarao, "Comparison of various reference current generation techniques for performance analysis of shunt active power filter using matlab simulation," *International Journal of Current Engineering and Technology*, vol. 6, no. 2, pp. 606–611, 2016.

[54] S. Wamane, J. Baviskar, and S. Wagh, "A comparative study on compensating current generation algorithms for shunt active filter under non-linear load conditions," *Int. J. Sci. Res. Publ*, vol. 3, no. 6, pp. 1–6, 2013.

[55] S. Karvekar and A. Kumbhojkar, "Comparison of different methods of reference current generation for shunt active power filter under balanced and unbalanced load conditions," in *2013 International Conference on Circuits, Power and Computing Technologies (ICCPCT)*. IEEE, 2013, pp. 430–434.

[56] M. A. Ikramullah and A. Rehman, "Comparison of reference current generation techniques for shunt active power filter," in *2018 5th International Conference on Electrical and Electronic Engineering (ICEEE)*. IEEE, 2018, pp. 62–66.

[57] S. Biricik, S. Redif, Ö. C. Özerdem, S. K. Khadem, and M. Basu, "Real-time control of shunt active power filter under distorted grid voltage and unbalanced load condition using self-tuning filter," *IET Power Electronics*, vol. 7, no. 7, pp. 1895–1905, 2014.

[58] E. Sundaram and M. Venugopal, "On design and implementation of three phase three level shunt active power filter for harmonic reduction using synchronous reference frame theory," *International Journal of Electrical Power & Energy Systems*, vol. 81, pp. 40–47, 2016.

[59] L. S. Czarnecki, "Effect of supply voltage harmonics on irp-based switching compensator control," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 483–488, 2009.

[60] K. Senthilnathan, I. Annapoorani, and S. Ravi, "Simulation and hardware implementation of shunt active power filter based on synchronous reference frame theory." *Telkomnika*, vol. 16, no. 1, 2018.

[61] M. Karthikeyan, K. Sharmilee, P. Balasubramaniam, N. Prakash, M. R. Babu, V. Subramaniyaswamy, and S. Sudhakar, "Design and implementation of ann-based sapf approach for current harmonics mitigation in industrial power systems," *Microprocessors and Microsystems*, p. 103194, 2020.

[62] Y. Hoon, M. A. Mohd Radzi, M. K. Hassan, and N. F. Mailah, "Control algorithms of shunt active power filter for harmonics mitigation: A review," *Energies*, vol. 10, no. 12, p. 2038, 2017.

[63] D. Yazdani, A. Bakhshai, G. Joós, and M. Mojiri, "A real-time extraction of harmonic and reactive current in a nonlinear load for grid-connected converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2185–2189, 2009.

[64] A. Marquez Alcaide, J. I Leon, M. Laguna, F. Gonzalez-Rodriguez, R. Portillo, E. Zafra-Ratia, S. Vazquez, L. G Franquelo, S. Bayhan, and H. Abu-Rub, "Real-time selective harmonic mitigation technique for power converters based on the exchange market algorithm," *Energies*, vol. 13, no. 7, p. 1659, 2020.

[65] A. Moeini and S. Wang, "A dc link sensor-less voltage balancing technique for cascaded h-bridge multilevel converters with asymmetric selective harmonic current mitigation-pwm," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7571–7581, 2017.

[66] A. Moeini, H. Zhao, and S. Wang, "A current-reference-based selective harmonic current mitigation pwm technique to improve the performance of cascaded h-bridge multilevel active rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 727–737, 2016.

[67] R. S. Herrera and P. Salmerón, "Instantaneous reactive power theory: A reference in the nonlinear loads compensation," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2015–2022, 2009.

[68] A. Teke, L. Saribulut, and M. Tumay, "A novel reference signal generation method for power-quality improvement of unified power-quality conditioner," *IEEE Transactions on power delivery*, vol. 26, no. 4, pp. 2205–2214, 2011.

[69] M. Popescu, A. Bitoleanu, and V. Suru, "A dsp-based implementation of the pq theory in active power filtering under nonideal voltage conditions," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 880–889, 2012.

[70] S. K. Chauhan, M. C. Shah, R. R. Tiwari, and P. Tekwani, "Analysis, design and digital implementation of a shunt active power filter with different schemes of reference current generation," *IET Power Electronics*, vol. 7, no. 3, pp. 627–639, 2013.

[71] S. Devassy and B. Singh, "Control of a solar photovoltaic integrated universal active power filter based on a discrete adaptive filter," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 7, pp. 3003–3012, 2017.

[72] J. Moriano, M. Rizo, E. J. Bueno, R. Martin, and F. J. Rodriguez, "A novel multifrequency current reference calculation to mitigate active power fluctuations," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 810–818, 2017.

[73] Y. Hoon, M. A. M. Radzi, M. K. Hassan, and N. F. Mailah, "Operation of three-level inverter-based shunt active power filter under nonideal grid voltage conditions with dual fundamental component extraction," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7558–7570, 2017.

[74] Y. Terriche, S. Golestan, J. M. Guerrero, D. Kerdoune, and J. C. Vasquez, "Matrix pencil method-based reference current generation for shunt active power filters," *IET Power Electronics*, vol. 11, no. 4, pp. 772–780, 2017.

[75] P. K. Ray, "Power quality improvement using vllms based adaptive shunt active filter," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 2, pp. 154–162, 2018.

[76] H. Chen, H. Liu, Y. Xing, and H. Hu, "Enhanced dft-based controller for selective harmonic compensation in active power filters," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8017–8030, 2018.

[77] S. Devassy and B. Singh, "Implementation of solar photovoltaic system with universal active filtering capability," *IEEE Transactions on Industry Applications*, 2019.

[78] S. Feng, J. Lei, J. Zhao, W. Chen, and F. Deng, "Improved reference generation of active and reactive power for matrix converter with model predictive control under input disturbances," *IEEE Access*, vol. 7, pp. 97 001–97 012, 2019.

[79] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on industrial electronics*, vol. 53, no. 5, pp. 1398–1409, 2006.

[80] I. J. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, "Control for grid-connected and intentional islanding operations of distributed power generation," *IEEE transactions on industrial electronics*, vol. 58, no. 1, pp. 147–157, 2010.

[81] O. Carranza, E. Figueres, G. Garcerá, and L. Gonzalez, "Comparative study of speed estimators with highly noisy measurement signals for wind energy generation systems," *Applied Energy*, vol. 88, no. 3, pp. 805–813, 2011.

[82] E. Figueres, G. Garcerá, J. Sandia, F. Gonzalez-Espin, and J. C. Rubio, "Sensitivity study of the dynamics of three-phase photovoltaic inverters with an lcl grid filter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 3, pp. 706–717, 2008.

[83] M. P. Kazmierkowski, R. Krishnan, F. Blaabjerg, and J. Irwin, *Control in power electronics: selected problems*. Academic press, 2002.

[84] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "Frequency response analysis of current controllers for selective harmonic compensation in active power filters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 337–347, 2008.

[85] T.-V. Tran, T.-W. Chun, H.-H. Lee, H.-G. Kim, and E.-C. Nho, "Pll-based seamless transfer control between grid-connected and islanding modes in grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5218–5228, 2013.

[86] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase plls: A review of recent advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1894–1907, 2016.

[87] D. Velasco, C. Trujillo, G. Garcera, and E. Figueres, "An active anti-islanding method based on phase-pll perturbation," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1056–1066, 2010.

[88] G.-C. Hsieh and J. C. Hung, "Phase-locked loop techniques. a survey," *IEEE Transactions on industrial electronics*, vol. 43, no. 6, pp. 609–615, 1996.

[89] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. Torres, and A. F. Souza, "Comparison of three single-phase pll algorithms for ups applications," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2923–2932, 2008.

[90] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Transactions on power electronics*, vol. 24, no. 3, pp. 654–664, 2009.

[91] S.-K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Transactions on Power electronics*, vol. 15, no. 3, pp. 431–438, 2000.

[92] F. Hans, W. Schumacher, and L. Harnefors, "Small-signal modeling of three-phase synchronous reference frame phase-locked loops," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5556–5560, 2017.

[93] A. Kulkarni and V. John, "Design of synchronous reference frame phase-locked loop with the presence of dc offsets in the input voltage," *IET Power Electronics*, vol. 8, no. 12, pp. 2435–2443, 2015.

[94] F. González-Espín, E. Figueres, and G. Garcerá, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 6, pp. 2718–2731, 2011.

[95] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Transactions on Industry applications*, vol. 33, no. 1, pp. 58–63, 1997.

[96] N. Hui, D. Wang, and Y. Li, "A novel hybrid filter-based pll to eliminate effect of input harmonics and dc offset," *IEEE Access*, vol. 6, pp. 19 762–19 773, 2018.

[97] F. Liccardo, P. Marino, and G. Raimondo, "Robust and fast three-phase pll tracking system," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 221–231, 2010.

[98] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *IEEE Transactions on Industry Applications*, vol. 45, no. 6, pp. 2039–2047, 2009.

[99] Y. Li, J. Yang, H. Wang, W. Ge, and Y. Ma, "A hybrid filtering technique-based pll targeting fast and robust tracking performance under distorted grid conditions," *Energies*, vol. 11, no. 4, p. 973, 2018.

[100] M. Karimi-Ghartemani and M. R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Transactions on Power Systems*, vol. 19, no. 3, pp. 1263–1270, 2004.

[101] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, and A. Bakhshai, "Derivation and design of in-loop filters in phase-locked loop systems," *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 4, pp. 930–940, 2011.

[102] L. Wang, Q. Jiang, L. Hong, C. Zhang, and Y. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4538–4549, 2012.

[103] I. Carugati, S. Maestri, P. G. Donato, D. Carrica, and M. Benedetti, "Variable sampling period filter pll for distorted three-phase systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 321–330, 2011.

[104] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2750–2763, 2013.

[105] L. Wang, Q. Jiang, and L. Hong, "A novel three-phase software phase-locked loop based on frequency-locked loop and initial phase angle detection phase-locked loop," in *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2012, pp. 150–155.

[106] S. Lakshmanan, A. Jain, and B. Rajpourhit, "Analysis and design of adaptive moving average filters based low-gain pll for grid connected solar power converters," in *2015 IEEE Power & Energy Society General Meeting*. IEEE, 2015, pp. 1–5.

[107] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, and J. Doval-Gandoy, "A quasi-type-1 phase-locked loop structure," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6264–6270, 2014.

[108] J. Wang, J. Liang, F. Gao, L. Zhang, and Z. Wang, "A method to improve the dynamic performance of moving average filter-based pll," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5978–5990, 2014.

[109] Y. Terriche, J. M. Guerrero, and J. C. Vasquez, "Performance improvement of shunt active power filter based on non-linear least-square approach," *Electric Power Systems Research*, vol. 160, pp. 44–55, 2018.

[110] F. A. Neves, M. C. Cavalcanti, H. E. P. de Souza, F. Bradaschia, E. J. Bueno, and M. Rizo, "A generalized delayed signal cancellation method for detecting fundamental-frequency positive-sequence three-phase signals," *IEEE Transactions on power delivery*, vol. 25, no. 3, pp. 1816–1825, 2010.

[111] J. Roldan-Perez, A. Garcia-Cerrada, M. Ochoa-Gimenez, and J. L. Zamora-Macho, "Delayed-signal-cancellation-based sag detector for a dynamic voltage restorer in distorted grids," *IEEE Transactions on Sustainable Energy*, 2018.

[112] M. Xie, H. Wen, C. Zhu, and Y. Yang, "A method to improve the transient response of dq-frame cascaded delayed-signal-cancellation pll," *Electric Power Systems Research*, vol. 155, pp. 121–130, 2018.

[113] T. Ren, H. Ding, Y. Xu, Z. Zhao, L. Chen, Y. Huang, and J. Zhou, "A new open-loop synchronization method based on compensation of phase deviation for pulsed generator converter," *IEEE Transactions on Plasma Science*, vol. 46, no. 10, pp. 3307–3312, 2018.

[114] Y. F. Wang and Y. W. Li, "Grid synchronization pll based on cascaded delayed signal cancellation," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1987–1997, 2010.

[115] P. S. Nascimento, H. E. de Souza, F. A. Neves, and L. R. Limongi, "Fpga implementation of the generalized delayed signal cancelationphase locked loop method for detecting harmonic sequence components in three-phase signals," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 645–658, 2012.

[116] J. Svensson, M. Bongiorno, and A. Sannino, "Practical implementation of delayed signal cancellation method for phase-sequence separation," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 18–26, 2006.

[117] S. Golestan, M. Ramezani, J. M. Guerrero, and M. Monfared, "dq-frame cascaded delayed signal cancellation-based pll: Analysis, design, and comparison with moving average filter-based pll," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1618–1632, 2014.

[118] S. Gude and C.-C. Chu, "Single-phase multiple delayed signal cancellation filter-based enhanced phase-locked loop for accurate estimations of grid voltage information," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2018, pp. 5664–5669.

[119] Q. Huang and K. Rajashekara, "An improved delayed signal cancellation pll for fast grid synchronization under distorted and unbalanced grid condition," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4985–4997, 2017.

[120] S. Gude and C.-C. Chu, "Three-phase plls by using frequency adaptive multiple delayed signal cancellation prefilters under adverse grid conditions," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3832–3844, 2018.

[121] M. Chen, L. Peng, B. Wang, and W. Wu, "Accurate and fast harmonic detection based on the generalized trigonometric function delayed signal cancellation," *IEEE Access*, vol. 7, pp. 3438–3447, 2019.

[122] D. Yazdani, M. Pahlevaninezhad, and A. Bakhshai, "Three-phase grid synchronization techniques for grid connected converters in distributed generation systems," in *2009 IEEE International Symposium on Industrial Electronics*. IEEE, 2009, pp. 1105–1110.

[123] B. Wang, U. Manandhar, X. Zhang, H. B. Gooi, and A. Ukil, "Deadbeat control for hybrid energy storage systems in dc microgrids," *IEEE Transactions on Sustainable Energy*, vol. 10, no. 4, pp. 1867–1877, 2018.

[124] K. Ruanmakok, K. Areerak, K. Areerak, and W. Sangtungtong, "The control of shunt active power filter using sliding mode controller," in *2014 11th international conference on electrical engineering/electronics, computer, telecommunications and information technology (ECTI-CON)*. IEEE, 2014, pp. 1–5.

[125] J. Morales, L. G. de Vicuña, R. Guzman, M. Castilla, and J. Miret, "Modeling and sliding mode control for three-phase active power filters using the vector operation technique," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 9, pp. 6828–6838, 2018.

[126] D. Cao and J. Fei, "Adaptive fractional fuzzy sliding mode control for three-phase active power filter," *IEEE Access*, vol. 4, pp. 6645–6651, 2016.

[127] A. Garcia-Cerrada, O. Pinzón-Ardila, V. Feliu-Batlle, P. Roncero-Sánchez, and P. García-González, "Application of a repetitive controller for a three-phase active power filter," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 237–246, 2007.

[128] C. Xie, X. Zhao, M. Savaghebi, L. Meng, J. M. Guerrero, and J. C. Vasquez, "Multirate fractional-order repetitive control of shunt active power filter suitable for microgrid applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 809–819, 2016.

[129] A. A. Bento, L. F. Monteiro, and E. R. da Silva, "Fast response one-cycle control strategy for three-phase shunt active power filter," in *2017 IEEE Southern Power Electronics Conference (SPEC)*. IEEE, 2017, pp. 1–7.

[130] E. Durna, "Adaptive fuzzy hysteresis band current control for reducing switching losses of hybrid active power filter," *IET Power Electronics*, vol. 11, no. 5, pp. 937–944, 2018.

[131] N. M. Ismail and M. K. Mishra, "Study on the design and switching dynamics of hysteresis current controlled four-leg voltage source inverter for load compensation," *IET Power Electronics*, vol. 11, no. 2, pp. 310–319, 2017.

[132] G. Adam, A. G. Stan, and G. Livinţ, "An adaptive hysteresis band current control for three phase shunt active power filter u sing fuzzy logic," in *2012 International Conference and Exposition on Electrical and Power Engineering*. IEEE, 2012, pp. 324–329.

[133] H. Komurcugil, "Double-band hysteresis current-controlled single-phase shunt active filter for switching frequency mitigation," *International Journal of Electrical Power & Energy Systems*, vol. 69, pp. 131–140, 2015.

[134] A. Belonkar and M. Salodkar, "Performance analysis of shunt active power filter with different switching signal generation techniques," in *Presentado en Recent Advances and Applications of Electrical Engineering: Proceedings of the 9th WSEAS International Conference on Applications of Electrical Engineering (AEE10), Penang, Malaysia*, 2013.

[135] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "High performance current controller for selective harmonic compensation in active power filters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1826–1835, 2007.

[136] L. Tarisciotti, A. Formentini, A. Gaeta, M. Degano, P. Zanchetta, R. Rabbeni, and M. Pucci, "Model predictive control for shunt active filters with fixed switching frequency," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 296–304, 2016.

[137] S. Shabeer, A. Grover, and A. H. Bhat, "Shunt hybrid power filter for harmonic reduction to improve power quality using pi and hysteresis controller," *International Journal of Computer Applications*, vol. 147, no. 4, 2016.

[138] R. Panigrahi and B. Subudhi, "Performance enhancement of shunt active power filter using a kalman filter-based h-infinity control strategy," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2622–2630, 2016.

[139] T. Hornik and Q.-C. Zhong, "A current-control strategy for voltage-source inverters in microgrids based on h-infinity and repetitive control," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 943–952, 2010.

[140] M. A. Ikramullah and A. Rehman, "Performance analysis of current injection techniques for shunt active power filter," in *IOP Conference Series: Earth and Environmental Science*, vol. 168, no. 1. IOP Publishing, 2018, p. 012014.

[141] G. Arunsankar and S. Srinath, "Optimal controller for mitigation of harmonics in hybrid shunt active power filter connected distribution system: An egoann technique," *Journal of Renewable and Sustainable Energy*, vol. 11, no. 2, p. 025507, 2019.

[142] Ikramullah and M. Ashraf, "Sliding mode control for performance improvement of shunt active power filter," *SN Applied Sciences*, vol. 1, no. 6, p. 531, 2019.

[143] A. Arivarasu, K. Muthukumar, and R. Balasubramanian, "Closed loop non linear control of shunt hybrid power filter for harmonics mitigation in industrial distribution system," *International Journal of Power Electronics and Drive Systems*, vol. 5, no. 2, p. 185, 2014.

[144] P. Acuna, L. Moran, M. Rivera, J. Dixon, and J. Rodriguez, "Improved active power filter performance for renewable power generation systems," *IEEE transactions on power electronics*, vol. 29, no. 2, pp. 687–694, 2013.

[145] E. Sreeraj, E. Prejith, K. Chatterjee, and S. Bandyopadhyay, "An active harmonic filter based on one-cycle control," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 3799–3809, 2013.

[146] W. Jiang, X. Ding, Y. Ni, J. Wang, L. Wang, and W. Ma, "An improved deadbeat control for a three-phase three-line active power filter with current-tracking error compensation," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2061–2072, 2017.

[147] D. J. Hogan, F. J. Gonzalez-Espin, J. G. Hayes, G. Lightbody, and R. Foley, "An adaptive digital-control scheme for improved active power filtering under distorted grid conditions," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 988–999, 2017.

[148] A. Abrishamifar, A. Ahmad, and M. Mohamadian, "Fixed switching frequency sliding mode control for single-phase unipolar inverters," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2507–2514, 2011.

[149] S. D. Swain, P. K. Ray, and K. B. Mohanty, "Improvement of power quality using a robust hybrid series active power filter," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3490–3498, 2016.

[150] V. S. Bandal and P. N. Madurwar, "Performance analysis of shunt active power filter using sliding mode control strategies," in *2012 12th International Workshop on Variable Structure Systems*. IEEE, 2012, pp. 214–219.

[151] S. R. Mohapatra and P. K. Ray, "A fixed switching frequency adaptive sliding mode controller for shunt active power filter system," in *TENCON 2014-2014 IEEE Region 10 Conference*. IEEE, 2014, pp. 1–6.

[152] R. Dian, W. Xu, and C. Mu, "Improved negative sequence current detection and control strategy for h-bridge three-level active power filter," *IEEE Transactions on Applied Superconductivity*, vol. 26, no. 7, pp. 1–5, 2016.

[153] M. A. A. M. Zainuri, M. A. M. Radzi, A. C. Soh, N. Mariun, and N. A. Rahim, "Dc-link capacitor voltage control for single-phase shunt active power filter with step size error cancellation in self-charging algorithm," *IET Power Electronics*, vol. 9, no. 2, pp. 323–335, 2016.

[154] K.-H. Tan, F.-J. Lin, and J.-H. Chen, "Dc-link voltage regulation using rpfnn-amf for three-phase active power filter," *IEEE Access*, vol. 6, pp. 37 454–37 463, 2018.

[155] Y. Hoon, M. Mohd Radzi, M. Hassan, and N. Mailah, "Dc-link capacitor voltage regulation for three-phase three-level inverter-based shunt active power filter with inverted error deviation control," *Energies*, vol. 9, no. 7, p. 533, 2016.

[156] Z. Nie and N. Schofield, "Multi-phase vsi dc-link capacitor considerations," *IET Electric Power Applications*, vol. 13, no. 11, pp. 1804–1811, 2019.

[157] W.-H. Choi, C.-S. Lam, M.-C. Wong, and Y.-D. Han, "Analysis of dc-link voltage controls in three-phase four-wire hybrid active power filters," *IEEE Transactions on power electronics*, vol. 28, no. 5, pp. 2180–2191, 2012.

[158] M. Mellincovsky, V. Yuhimenko, Q.-C. Zhong, M. M. Peretz, and A. Kuperman, "Active dc link capacitance reduction in grid-connected power conversion systems by direct voltage regulation," *IEEE Access*, vol. 6, pp. 18 163–18 173, 2018.

[159] R. R. Nasyrov and R. I. Aljendy, "Comprehensive comparison between hybrid fuzzy-pi and pso-pi controllers based active power filter for compensation of harmonics and reactive power under different load conditions," in *2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus)*. IEEE, 2018, pp. 725–730.

[160] R. S. Herrera, P. Salmerón, and H. Kim, "Instantaneous reactive power theory applied to active power filter compensation: Different approaches, assessment, and experimental results," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 184–196, 2008.

[161] M. Kesler and E. Ozdemir, "Synchronous-reference-frame-based control method for upqc under unbalanced and distorted load conditions," *IEEE transactions on industrial electronics*, vol. 58, no. 9, pp. 3967–3975, 2010.

[162] T. Messo, J. Jokipii, J. Puukko, and T. Suntio, "Determining the value of dc-link capacitance to ensure stable operation of a three-phase photovoltaic inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 665–673, 2013.

[163] T. Mannen and H. Fujita, "A dc capacitor voltage control method for active power filters using modified reference including the theoretically derived voltage ripple," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4179–4187, 2016.

[164] D. Sreenivasarao, P. Agarwal, and B. Das, "Performance enhancement of a reduced rating hybrid d-statcom for three-phase, four-wire system," *Electric power systems research*, vol. 97, pp. 158–171, 2013.

[165] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 765–778, 2012.

[166] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Performance improvement of a prefiltered synchronous-reference-frame pll by using a pid-type loop filter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3469–3479, 2013.

[167] Y. Han, M. Luo, C. Chen, A. Jiang, X. Zhao, and J. M. Guerrero, "Performance evaluations of four maf-based pll algorithms for grid-synchronization of three-phase grid-connected pwm inverters and dgs," *Journal of Power Electronics*, vol. 16, no. 5, pp. 1904–1917, 2016.

[168] Ikramullah and M. Ashraf, "Comparison of synchronization techniques under distorted grid conditions," *IEEE Access*, vol. 7, pp. 101 345–101 354, 2019.

[169] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, and J. Doval-Gandoy, "An efficient implementation of generalized delayed signal cancellation pll," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1085–1094, 2015.

[170] M. Iravani, E. Lavers, P. Lehn, D. Durbak, D. Fletcher, P. Wilson, R. Wachal, K. Sen, J. Martinez, B. Johnson *et al.*, "A benchmark system for digital time-domain simulation of an active power filter," *IEEE Transactions on Power Delivery*, vol. 20, no. 1, pp. 234–241, 2005.

[171] A.-H. M. Abu-Jalala, T. Cox, C. Gerada, M. Rashed, T. Hamiti, and N. Brown, "Power quality improvement of synchronous generators using an active power filter," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4080–4090, 2018.

[172] S. Samal, A. Hota, P. K. Hota, and P. K. Barik, "Srf based shunt active power filter integrated with microgrid for harmonics mitigation," *International Journal of Innovative Technology and Exploring Engineering*, pp. 869–874, 2019.