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Analytical and DNN Based Prediction of DC Characteristics of Nanoscale FinFETs

by

Qamaruddin

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Analytical and DNN Based Prediction of DC Characteristics of Nanoscale FinFETs

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This is to certify that the research work presented in the thesis, entitled "**Analytical and DNN Based Prediction of DC Characteristics of Nanoscale FinFETs**" was conducted under the supervision of **Dr. Muhammad Mansoor Ahmed**. No part of this thesis has been submitted anywhere else for any other degree. This thesis is submitted to the **Department of Electrical Engineering, Capital University of Science and Technology** in partial fulfillment of the requirements for the degree of Doctor in Philosophy in the field of **Electrical Engineering**. The open defence of the thesis was conducted on **December 09, 2022**.

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1. Q. U. D. Memon, U. F. Ahmed and M. M. Ahmed. "A Unified Depletion/Inversion Model for Heterojunction Trigate FinFETs DC Characteristics," *IEEE Access* 9(2021), 89768-89777.

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Abstract

Si technology has played a vital role in today's semiconductor industry and a number of Si based devices have been invented, but none of them got more attention than field effect transistors (FETs). The scaling of FETs was successfully carried out upto 100 nm, but further downscaling was halted due to short channel effects and high leakage current. In order to overcome these problems, FinFETs were introduced which had a 3D channel that inherently provided a better gate on the channel characteristics. In this research, various modeling techniques for FinFETs DC characteristics have been developed to further its advancement for high-tech industry.

The first part of this research presents the development of a comprehensive model for trigate AlGaN/GaN FinFETs DC characteristics both for depletion and inversion mode of operations. For the depletion mode, 2DEG carrier concentration has been evaluated to assess drain current (I_{2D}). Increase in gate potential after having fully un-depleted 2DEG, caused a corresponding increase in the drain current which could possibly be associated with the creation of additional channels in the device due to carriers inversion process. This component of the drain current (I_{inv}) has been modeled by solving a 2D Poisson equation. It has been shown that the total drain current $I_{ds} = I_{inv} + I_{\mathrm{2D}}$. The validity of the developed technique has been demonstrated using experimental data which exhibited a good degree of accuracy.

Second part of the thesis focuses on a Schrödinger-Poisson based technique to predict DC characteristics of trigate Si FinFETs. The channel characteristics are modeled by a 3D Schrödinger wave equation considering quantum-mechanical ballistic transport. Using a non-equilibrium green function (NEGF) and a 3D Poisson equation, drain current associated with source-drain Fermi energy difference is evaluated. Contact resistance and its impact on the drain current is adjusted using a modeled parameter in Fermi-Dirac distribution function. To validate the proposed model, output and transfer characteristics of nanoscale FinFETs are compared with experimental data and a good degree of accuracy is demonstrated.

It has been shown that the proposed model has the ability to predict FinFETs characteristics having $T_{fin} = 3 - 35$ nm.

Third part of thesis presents a deep neural network (DNN) model which has been designed to predict DC characteristics of FinFETs prior to their fabrication. To train the model, a sizable dataset has been generated using COMSOL software by varying device fabrication parameters. The model was then trained to a good degree of accuracy with selected dataset of FinFET characteristics, followed by an assessment of training accuracy using the control data. It has been demonstrated that the developed technique has the ability to predict DC characteristics of nanoscale FinFETs by using those variables which are handled by a design engineer. It is further shown that the technique is highly efficient when compared with standard simulation softwares hence, providing the industry a potential time and cost efficient solution.

Contents

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Abbreviations

2DEG	2 dimensional electron gas
AC	Alternating current
ADS	Advance software design
Al	Aluminum
AlGaAs	Aluminum gallium arsenide
AlGaN	Aluminum gallium nitride
AlN	Aluminum nitride
ANN	Artifical neural network
CAD	Computer aided design
CFET	Conventional field effect transistor
CV	Capacitance–voltage
DC	Direct current
DELTA	Depleted lean channel transistor
DG	Double gate
DIBL	Drian induced barrier lowering
DNN	Deep neural network
DRAM	Dynamic random access memory
FET	Field effect transistor
FinFET	Fin Field effect transistor
GAA	Gate all around
GAAFET	Gate all around field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride

Ge	Germanium
GIDL	Gate induced drain leakage
GTFP	Gain transconductance frequency product
HEMT	High electron mobility transistor
IC	Integrated circuit
$I-V$	Current–voltage
JFET	Junction field effect transistor
MBE	Molecular beam epitaxy
MESFET	Metal semiconductor field effect transistor
MISO	Multiple input single output
ML	Machine Learning
MOSFET	Metal oxide field effect transistor
MSE	Mean square error
NEGF	Non-equilibrium green function
NW	Nanowire
QME	Quantum mechanical effects
RAM	Random acces memory
RF	Radio frequency
RMSE	Root mean square error
SCE	Short channel effect
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
SNM	Static noise margin
SOI	Silicon on insulator
SRAM	Static random access memory
T	Transistor cell
TCAD	Technology computer aided design
TFP	Transconductance frequency product
TSMC	Taiwan semiconductor manufacturing company

Symbols

2D, 3D	2 and 3 dimensional
a	Grid step
α	Fitting parameter
b	Bias value
β	Model parameter
C_{gd}	Gate to drain capacitor
C_{gs}	Gate to source capacitor
C_{ox}	Oxide capacitance
d	Distance between top gate and 2DEG
Δ	Laplace operator
ΔE_c	Bandgap discontinuity
ΔL_g	Channel length modulation
$\mathbf{E}$	Energy of wave function
E	Field inside the channel
ϵ_A	AlGaN permittivity
ϵ_G	GaN permittivity
ϵ_{eff}	Permittivity of 2DEG
ϵ_{si}	Silicon permittivity
ϵ_{ox}	Oxide permittivity
E_c	Lowest conduction band energy
E_F	Fermi energy level
E_g	$E_c - E_v$
E_{sat}	Saturation field

E_v	Valence band energy
E_y	y-directed electric field
f_{max}	Maximum frequeuncy
f_t	Unity gain frequeuncy
$\mathbf{f_{1,2}}$	Fermi-Dirac distribution
$\mathbf{G^n}$	Electron Density Matrix
g_d	Output conductance
g_m	Transconductance
$\mathbf{H}$	Hamiltonian matrix
h	Planks constant
H_{fin}	Fin height
I_{2D}	2DEG current
$I_{\mathrm{2D(l)}}$	2DEG current at linear region
$I_{\mathrm{2D(s)}}$	2DEG current at saturation region
I_{ds}	Drain to source current
I_{ds}^A	Actual drain to source current
I_{ds}^P	Experimental drain to source current
$I_{ds(sat)}$	Drain to source current at saturation region
I_{inv}	Inversion current
k_B	Boltzmann constant
k_i	Wave number
L_{fin}	Fin length
L_g	Gate length
L_{gd}	Gate to drain length
L_{gs}	Gate to source length
L_u	Underlap channel length
M	Number of $I-V$ curves
m	Mass of electron
m^*	Effective mass
N	Number of bias points
N_d	Bulk concentration

n_i	Intrinsic carrier concentration
n_s	2DEG carrier concentration
$P_{1,2}$	Chemical potential energy
Q	Channel charge
Q_i	Inversion charge
q	Electron charge
q_{id}	Electron charges at drain
q_{is}	Electron charges at source
Q_{inv}	Inversion charge
Q_{bulk}	Bulk charge
r	Structure parameter
R_{gd}	Gate to drain resistance
R_{gs}	Gate to source resistance
$\mathbf{s}$	Inflow of electron
T	Temperature
t	Time
T_{fin}	Fin thickness
T_{ox}	Oxide thickness
t_{si}	Silicon thickness
$\mathbf{U}$	Channel potential energy
U_f	Electrochemical Potential
$\mathbf{V}$	Potential energy
V	Applied voltage
V_{ch}	Channel potential
V_d	Drain voltage
v_d	Drift velocity
V_{ds}	$V_d - V_s$
$V_{\mathrm{d(sat)}}$	Drain voltage at saturation point
V_{fb}	Flat band voltage
V_g	Gate voltage
V_{gs}	$V_g - V_s$

V_{GF}	Low drain voltage
V_L	Voltage across length
V_s	Source voltage
V_T	Thermal voltage
V_{th}	Threshold voltage
v_{sat}	Saturation velocity
W	Gate width
w	Weight value
W_{eff}	Effective fin width
W_{fin}	Width of the fin
x, y, z	Co-ordinate system
$\mathbf{\Sigma}$	Rate of outflow of electron
σ	Activation function
$\hbar$	Reduced Plank's constant
λ_i	Eigenvalues
$\lambda_1, \lambda_2, \lambda_3, V_{g1}, V_{g2}$	Model constants
$\zeta_1, \zeta_2, \zeta_3$	Temperature dependent parameter
η	Learning factor
μ	Mobility
μ_0	Low field mobility
ϕ_B	Built in potential
ϕ_b	Schottky barrier height, Metal work function
ψ, ψ_p	Surface potential
ψ_d	Surface potential at drain terminal
ψ_s	Surface potential at source terminal
χ	Electron affinity
ψ_0	Mid channel potential
$\mathbf{\Gamma}$	Hermitian matrix
$\boldsymbol{\psi_{xyz}}$	xyz dependent wave function

Chapter 1

Introduction

The idea of field effect transistor (FET) was initially presented in the first quarter of 20^{th} century however, the inventors were unable to build a working practical semiconducting device based on the proposed concepts [1]. By 1950, the boom in the electronic industry was primarily based on FETs as the large scale integration of these devices flourished the industry. Introduction of FETs in semiconductor industry had increased the number of transistors exponentially on a chip area enabling complex technologies and systems to be developed.

FETs based on their device structure are classified into: a) junction field effect transistors (JFETs); b) metal oxide semiconductor field effect transistors (MOSFETs); c) metal semiconductor field effect transistors (MESFETs) and d) high electron mobility transistors (HEMTs) [2]. JFETs and MOSFETs were the first and second generation FET devices, respectively; and later on MESFETs and HEMTs were introduced; considered as the third generation devices. However, to cope with the ever-growing device scaling, Fin Field Effect Transistors (FinFETs) were first proposed as an alternative solution to JFET technology in 90s by Hisamoto *et al.* [3] and were designed to enhance further scalability of FET technology.

JFET controls the current flow from source-to-drain through a field caused by the gate voltage. Thus, gate terminal plays a crucial role in defining the response of

the device. On account of growing demands of space efficient integrated circuits (IC), the downscaling of JFET was limited due to its higher gate barrier [4] and high gate leakage caused by the narrow bandgap material used in its fabrication [5]. Furthermore, JFET has a high input and low output impedances and the performance of JFETs deteriorates at higher operating frequencies associated with internal Miller capacitors of the device. Improvements in JFET are achieved by growing a layer of Silicon dioxide (SiO_2) on top of Si and by depositing a layer of metal on the very top, and the device thus formed, is called MOSFET [6]. MOSFET is considered a better substitute in semiconductor industry, as it has relatively higher input impedance and a negligible leakage current [5]. MOSFET usage is restricted because of the breakdown of oxide, as the isolation between the gate and channel can be damaged easily by the accumulation of static charges [7]. In addition, both JFET and MOSFET performance deteriorate at higher temperature and this becomes more serious at large scale integration.

MESFET is a field effect transistor similar to JFET with a Schottky junction instead of a *pn*-junction for the gate. In MESFET, compound semiconductor such as, GaAs is used which offers better mobility compared to Si, and thus better high

TABLE 1.1: Fundamental features of various types of FETs

Parameters	**MOSFET**	**MESFET**	**HEMT**
Material	Elemental	Compound	Heterojunction
Input Impedance [8]	Very High ($\sim 10^6$)	High	High
Off Current [5, 9]	∼100 nA	∼10 nA	∼10 nA
Substrate	Semiconductor	Semi insulator	Semi insulator
Types	E & D	D	D
Application [10]	Digital and memory devices	RF and power	Low Noise and mm-wave
Usual gate length [7]	∼100 nm	∼60 nm	∼30 nm

E & D:Enhancement and Depletion

frequency characteristics [11]. To further improve the performance, heterojunction materials such as AlGaN/GaN are used and with the introduction of these materials, focus is shifted towards HEMT technology [12]. HEMT offers higher mobility due to the formation of 2-dimensional electron gas (2DEG) [11], and can operate even below milli kelvin.

However, in all above mentioned devices, scalability remained a major concern. Reduction in the device size generated other associated issues commonly known as short channel effects (SCE) which limited further reduction in the device size and hence, number of components per unit area of the chip. However, by using different compound materials and technology modifications, at the most, 32 nm gate length (L_g) devices are reported [13, 14]. Table 1.1 summarizes the properties and scaling limits of conventional FETs.

Beyond 30 nm, SCEs such as drain induced barrier lowering (DIBL), threshold voltage roll off, compression in transconductance, parasitic capacitance and gate leakage through hot electron tunneling, etc; are observed [15]. To cater these problems while also continuing further device scaling, FinFETs were introduced. FinFET has a 3D channel referred to as fin of the device, which is enveloped by the gate metal from three sides [16]. Due to the gate which is wrapped around the channel from three sides, these devices are also called trigate devices as illustrated

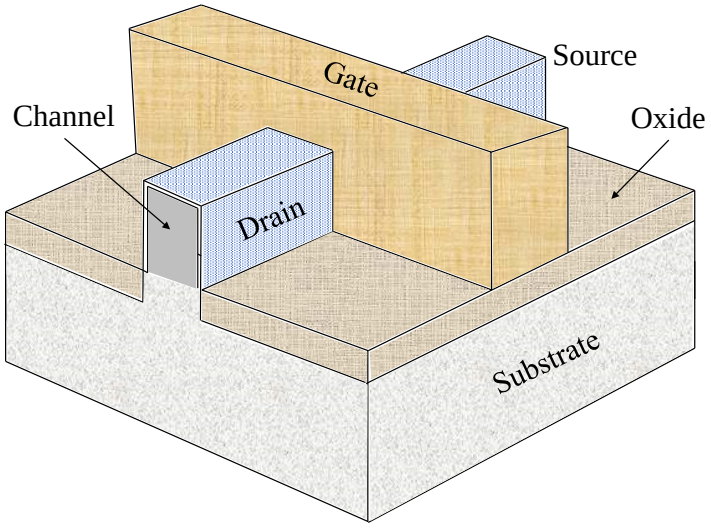

FIGURE 1.1: Crossectional view of a trigate FinFET.

in Fig. 1.1. The 3D gate structure allows better gate control upon the channel current and hence SCEs. The introduction of FinFETs made revolutionary improvements in semiconductor technology and opened a new era of IC scalability [17]. First generation FinFETs were based on double-gate (DG) MOSFET technology with reported L_g down to 14 nm [18]. Currently, trigate FinFET is considered as device of the day having good popularity in semiconductor industry. Now 14 nm / 16 nm trigate FinFET technology has become a mature product whereas researchers are working on nanowire FinFETs with sub 10 nm L_g [19].

1.1 Wide Bandgap Materials

A transistor is made up of a semiconductor material, so the material of the device has a major role in determining its performance. Since 1950, Si has been the most often utilized device material and by 1980, its technology attained highest maturity with score of applications in digital industries. Si based technology had reached to its theoretical limits where further optimization in terms of performance and device miniaturization was hard to achieve. The fundamental constraint on further growth of Si-based technology was its slow switching speed, device performance deterioration at higher temperature and substantial power losses. To improve the devices further, both from device size as well as the performance point of view, scientists and technologists moved towards compound semiconductors such as GaAs, SiC, AlGaAs etc.

GaAs based devices, which are based on a compound semiconductor, gained popularity since these devices have better electron mobility and higher saturation velocity (v_{sat}) when compared to Si-based devices. Although GaAs based devices perform relatively better at higher temperature, yet these suffered with some limitations because, the material itself has been classified as narrow bandgap material, causing constraints on its applications in the industry. Nevertheless, GaAs devices offered greater switching frequencies, allowing them, predominantly, to be employed in low-power microwave industry and satellite communication. Si-based

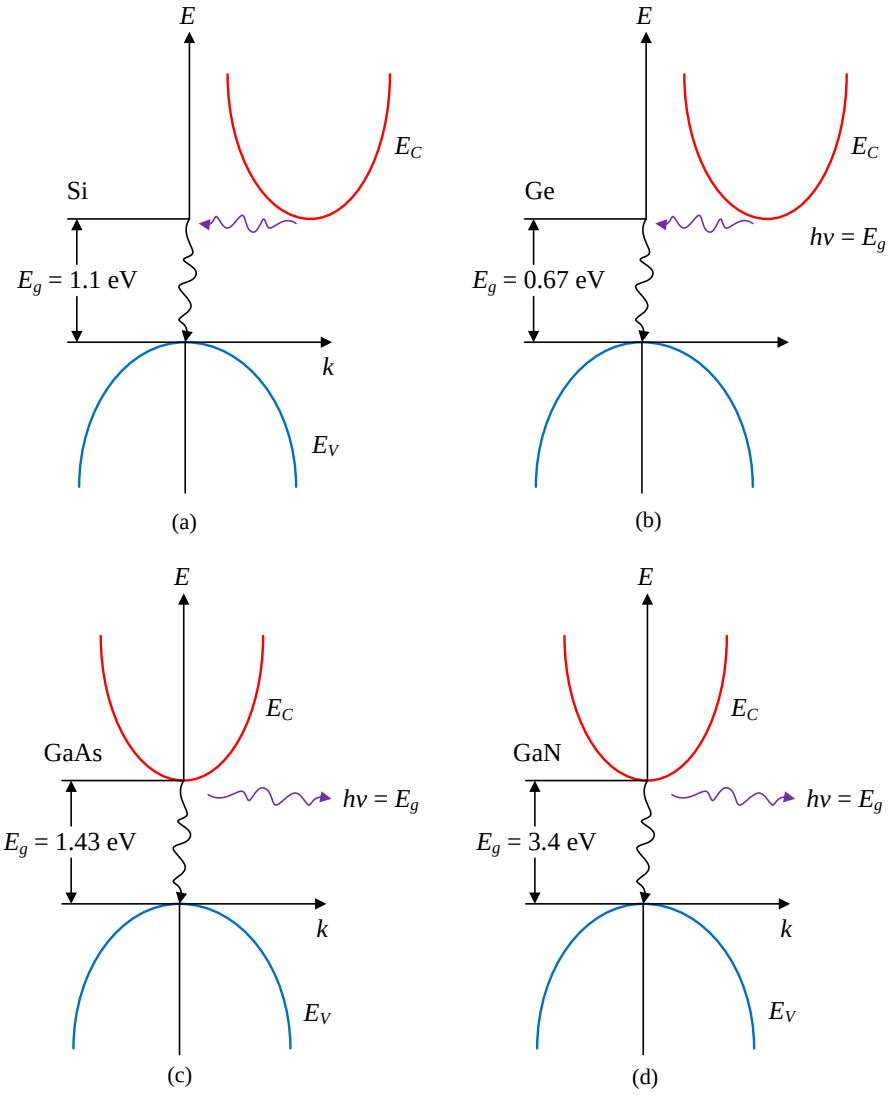

FIGURE 1.2: Band diagram of narrow and wide bandgap materials used in electronic industry.

bipolar devices, on the other hand, have greater power handling capabilities, but low operating frequency ranges. Furthermore, it was also realized that many important applications such as: military; aerospace; automotive; and motor drives required special devices capable to retain their characteristics in harsh environment.

To address these constraints, a new class of material termed as wide bandgap material, was adopted to meet the advanced technological requirements. When compared to its counterparts, wide bandgap materials such as SiC, GaN, AIN, AlGaN etc offer relatively better characteristics, and thus emerged as potential candidates for future generation of electronic devices. Among these wide bandgap materials, GaN and SiC provide high mobility along with high temperature stability; allowing them to deliver higher currents with improved switching frequencies. Such materials can also sustain at high electric field even at higher temperature compared to narrow bandgap materials, and are therefore, promising contender for future generation of devices.

A pictorial representation of narrow and wide bandgap materials is shown in Fig. 1.2. Ge has a indirect bandgap of 0.67 eV, while Si exhibits an indirect bandgap of 1.1 eV. Devices made by these materials fail at higher temperature due to breakdown phenomenon, and hence Si and Ge are not promising candidates for high temperature applications. On the other hand, GaAs has a bandgap of 1.43 eV, making it a relatively better option for semiconductor industry provided other parameters such as mobility and carrier velocity are also supportive. Lastly, as depicted in Fig. 1.2, GaN has a 3.4 eV energy gap and could be called as a wide bandgap material. Additionally it has a bandgap that is nearly triple to Silicon's, owing to that it can handle higher voltages, power, and temperature. Since GaN offers higher carrier velocity, therefore, GaN based devices allow smaller, faster, robust and power efficient devices compared to its narrow bandgap counterparts.

1.2 FinFET−Fin Field Effect Transistor

FinFET is an alternative of planar MOSFET structure. Based on the gate configurations, FinFETs are classified into two categories: a) trigate FinFETs and b) independent gate FinFETs. Fig 1.3 (a) & (b) show a crossectional view of a trigate and independent gate FinFETs, respectively. Independent gate device is a four terminal device, while trigate FinFET is a three terminal device. The gate

of a trigate FinFET maintain a constant potential, called as equi-potential acting on three sides of the channel, while independent gate FinFET may have the same or independent potentials applied on gates. The basic physical dimensions of a FinFET are: gate length L_g; fin thickness T_{fin}; fin length L_{fin}; and height of the fin, H_{fin}. The effective width (W_{eff}) of a FinFET plays a major role in current and is determined by $W_{eff} = 2H_{fin} + T_{fin}$. To increase the drive current of a FinFET, parallel fins may be added to increase W_{eff}. On the other hand, H_{fin} to T_{fin} ratio should be kept less than 3, to mitigate the SCEs [20]. The energy band diagram of an n–channel FinFETs is shown in Fig 1.4. This figure shows a biased system having an oxide layer sandwich with n–type semiconductor and the gate metal. In Fig. 1.4, apart from other usual variables ϕ_b represents work-function of the gate metal, E_F is the Fermi energy, E_c energy of the conduction and E_v represents the valance band energy.

A further down scaling of FinFETs is considered as a challenging task both for the researchers and the industry because, as the channel of a FinFET becomes smaller, a variety of effects such as hot carrier effects, velocity overshoot, shift in threshold voltages and degradation of mobility due to surface scattering are observed [21]. To minimize these effects, heterostructure FinFETs are proposed [22] which also provide solution for SCEs especially those related to mobility degradation and thus, eases further scalability in FET devices.

1.3 Heterostructure FinFET

Over the many years, a lot of improvements have been suggested involving structure optimization of FinFET. As the technology advanced and inventions of new gadgets and other electronic devices flooded the market, one of the key demands pertaining to device operation was its ability to perform in an unfriendly environment, where most of the other devices either fail or exhibit an uncertain behavior. Researchers have been able to fabricate heterojunction FinFETs by combining two mis-matched semiconductor layers such as, AlGaN/GaN. A combination of such

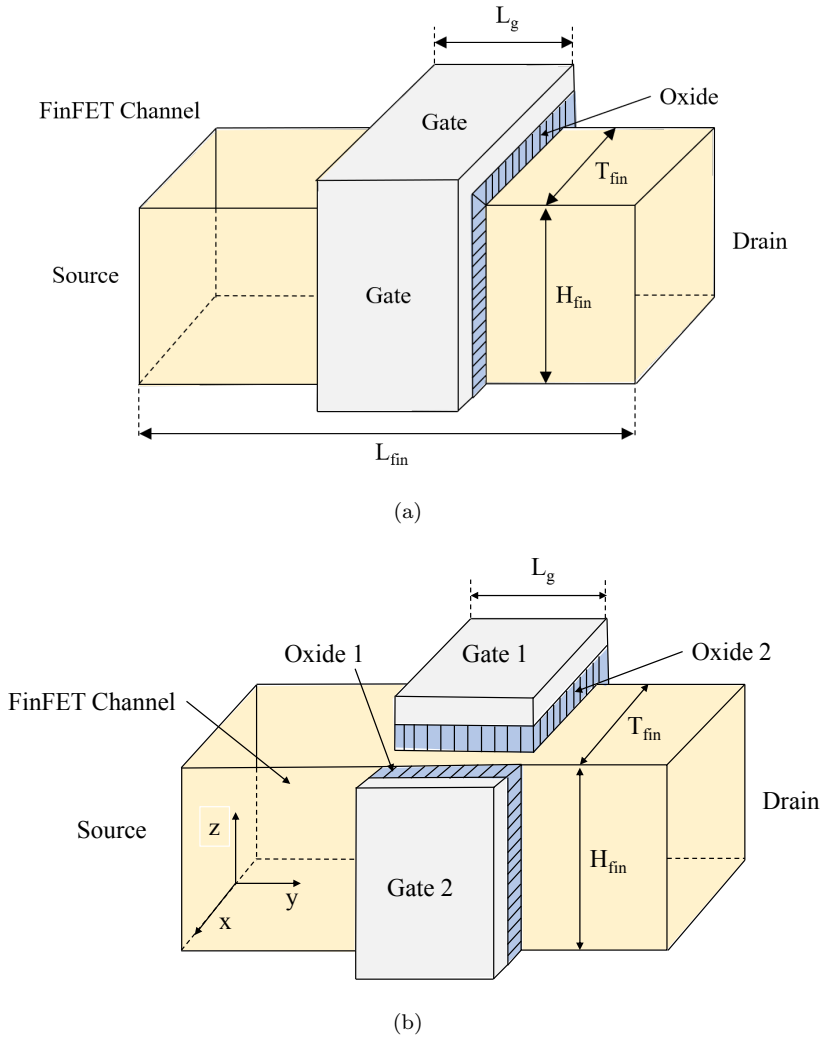

FIGURE 1.3: (a) Trigate and (b) independent gate FinFETs.

two layers, because of mis-matched bandgap, allows the free electrons to trap at the interface of the two materials, defining a charge layer referred to as 2DEG also shown in Fig. 1.5 [23, 24]. Electrons once trapped in 2DEG are available for conduction at below liquid helium temperature. The devices made by such a material, offer stable characteristics for a wide range of temperatures, starting from milli kelvin to a reasonably high temperature observed in automobile and other engine environments. Additionally, charges trapped in the form of 2DEG are not associated with lattice atoms, rather they are trapped in a quantum well, therefore, they offer superior mobility and high v_{sat} when compared with bulk materials.

Wide bandgap heterostructure offers an additional benefit, because of piezoelectric

effect [25] observed in such materials. This effect allows a natural generation of carriers and their trapping in the quantum well without involving the spacer layer to reduce the ionized ions scattering. Thus, the devices made from such a heterojunction, offer better mobility along with the ease of fabrication, and owing to that, heterostructure FinFETs are preferred in the industry [26].

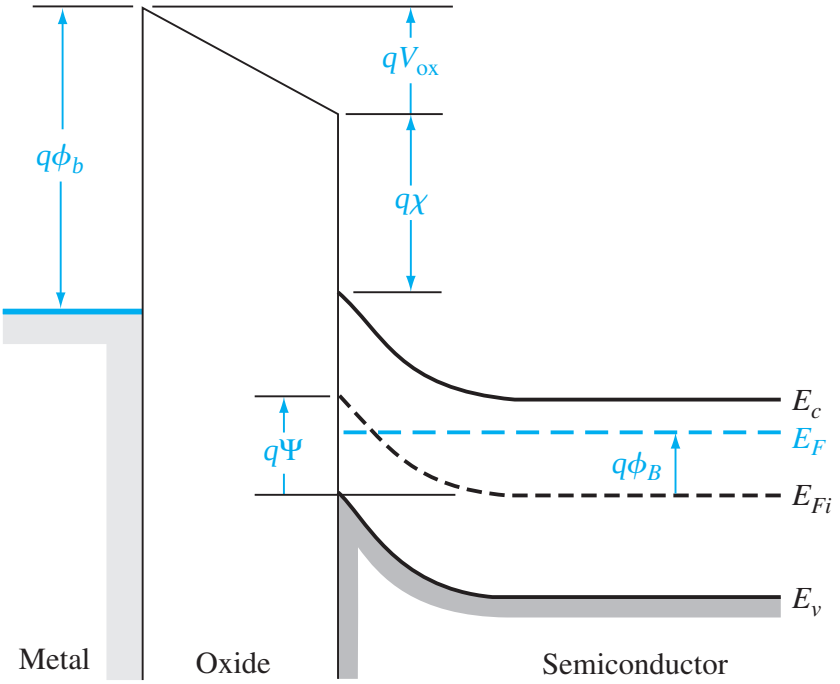

FIGURE 1.4: Energy band diagram of n channel FinFETs.

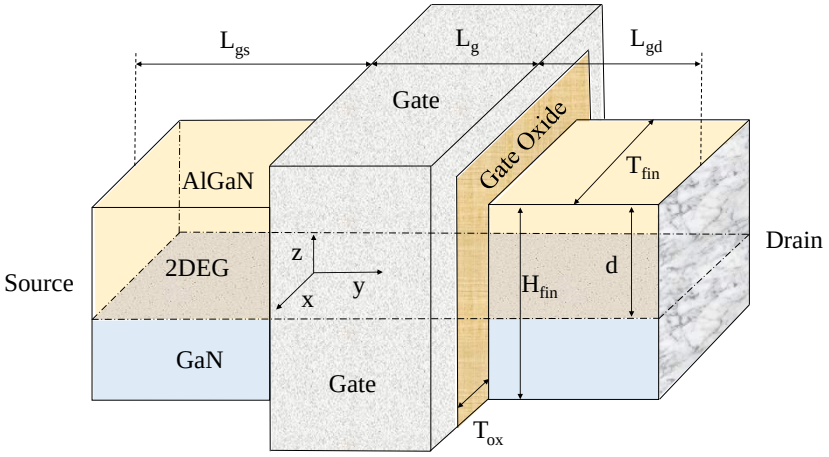

FIGURE 1.5: 3D view of a heterostructure FinFET.

1.4 FinFET Layer Structure

Based on the composition of device material, FinFETs are classified into homo and heterostructure FinFETs. In a heterostructure FinFET, fin of the device comprises of two materials having different bandgaps, such as AlGaAs/GaAs or AlGaN/GaN etc as explained in the preceding sections. On the other hand, homostructure devices are based on elemental or compound semiconductor materials, such as Si, GaAs or GaN etc. Based on the type of the device, FinFETs can be realized by employing various layers as explained below.

1.4.1 Substrate

Substrate is an important part of a FinFET often referred to as the base of device, upon which the entire structure is built on, as shown in Fig. 1.1. Selection of substrate depends upon the device layer structure. For the devices in which fin is defined by the Si material, substrates of two types are normally used i.e., Si and SOI. Amongst these, Si is the most commonly used material which offer acceptable thermal conductivity [27], while SOI substrate incorporates an insulating layer between the main substrate and the channel to reduce the effect of carrier trapping but on the expense of fabrication complexity [28].

1.4.2 Oxide Layer

In FinFET fabrication, oxide layer is employed for various purposes, such as, gate oxide as shown in Fig. 1.3 (a) & (b), capping oxide as illustrated in Fig. 1.1. Changes in gate oxide thickness (T_{ox}) may effect the threshold voltage (V_{th}) and DC performance of the device. In addition, reducing the thickness of oxide may increase the gate leakage current, whereas increasing it beyond a certain limit, reduces gate control upon the channel [29]. Capping oxide is normally employed to maintain device performance under varying ambient conditions. The thickness of capping oxide layers depends upon the drain, source and gate metal geometry

[30]. The prime purpose of this layer is that, these terminals along with the exposed semiconductor material should be covered appropriately to make them immune so that they should be less sensitive to varying ambient conditions [31].

1.4.3 Nucleation Layer

Nucleation layer is grown on the substrate by using an epitaxial growth technique such as molecular beam epitaxy (MBE) [21]. The purpose of this layer is to reduce the stress and lattice mismatch between substrate epitaxial layers which will be grown subsequently [21]. Nucleation layers are usually defined by the super lattices and they are normally of the same material as that of channel. Any lattice defects which are there in the substrate are blocked by these epitaxially grown layers [31].

1.4.4 Carrier Layer

In heterostructure devices, channel essentially comprises of two layers commonly known as carrier and barrier layer. The interface of these two layers accommodates free carriers which define 2DEG. The combination of these two layers makes the device heterostructure, because of the bandgap mismatch between these layers [21]. The carriers for 2DEG are supplied by a relatively wide bandgap layer and such a layer can be either intrinsic or extrinsic in nature depending upon the chosen material. If the chosen layer has natural piezoelectric effect as observed in AlGaN; in such a case, carriers can be generated under the influence of piezoelectric effect. The generated carriers then naturally move towards lower bandgap layer to define 2DEG [32]. The benefit of existence of piezoelectric effect in a relatively wide bandgap layer allows the formation of 2DEG without the insertion of carrier layer (doped layer) and hence, enhances the mobility of 2DEG electrons in the absence of ionized ion scattering [33]. In general, materials of both of these layers are chosen to facilitate the formation of 2DEG at the interface, by keeping the bandgap of carrier layer relatively lower than that of barrier layer [34].

1.4.5 Barrier Layer

Barrier layer is formed on top of the carrier layer for the formation of 2DEG as shown in Fig. 1.5. This figure shows the minimum requirements to form a heterostructure FinFET. In order to improve the device performance further, sometimes the barrier layer is also covered with another layer of a compatible material, to minimize oxide formation, specially if the barrier layer contains highly reactive elements such as Al. Special attention is required to design the thickness of barrier layer to avoid parasitic FET formation. Devices which are principally meant to give 2DEG dependent characteristics, require a fully depleted barrier layer at gate-to-source voltages, $V_{gs} = 0$ V. If there is a finite un-depleted thickness of the barrier layer available at $V_{gs} = 0$ V, the device characteristics will be governed by the two layers; a) barrier layer and b) 2DEG layer, which is an undesirable feature in heterostructure FinFETs [21]. Hence, it is a fundamental requirement that the thickness of the barrier layer should be such that at $V_{gs} = 0$ V, it is fully depleted. As a result, the drain-source conduction, under the applied drain bias, will be governed by the 2DEG characteristics of the device [35].

1.4.6 Contact Layer

There are three types of contacts in a FinFET. Two of them are ohmic known as drain and source contacts, and the third one is the gate contact known as Schottky contact, which could be either with or without gate oxide [21]. If the gate contact is without gate oxide, then the device operation would be fundamentally described by the MESFET operation and if the gate metal is placed on top of an oxide layer then the device operation is identical to that of MOSFET. Contact layers are normally grown on top of barrier layer, in order to reduce the contact resistance of the device. Generally, contact resistance is defined as ohmic resistance caused by the ohmic metal plus the resistance offered by the bulk region of the device between gate-drain/gate-source. Presence of heavily doped contact layer on top of barrier layer, but underneath the ohmic metal, will minimize the ohmic

contact resistance and hence, the maximum portion of the applied potential shall appear under the gate region, which controls device characteristics. Therefore, the resistance offered by gate-drain/gate-source region is referred to as parasitic resistances and the presence of the contact layer will minimize these [21, 32].

1.5 Advantages of FinFET

The invention of FinFETs has caused a tremendous impact on semiconductor industry and is still evolving with new research. Despite of the manufacturing complexities, the FinFET has made its way into the industry and prospered with promising superiority over its counterparts. The FinFET proved its suitability for IC fabrication due to high scalability and provided a new pathway for Moore's law beyond 20 nm as they have much better performance with reduced power consumption compared to planar transistors. A 16 nm / 14 nm FinFET device can potentially offer a 40 – 50 % increased performance compared to a 28 nm planar device [31]. Furthermore, fins are vertical in nature, allowing better gate control which leads to high fabrication density. Additionally, due to their unique structure, FinFETs have low leakage current, can operate at lower voltage and offer a higher battery life for mobile systems [31, 36]. Following paragraphs discuss some of the major factors which are offered by FinFET technology and therefore preferred by the industry.

1.5.1 Reduction in Gate Induced Drain Leakage

It is an established fact that, the FinFET is a three terminal device and in such a device, the highest potential is observed between the gate and drain terminals. The carriers in this region become hot and have sufficient energy to climb over the barrier, referred to as thermionic emission [37]. These hot carriers are prime contributors to a current called as gate induced drain leakage (GIDL) current. The presence of significant GIDL causes a rise in the temperature of chip and hence

it is a constraining factor which limits the number of devices per unit area of the chip. Researchers have been trying in the past to reduce GIDL in order to improve battery lifetime and also to increase device density on a chip. A crucial factor to reduce GIDL is, to modify the depletion underneath the gate, especially towards gate-drain region. Owing to this fact, earlier in MESFET design, the planar device geometry was modified into recessed gate FET where the gate is placed below the drain-source plane, which modified the edges of depletion and hence, it improved GIDL. A similar philosophy has been applied in FinFET, where the gate-drain depletion has been modified by having a trigate geometry. This improved the performance of the device by reducing undesirable flow of current caused by the gate-drain potential and hence a reduction in GIDL is observed. The presence of oxide layer, its type and thickness will also play a role in determining the magnitude of GIDL [38]. Since GIDL depends upon the depletion geometry in the gate-drain region of the device which is dependent upon T_{fin} and H_{fin}, hence their optimized values will also play a role in reducing GIDL [37].

1.5.2 Reduction in Drain Induced Barrier Lowering

Drain induced barrier lowering (DIBL) is a negative feature observed in Schottky based FETs and it is more prominent in short channel devices. Since, the depletion under a gate is not uniformly distributed and its thickness is more towards the drain side of the device, increased number of charges in the depletion towards the drain side, cause image charges in the gate metal resulting into a reduction in the gate potential, which eventually reduces the thickness of depletion towards the drain side of the device referred to as DIBL [39]. As the carriers are hot in this region, and presence of DIBL offers a relatively lower barrier which results into an increased flow of carriers from the channel to the gate metal thus, causing an undesired flow of current. Normally, such behavior is dominating in those FETs where gate is placed directly upon the semiconductor without intervening oxide layer. Since, the shape of depletion is modified because of the trigate nature of

the FinFET, so this geometry also mitigates DIBL and hence, improves the device performance [39].

1.5.3 Reduction in Gate Parasitic Capacitances

Parasitic capacitances referred to as Miller capacitances are unavoidable and they exist between drain-gate and source-gate regions of the device and determine its high frequency characteristics. The parasitic capacitances depend upon the device dimensions, specially L_g [40]. While the L_g decreases in a conventional FET, its Miller capacitors also decrease, but at the same time it reduces its transconductance (g_m), which results into reduction in its RF performance [41]. Hence, it is always a desirable feature that, the device used in the system should have Miller capacitors as low as possible. Mathematically, Miller capacitors and unity gain frequency (f_t) of operation are related as

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1.1}$$

where, C_{gs} is gate-to-source and C_{gd} is gate-to-drain Miller capacitors. Nanoscale FinFETs meant for millimeter waves applications, because of their specific geometry, offers exceptionally low value of C_{gs} and C_{gd} along with relatively high value of g_m because of 3D operation of the gate. Thus, FinFETs are highly suitable for high frequency applications. The value of capacitances can be tailored according to the need of an application by optimizing the geometry of fin i.e., T_{fin}, H_{fin}, L_g, and L_{fin}. In short, the negative effects of parasitic capacitance can be overcommed in a more effective manner in FinFET applications which makes them more suitable for high frequency.

1.5.4 Improvement in Sub-threshold Characteristics

Threshold voltage (V_{th}) is the minimum gate-to-source voltage that is required to make a conducting path between the source and drain, if it is not already there.

On the other hand, for depletion type FinFET, where the channel is physically available, V_{th} is a voltage which will deplete the channel completely and ideally at this applied voltage there should be zero drain current flowing between drain and source. The magnitude of V_{th} plays an important role in determining the sensitivity of the device and it will also determine the battery life of a system in which FinFET is used as an active device [42]. In an ideal device, $V_{gs} = V_{th}$ should define $I_{ds} = 0$, but practically speaking, at such condition in conventional FET, I_{ds} has got a non-zero value. To improve this, FinFET technology was introduced, wherein the channel is controlled from 3 different directions, bringing the sub-threshold characteristics closer to their ideal values. This technology also improved the off-state conduction of the device, hence allowing a better device thermal management which eventually led to very large scale device integration [43, 44].

1.6 FinFET Characteristics

FinFETs operate like conventional MOSFET devices i.e., they can have both depletion and enhancement mode of operations. Furthermore, depending upon the dominant carriers, they are classified into either $p-$channel or $n-$channel devices. Typical DC characteristics of a FinFET are shown in Fig. 1.6 (a), wherein it can be observed that by increasing V_{ds}, I_{ds} also increases in a linear fashion for small values of V_{ds} and then it saturates to a constant value known as $I_{ds(sat)}$. On the other hand, voltages applied on the gate terminal i.e., V_{gs}, controls the amount of current flowing through the channel by changing the depletion height. Moreover, transfer characteristics $g_m(V_{gs})$ also play an important role in determining the quality of the device as shown in Fig. 1.6 (b). A high value of g_m will indicate a good gate response and such devices will offer a good gain to an incoming signal. It can be seen from Fig. 1.6 (b) that, g_m is also dependent upon V_{ds} and usually the g_m of a device is reported after the onset of current saturation i.e., $V_{ds} \geq V_{ds(sat)}$. The device output conductance, g_d is also used to determine the quality of a finished FinFET. Fig. 1.6 (c) shows a typical g_d response of a FinFET which is

dependent both on V_{gs} and V_{ds}. The data of plot indicate that, the device offer high g_d at relatively lower applied bias and it tends to saturate where current of the device exhibits saturation, and hence it offers lowest value of g_d. A contrast of leakage current for conventional FET and FinFET is given in Fig. 1.7. As depicted, both planar and FinFET offer the same leakage current at higher V_{gs} value, but as V_{gs} decreases, FinFET exhibit considerably lower gate leakages. This phenomenon could be associated with the trigate structure of the device, where the channel is controlled from multiple sides by the gate potential applied on it [45]. Capacitors, C_{gs} and C_{gd} play an important role in device AC performance. Due to the trigate geometry, both C_{gs} and C_{gd} of FinFETs are relatively lower compared to conventional FETs thus, they offer high operating frequency as evident by Eq. 1.1. This is also shown in Fig. 1.8 (a), wherein the maximum achievable frequency, f_{max} as a function of L_g for both conventional FETs and FinFETs are shown. By examining the figure, it can be seen that as L_g reduces, f_{max} increases. However, FinFETs offer higher f_{max} across all L_g values compared to conventional FET.

Other AC performance parameters are transconductance-frequency product (TFP) and gain transconductance frequency product (GTFP). TFP represents the trade off between power and bandwidth in high speed device design, while GTFP gives overall performance criterion of a new device. These parameters provide an excellent estimation of a device capability with respect to AC performance. By examining the TFP and GTFP for conventional FETs and FinFETs plotted in Figs. 1.8 (b) & (c), respectively, one can observe that for the given range of L_g, FinFETs performance is better compared to conventional FETs. Hence, making it a superior device in the FETs family.

1.7 DC Model

In conventional FETs, the potential distribution inside the channel can be estimated by solving a 2D Poisson equation given as [47]

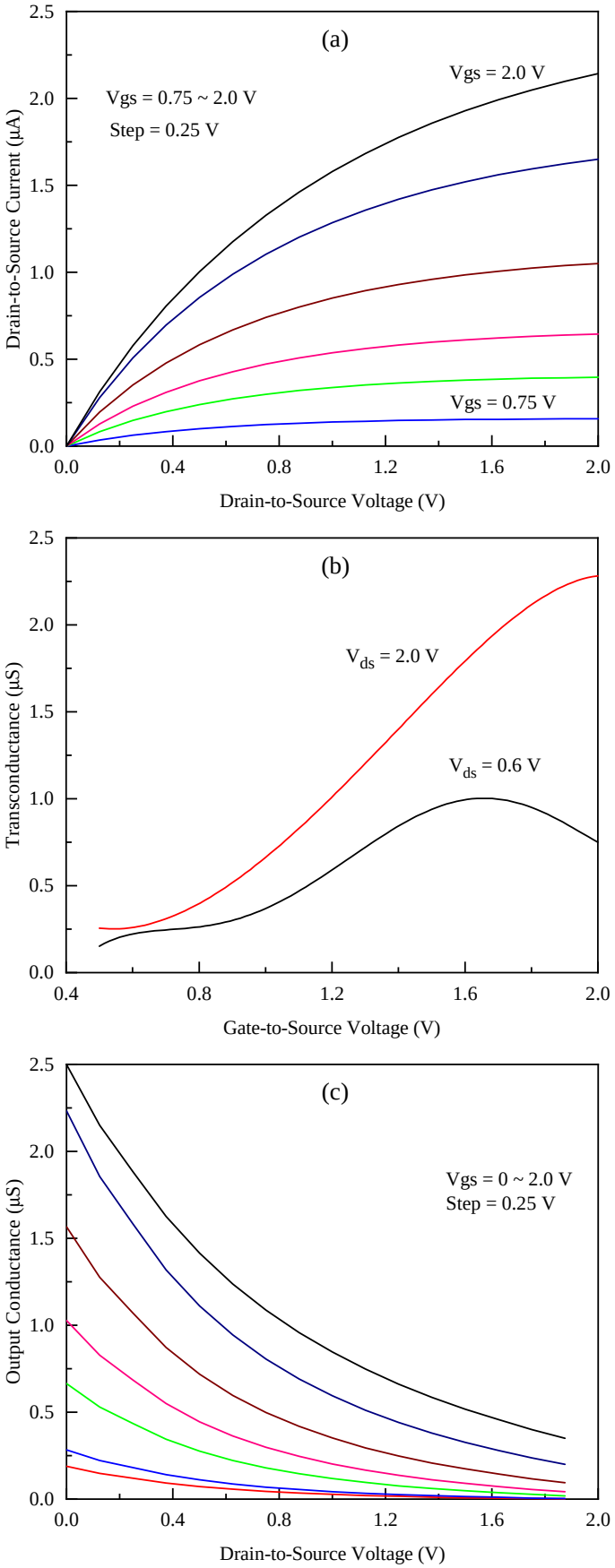

FIGURE 1.6: Typical (a) output characteristics (b) transfer characteristics (c) output conductance of a FinFET.

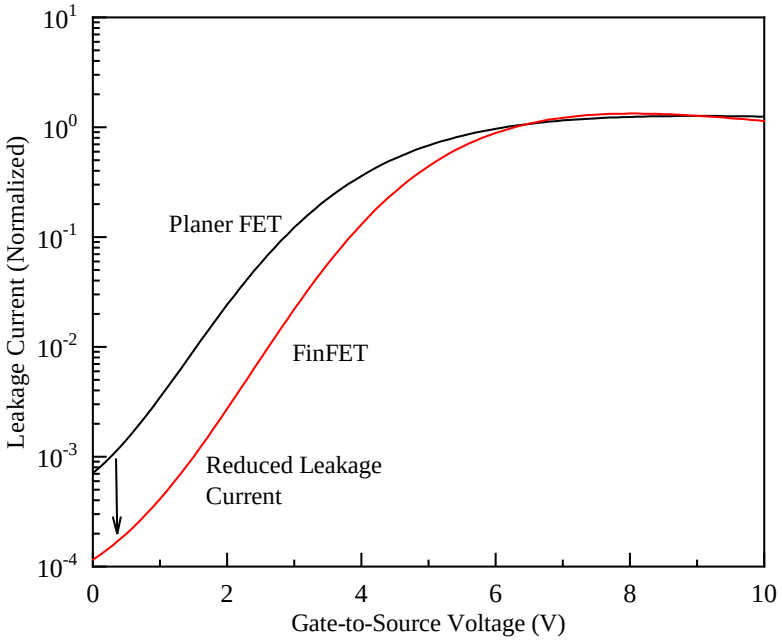

FIGURE 1.7: Leakage current comparison for conventional FET and FinFET.

$$\frac{\partial^2\psi(x,y)}{\partial x^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi(x,y) + \phi_B - V_{ch}(y)}{V_T}\right) + \frac{qN_d}{\epsilon_{si}}. \tag{1.2}$$

The parameters used in Eq. 1.2 have usual meaning as defined in the list of variables. The same approach can be applied to evaluate field distribution inside a FinFET however, to accommodate 3D geometry, a 3D Poisson equation will be employed:

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2} + \frac{\partial^2\psi(x,y,z)}{\partial y^2} + \frac{\partial^2\psi(x,y,z)}{\partial z^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi(x,y,z) + \phi_B - V_{ch}(y)}{V_T}\right) + \frac{qN_d}{\epsilon_{si}}. \tag{1.3}$$

By solving Eq. 1.3 under appropriate boundary conditions, charges available in the channel (Q_{inv}) of the device will be calculated. By involving the mobility, μ, I_{ds} can then be evaluated by using expression of the form:

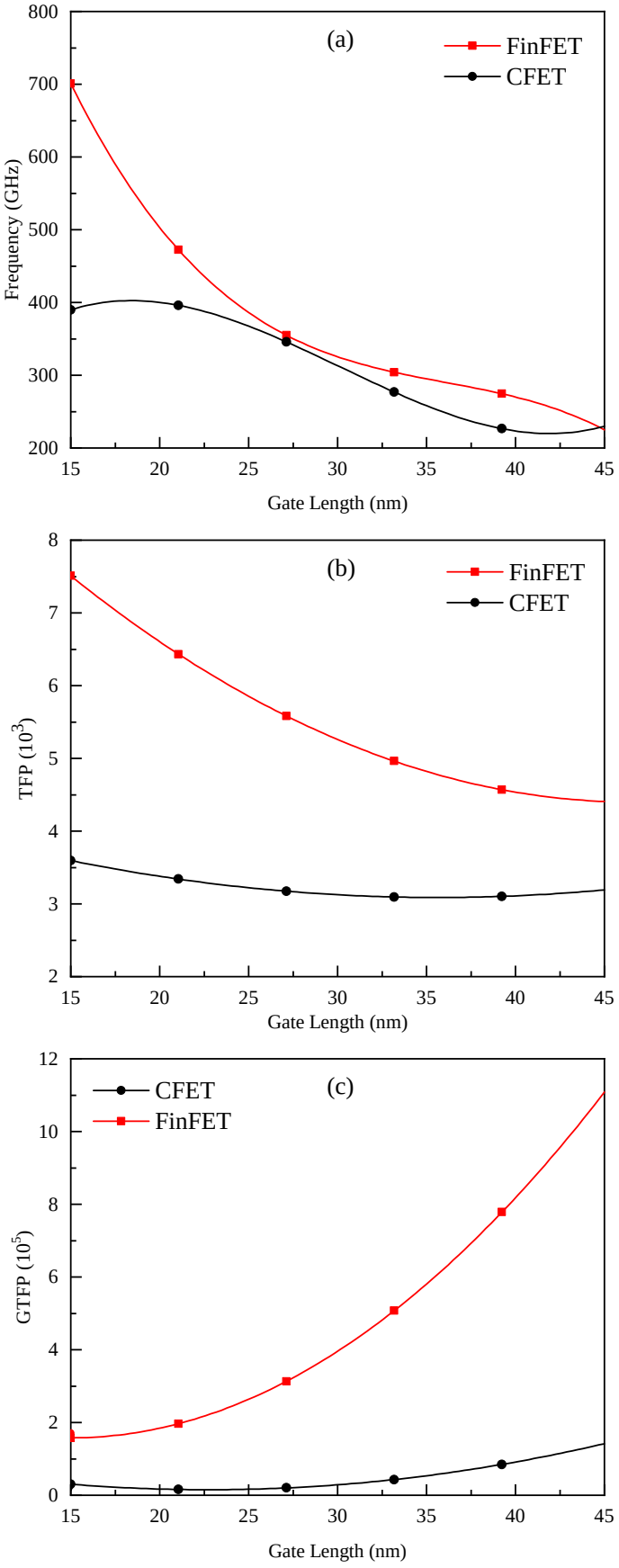

FIGURE 1.8: Comparison of (a) frequency (b) Transconductance-frequency product (TFP) (c) Gain transconductance frequency product (GTFP) with L_g of conventional FET (CFET) and FinFET devices [46].

$$I_{ds} = \mu(2H_{fin} + T_{fin})Q_{inv}\frac{dV(y)}{dy} \tag{1.4}$$

1.8 Quantum Mechanical Effects

FinFETs have the ability to control channel current while minimizing SCEs by using multi dimensional 3D gates. This 3D gate geometry provides efficient electrostatic control over the channel by increasing the effective channel width and paves the way for further transistor size reduction. However, upon reducing the L_{fin} to a few nanometers, the T_{ox} also has to be decreased [48]. The decrease in dielectric thickness with the L_{fin}, increases the impact of tunneling significantly. This phenomenon occurs when carriers tunnel through the device's gate dielectric, which ideally should act as a perfect barrier. Although the electron energy is less than the gate dielectric barrier energy, but still, there is a finite probability of carriers transmission, referred to as quantum mechanical effects. Furthermore, the concern becomes more critical when the penetrating particles start behaving like a wave. So, the presence of quantum mechanical effects in nano-FinFETs become unavoidable to comprehend electron transport and to optimize the device size.

A conventional device structure requires classical equations to evaluate electron distribution inside the channel, whereas, in nano-structures electrons behave as a wave classified by a quantum phenomenon, thus, the current caused by such quantum particles shall be governed by a quantum transport model. To move carriers from source to drain and to account for quantum effects, under special circumstances, a hybrid technique involving classical and quantum effects may be employed simultaneously [49]. Quantum mechanical transport models can be obtained by solving the Schrödinger wave equation in three dimensions to establish the contribution of quantum particles responsible to determine the characteristics of the device. On the other hand, in hybrid technique, both Poisson and Schrödinger equations can be engaged simultaneously to evaluate the device characteristics. The main purpose of engaging 3D Poisson equation would be to

determine the charge distribution in the channel. With this approach, nano-scale FinFET DC characteristics can be modeled accurately compared to a conventional approach wherein, the Poisson equation coupled with a mobility model is engaged, to determine the device characteristics [21].

1.9 Research Motivation

The era in which we are living can truly be called as advanced era, where our lives are totally dependent upon technology and mostly on smart devices, such as cell-phones, laptops and other similar gadgets. These technological advancements have made our lives a lot easier while there is always a desire of reducing the physical size of mobile devices without compromising on their performance. Technological advancements have caused further reduction in the size of semiconductor device which is a basic building block of a smart device. A phenomenal growth in semi-conductor industry was observed even after five decades from the development of first FET. As the time passed, and the research advanced in various technological fields, the demand of these devices increased sharply as predicted by Moore's law [15]. With the advent of advance processing techniques even with the reduction of their physical size, the performance of these devices increased exponentially. This made the appliances and gadgets used in our daily life smaller, easier and more feature oriented.

Research has also been carried out to add new materials for the fabrication of FETs to make appliances better with increased fabrication density. In an effort to further enhance the performance of FET based systems where the downscaling was halted at 100 nm due to increased SCEs, multi gate FinFETs are introduced. Multi-gate technology is a relatively newer one but highly promising because it offers improved device performance at nano-scale level. Thus, researchers are concentrating to develop nano-scale FinFETs both on Si and compound semiconductor such as GaAs, AlGaN/GaN etc, to cater industrial needs.

Recently, AlGaN/GaN FinFETs are developed which operate both in depletion as well as in inversion mode of operation. For such 3D structure of FinFETs, there is a need to develop analytical models which can predict the characteristics of FinFETs for their entire range of operations i.e., depletion as well as enhancement mode. The previously reported models, which will be discussed in the next chapter, are meant only for FinFET depletion mode of operation and hence they are silent and unable to predict the device performance in enhancement mode simultaneously. Hence, any such effort, wherein, the FinFET characteristics would be predicted mathematically in a comprehensive manner incorporating both depletion and enhancement mode, shall be an extension in FinFET device understanding and to the best of our knowledge, such a study is not reported in the literature.

FinFETs having gate length below 10 nm exhibit quantum mechanical effects and their characteristics cannot be determined using conventional FET modeling approaches. For such devices, it is imperative to incorporate quantum effects wherein the particles are described by a wave function and the energy of such wave function is described by a quantum expression usually achieved by solving Schrödinger wave equation. Coupling the physical dimensions of the device with quantum mechanical effects is a challenging task and this research work is aimed to develop such a technique which will predict the device response and hence, offer a better device understanding at nano-scale level. Such a model can be employed as a tool in device design and simulation softwares to predict the device response even before its fabrication.

Artificial intelligence (AI) is considered an effective tool and is being employed widely in various fields to have a better and efficient technological solutions. Since, nano-scale FinFET involves a high-tech semiconductor industry, to overcome the product developmental cost, it would be wise to have an AI based technique capable to predict the device characteristics to a good degree of accuracy by involving device physical parameters, which are normally engaged by a design engineer to optimize the device performance. To develop such a system, a dataset involving device physical parameters and corresponding characteristics shall be a core requirement. An exhaustive search for such a database was carried out and it was

noted that there is no such data available or reported in the literature. It is proposed that to develop an AI based system by involving an established tool known as COMSOL Multiphysics, a data bank of FinFET characteristics shall be developed. Based on the developed data bank, a deep neural network (DNN) should be proposed to predict the device characteristics involving the device physical dimensions. The proposed technique could be compatible to the relevant industry to predict nano-scale FinFET characteristics prior to their fabrication and hence its engagement could potentially reduce the product cost.

1.10 Thesis Outline

Chapter 1 presented fundamental concepts pertaining to FinFETs fabrication, characterization and their technological importance. It has been discussed that the FinFET would be the device of future and it will play an important role in miniaturized systems specially in mobile technology. It is discussed that nano-scale FinFETs are preferred because they have the ability to mitigate SCEs usually observed in FET devices when the channel length is reduced below 100 nm. It is discussed that, a FinFET performs relatively better than its competitors because of its 3D geometry. The dependence of device characteristics on its various layers is also discussed in this chapter. Different materials, and their associated characteristics, which could be involved in FinFET fabrication are also discussed. The chapter also presents a brief related to FinFET structure when fabricated using 2DEG materials. It has also been described that an accurate device DC model could only be realized if quantum mechanical effects presence in such devices are taken into considerations.

Chapter 2 focuses on previously reported studies related to FinFETs and its technological parameters such as device layer structure, device design and fabrication. A detailed overview of conventional modeling techniques, quantum transport models and applicability of such techniques to a 3D homostructure is presented.

Moreover, quantum transport and involvement of AI to predict device characteristics have also been discussed in this chapter. A comparative analysis of various models is presented and based on the reported data research gaps for future study are developed.

Chapter 3 presents a comprehensive $I - V$ model for the evaluation of above threshold DC characteristics of trigate heterostructure FinFETs, for both depletion and inversion mode of operations. According to our conservative estimate, no such model is reported in the literature combining both depletion and inversion mode of operations simultaneously. Current associated with 2DEG referred to as depletion current has been evaluated by solving a 2D Poisson equation with appropriate boundary conditions. On the other hand, the inversion current is assessed by involving a 3D Poisson equation and the developed $I - V$ model incorporates both the solutions to define a comprehensive expression for the generation of DC characteristics of FinFETs as a function of applied bias. It has been shown that the developed model offers a reasonable accuracy when the modelled characteristics are compared with experimental data.

Chapter 4 presents a Schrödinger-Poisson based technique to predict the behavior of trigate FinFETs. The Schrödinger equation is solved for 3D device structure by incorporating quantum-mechanical ballistic transport. A 3D Poisson equation and non-equilibrium green function are used to evaluate charge distribution which is eventually coupled with Schrödinger equation to assess drain current of FinFETs. The contact resistance and its impact on drain current is also assessed using Fermi-Dirac distribution function. It is demonstrated that the drain current, as a function of drain bias, saturates because of the finite supply of carriers from the source electrode. The model is calibrated using TCAD and its accuracy is established using experimental data.

Chapter 5 presents a technique which predicts DC characteristics of FinFETs prior to their fabrication. The developed technique uses a deep learning AI approach, wherein for the training of the system, a dataset of DC characteristics

is initially developed using COMSOL Multiphysics software, which generates device characteristics by involving its physical parameters including gate length, fin length, fin height, fin thickness and doping concentration. The trained AI network has the ability to generate FinFET characteristics of any dimension prior to its fabrication. It is demonstrated using the control data, that the proposed deep learning approach has the ability to predict device response in seconds as opposed to hours required by standard simulators. Thus, the developed approach could be a beneficial tool for industry to make industrial process efficient both from time as well as cost point of views.

Chapter 6 discusses the outcomes achieved from this research and proposes possible extension which can be carried out as a future work.

Chapter 2

Literature Review

Since the advent of semiconductor devices, there has been always a struggle to improve the device performance, and to do so, a number of device architectural advancements have been proposed such as JFET, MOSFET, MESFET etc. The scalability of these FETs proved to be a cumbersome task for design engineers and as the L_g shrinks beyond 50 nm, it begins to lose its control upon the channel and undesired issues are observed. To overcome the challenges in nano-scale technology, FinFETs were introduced in 1989 by Hisamoto *et al.* [3]. A device, named as depleted lean channel transistor (DELTA) at that time, was developed, which was composed of a vertical fin enveloped by two gate electrodes. A substantially reduced leakage current was observed and a reduction in short channel effects was also noticed in the proposed device design [50], thus improving the controllability of gate upon the channel [51, 52].

The commercialization of FinFETs started in the first decade of the 20^{th} century with the invention of Omega FinFETs by Taiwan Semiconductor Manufacturing Company (TSMC) [53]. Later on, the FinFET evolution was followed by the development of 90 nm Bulk FinFETs by Samsung which was used in RAMs [54]. Commercialization of FinFETs on full scale started with the development of Intel's 22 nm [55] device which was used in the fabrication of 500 million ICs in first 3 years [18]. A number of other well established industries also started the production of FinFETs based memory chips, multi-level cell, SRAM, DRAM etc.

FinFETs are expected to continue playing their role in the coming years. It is assumed that FinFET structure having the channel wrapped from three sides may reach to its limits beyond 5 nm. To overcome the issues, gate-all-around FET (GAAFET) may be the leading contender for next generation applications. It is understood that GAAFET can bring better scalability, faster switching time, lower leakage and high chip density. Moreover, vertically aligned nanowires and nanosheets are some other options to be explored for next generation devices [56].

2.1 FinFET Technology-An Overview

With the acceptance of FinFET idea in 1989, numerous researchers have proposed different FinFET structures to enhance electrical performance of the device. In 2000, Chang *et al.* [57] studied the relationship between L_g and V_{th} in a DG MOSFET. They concluded that a single gate device has higher V_{th}, thus, L_g scaling becomes a challenging task. Whereas, a DG device can be employed to get better control upon V_{th}, allowing further scalability of the device. To address V_{th} related issues, Choi *et al.* [58] developed a 20 nm DG FinFET, which helped further to mitigate the device scaling issues. In DG FinFETs a higher drive current of 365 μA/μm compared to 270 μA/μm in a typical MOSFET, was observed along with reduction in OFF state leakage current. Kim *et al.* [59] reported that by using trigate FinFETs, SCEs were reduced.

Sharma *et al.* [46] studied the effects of H_{fin}, T_{fin}, L_{fin} and L_g on RF performance of FinFETs. They observed that by decreasing L_g, an increase in gain and f_{max} is achieved. Furthermore, they observed that FinFETs have the potential to operate at relatively higher frequency compared to conventional FETs. Meshra *et al.* [60] developed 22 nm trigate FinFETs and studied the effects of H_{fin} and number of fins on the device characteristics. They concluded that, in order to improve the drive current, it is better to increase H_{fin} rather to increase the number of fins.

Gu *et al.* [61], analyzed 6-T and 4-T FinFETs based Static Random Access Memory (SRAM) cells and observed a 30 % less Static Noise Margin (SNM) in

6-T designs compared to MOSFET SRAM cell. Ensan *et al.* [62] also developed SRAMs using 21 nm FinFET technology and demonstrated that, SRAMs developed using FinFETs occupy less chip area and also consume less battery power. Mutterja *et al.* [63] developed logic gates using independent DG FinFET technology. They concluded that, an increased device density per unit area can be achieved using FinFETs compared to other established FET technologies.

Nirmal *et al.* [64] did a research on heterojunction FinFETs and observed a substantial reduction in SCEs. Liu *et al.* [65] studied self-heating effects in FinFETs and observed a reduction in channel current due to increased resistance observed at higher temperature possibly caused by the increased amplitude of lattice phonon.

Alvardo *et al.* [66] developed a low noise amplifier using FinFET technology. They extracted the device's intrinsic and extrinsic parameters and studied FinFETs potential as a microwave device. Gaillardon *et al.* [67] studied noise power in FETs and found that FinFETs offer relatively low noise power compared to conventional FETs. Thus, FinFETs based circuitry can potentially increase the battery life up to 25%.

Ledderer *et al.* [68] studied AC performance of 15 nm trigate FinFETs by extracting S-parameters upto 110 GHz. The effects of number of fins on intrinsic device parameters were studied and they concluded that by increasing the number of fins, f_{max} of a FinFET increases. Crupi *et al.* [69] showed that a FinFET has the capability of operating above 110 GHz. They also studied the effects of bias and number of fins on f_{max}. Kundu *et al.* [70], observed S-parameters of 65 nm FinFETs up to 50 GHz. They observed that f_{max} of the device is higher compared to conventional FETs because of the reduction in Miller capacitors and increase in the device g_m. Sakhi *et al.* [71] investigated the FinFETs behavior in subthreshold region. The effects of FinFETs dimensions were also studied on its operations.

Qin *et al.* [72] developed a model to simulate AC performance of FinFETs upto 300 GHz. They studied the effects of fin dimensions on the device AC characteristics. They also showed that L_g has a direct relationship with frequency, while

TABLE 2.1: A brief history of FinFET technology.

Author	Ref.	Year	Description
Chang *et al.*	[57]	2000	Effect of L_g on V_{th}.
Choi *et al.*	[58]	2001	20 nm DG FinFETs.
Kim *et al.*	[59]	2004	Improved SCEs in 30 nm DG FinFETs.
Lederer *et al.*	[68]	2005	S-parameters upto 110 GHz for $L_g = 50$ nm.
Guo *et al.*	[61]	2005	SRAM design using FinFETs.
Crupi *et al.*	[69]	2006	Effects of number of fins on f_{max}.
Muttreja *et al.*	[63]	2007	Logic gates using independent DG FinFETs.
Kundu *et al.*	[70]	2010	S-parameters upto 50 GHz for $L_g = 65$ nm.
Sharma *et al.*	[46]	2012	Effects of FinFET dimensions.
Mishra *et al.*	[60]	2013	H_{fin} and its importance in FinFETs.
Nirmal *et al.*	[64]	2013	Reduced SCEs using dielectric material.
Alvarado *et al.*	[66]	2013	Low noise amplifier using FinFET.
Liu *et al.*	[65]	2014	Self-heating effects in FinFETs.
Gaillardon *et al.*	[67]	2016	Noise power in FinFETs.
Sakhi *et al.*	[71]	2017	Sub-threshold study of FinFETs.
Qin *et al.*	[72]	2018	Effect of L_g on S-parameters.
Ensan *et al.*	[62]	2019	SRAM cell using FinFETs.

there is an inverse relationship between frequency and T_{fin}. Furthermore, they observed that R_{ds} and R_{gd} decrease by increasing T_{fin}, while L_g has almost no effect on their values. A summary of FinFET technological advancements observed so far is presented in Table 2.1.

2.2 Evolution in Heterostructure FinFETs

By using two dissimilar semiconductors such as AlGaN/GaN one can have a structure known as heterostructure. Such a heterostructure generates 2DEG at its interface and can be used as channel of the device. In 2000, Ambacher *et al.* [73] determined 2DEG sheet carrier concentration, induced by polarization charges using a solution of Schrödinger and Poisson equations under appropriate boundary conditions in heterostructure devices. The study also included the dependence of 2DEG formation on piezoelectric and polarization induced effects.

Knowing the superior electrical qualities of 2DEG heterostructure, in 2002, Mishra *et al.* [74] studied market trends of different semiconductor devices, materials and their applications and predicted that heterostructure devices including FinFETs will dominate the market with attractive superiority in high power radar and wireless communication systems.

In 2013, Takashima *et al.* [75] investigated the effects of sidewall contribution on the device channel by fabricating AlGaN/GaN FinFETs. An improvement in SCEs was observed in the fabricated devices. Furthermore, they also investigated V_{th} dependence upon the T_{fin} and concluded that narrower channel is dominated by the side-gates of the device. Also, superior channel characteristics, such as reduced channel resistance and high g_m, are observed in FinFETs when compared with conventional FETs.

In 2014, Im *et al.* [76] fabricated AlGaN/GaN FinFETs. They studied 2DEG and sidewalls contribution in the channel current and observed excellent on-state performance in the developed devices. In 2015, Jo *et al.* [23] fabricated steeped

wall AlGaN/GaN FinFETs and reported extremely broad g_m, along with high on-state performance.

In 2015, Son *et al.* [24] fabricated multiple AlGaN/GaN FinFETs with various W_{fin} values and observed its effects on g_m, on-state and off-state performances of the device. Im *et al.* [77], in 2016, also fabricated multiple AlGaN/GaN FinFETs having different W_{fin} values and investigated temperature dependent DC performance. They investigated contribution of sidewall channels in the overall characteristics of wide and narrow FinFETs. Furthermore, a brief observation has also been carried out to assess g_m dependence on 2DEG and sidewall of the device.

In 2016, Ren *et al.* [78] studied heterostructure FinFETs and verified their results with TCAD simulations. The relationship between V_{th} and W_{fin} has been established using Poisson equation. The model also includes the influence of T_{ox} and dielectric permitivity of FinFETs.

Ghattak *et al.* [79] studied a V_{th} model for heterostructure FinFETs and compared the results with the experimental data. They proposed that in order to transform a normally-ON device into a normally-OFF device, W_{fin} can be scaled accordingly.

In 2017, Zhang *et al.* [80] fabricated heterostructure FinFETs featuring T-shaped gates and achieved linear g_m characteristics. They observed 1.45 times higher current density and 1.66 times higher power density at 8 GHz when compared to traditional HEMTs. In the following year, Zhang *et al.* [81] examined fin configurations in heterostructure FinFETs both theoretically and experimentally. A physics based model has been built for qualitative analysis whereas, the devices were fabricated for experimental verification. They studied g_m response in detail and established that L_{fin} has to be reduced for improved cutoff frequency. They also observed that g_m of a device depends upon H_{fin} and for improved performance an optimized value of H_{fin} is of prime importance.

In 2018, Xu *et al.* [32] simulated 2DEG characteristics in TCAD and proposed different optimized parameters for improved performance of heterostructure FinFETs. Their proposed solution suggested that the selection of appropriate device

TABLE 2.2: A brief overview of AlGaN/GaN based heterostructure FinFETs.

Author	Ref.	Description
Ambacher (2000)	[73]	2DEG carrier concentration evaluaiton.
Mishra (2002)	[74]	Market trends of heterostructure devices.
Takashima (2013)	[75]	Sidewall contribution in AlGaN/GaN FinFETs.
Im (2014)	[76]	DC performance of AlGaN/GaN FinFETs.
Jo (2015)	[23]	To improve flatness in g_m of AlGaN/GaN FinFETs.
Son (2015)	[24]	Effects of W_{fin} on AlGaN/GaN FinFETs.
Im (2016)	[77]	Temperature effects on AlGaN/GaN FinFETs.
Ren (2016)	[78]	Physics based V_{th} model of AlGaN/GaN FinFETs.
Ghattak (2017)	[79]	V_{th} model for power AlGaN/GaN FinFETs.
Zhang (2017)	[80]	DC and RF performance of AlGaN/GaN FinFETs.
Zhang (2018)	[81]	Power performance of AlGaN/GaN FinFETs.
Xu (2018)	[32]	TCAD simulations of AlGaN/GaN FinFETs.
Ahmed (2020)	[82]	Analytical model of AlGaN/GaN FinFETs.
Huang (2020)	[83]	AlGaN/GaN FinFET for power applications.

parameters ensures simultaneous activation of 2DEG and sidewall MOS channel formation, at positive V_{th} which is a requirement for normally-OFF operation.

Ahmed *et al.* [82] presented an analytical model for rectangular channel heterostructure FinFETs with three-sided Schottky barrier gate, by utilizing a 3D Poisson equation. In this study, the influence of trigate geometry on charge sheet carrier concentration has been assessed and authors reported that heterostructure FinFETs deplete more rapidly than ordinary HEMTs, owing to the additional field generated by the side gates. In 2020, Huang *et al.* [83] fabricated trigate HEMTs

and observed improved on-off current, sub-threshold swing, and breakdown voltage compared to planar HEMTs. Because of these superior characteristics they carry higher potential to be used in next generation high power circuitries.

In a nutshell, it can be concluded that heterostructure FinFETs offer superior electrical performance and they are normally fabricated by using two distinct wide bandgap materials such as AlGaN/GaN. Based on the fin geometry, these devices can normally be ON or OFF as per the need of an application. The gate of heterostructure FinFETs can be placed directly on the semiconductor, alternatively they can be fabricated by using an intervening oxide layer. The characteristics of heterostructure FinFETs are primarily determined by the 2DEG, however, in some cases, it is observed that there is a formation of side channels which also contribute towards the performance of these devices. Those heterostructure FinFETs where side channels are also observed, they can accommodate a bigger gate swing of an incoming signal. Apart from the 2DEG, the performance of FinFETs as discussed above, is heavily dependent upon L_g, L_{fin}, H_{fin} and T_{fin}. It is established that these variables should be scaled appropriately for optimum performance of the device. An overview of AlGaN/GaN heterostructure FinFETs is presented in Table-2.2.

2.3 Carrier Transport Mechanism in FinFETs

Carriers transport in a semiconductor device has been the subject of significant interest over the last few decades. However, continuous downscaling of transistors has made this subject a more challenging job to handle. At nanoscale, it is neither conceptually nor mathematically a simple phenomenon. However, it is still fundamentally important to understand carriers transport mechanism in a nanoscale FinFET in order to describe its operation. It is an established fact that the response of a FinFET is primarily defined by the transportation of its carriers from source to drain which is controlled by the gate terminal of the device. This transportation is dependent upon various possible mechanisms such as:

(a) drift of charge carriers under applied bias;

(b) diffusion of carriers because of the density gradient;

(c) thermionic emission of the carriers because of the channel temperature and

(d) carriers tunneling under quantum effects.

If the dimension of a FinFET is such that it could be called as a long channel device, then the electrical response of the device would be controlled by the drifting carriers and the channel current will then be dependent upon the mobility offered by these carriers and its associated drift velocity, v_d. It is a known fact that, if we keep on increasing V_{ds}, the velocity saturates at a certain higher applied potential, which is a material dependent property. Therefore, based on FET channel material, the v_{sat} will have a limiting value and beyond that it would be independent from the applied bias. This leads to current saturation as a function of applied V_{ds} which is routinely observed in high frequency FETs [46]. Contrary to this, FinFET is a quantum device where apart from the drift current, special transportation phenomena are also taking place such as velocity overshoot and carriers tunneling [84, 85].

In case, the device current is predominantly associated with drifting of carriers, then a conventional approach is applied where the current is evaluated by involving carriers density and v_d. The carriers density as a function of applied bias can be evaluated by solving Poisson equation for a given device geometry. On the other hand, if L_{fin} is considerably small such that the wave function of one side (source) is overlapping with the other side (drain), for such a channel the carriers transportation falls under the definition of ballistic transport. The device electrical response can then be estimated by engaging Schrödinger wave equation wherein, the carriers of a source side are represented by a wave function which is overlapping to the drain side to allow quantum transport. The device behavior can mathematically be represented by engaging Poisson and Schrödinger equations simultaneously. Poisson equation gives the estimation of carrier density

whilst Schrödinger wave equation describes its flow as a propagating wave inside the channel.

If a FinFET channel is defined by a 2DEG, then it is an established fact that such a device is a quantum device and its response can only be estimated by taking into consideration energy wave function representing the energy of the carriers available in 2DEG [84]. So in general, a nanoscale FinFET having a channel made by a semiconductor material or a 2DEG layer, in both the cases a quantum mechanics based carriers transportation will be observed as a dominating current contributor, and the device characteristics assessment requires a solution based on Schrödinger wave equation.

Apart from the channel conduction, FinFETs may have a current flowing from channel to the gate referred to as leakage current. Such a current can either be associated with thermionic emission (long channel devices) or with channel-to-gate tunneling. Such tunneling will only be observed if the channel wave function describing the movement of the carriers has penetration into the gate electrode. In FETs, channel-gate transportation should be as low as possible and ideally it should be zero.

Short channel FinFETs usually require complex mathematical formulation to represent their electrical response as a function of applied bias. A number of studies have been conducted in last two decades, listed in Table-2.3; wherein, researchers tried to investigate carriers transport mechanism for various types of FinFETs.

In 2004, Kim *et al.* [59] analyzed FinFETs performance using classical and quantum mechanical approaches. They investigated device performance by solving 2D Schrödinger-Poisson equations for different values of T_{fin} and validated their results with experimental data. Shao *et al.* [86] presented a quantum model for trigate FinFETs structures using ballistic transport. The model comprises of non-equilibrium Green's function (NEGF) and Schrödinger wave equation to investigate quantum transport and electron density profile. Khan *et al.* [87] developed a fully self-consistent quantum transport simulator using contact block reduction approach. A brief investigation related to H_{fin} variation and its impact

on the device characteristics has been carried out by using the developed 2D & 3D simulators. Additionally, a comparative study has also been carried out on electron densities in DG and trigate FinFETs.

Natori *et al.* [88] came up with a compact transport model for nanowire FinFETs for the understanding of device operation. The research also discussed SCEs and temperature based performance of the device. They also studied quantum capacitance and quantum current and concluded that in linear region, the magnitude of current in a nanowire FinFET is primarily controlled by quantum capacitance. Dastjerdy [89] used NEGF approach to explore the features of nanowire FinFETs based on 3D quantum effects. The study concluded that Si nanowire performs better in FinFETs than a GAA channel.

Deyasi *et al.* [91] investigated the performance of GAA and nanowire FinFETs. They studied the effects of different types of gate structures on sub-threshold swing, channel length modulation, quantum capacitance and g_m, using Schrödinger-Poisson equations. In 2011, Sabry *et al.* [90] simulated FinFETs by involving quantum transport techniques and concluded that NEGF enables better design optimization of FinFETs and provides accurate prediction of its characteristics. Hsiao *et al.* [19] developed a 3D quantum transport model, based on the solution of NEGF and Poisson equation, to investigate electron transport in a GaAs GAA FinFETs. The reported solution considered electron-phonon, ionized impurity and surface roughness scatterings to assess the drain current. Zhang. *et al.* [92] studied the transport properties in nano FinFETs and their study concluded that transport properties are controlled by Fermi energies variation from source-drain sides of a FinFET.

The inventions of 3D devices has urged researchers to develop new electronic switches and circuits for improved performance. In 2022, Huang *et al.* [93] developed a flash memory involving 3D NOR gates. They investigated their proposed 3D device structure, integration scheme and circuit architecture to obtain 3D NOR flash devices. Their reported memory devices have large read current i.e.,

TABLE 2.3: A brief overview of quantum transport mechanisms of FinFETs.

Author	Ref	Description
Kim (2004)	[59]	2D quantum transport model of DG FinFETs.
Shao (2005)	[86]	3D quantum transport model of DG FinFETs.
Khan (2008)	[87]	Ballistic transport model of trigate FinFETs.
Natori (2008)	[88]	Quantum capacitance study in ballistic NW FinFETs.
Dastjerdy (2011)	[89]	3D quantum model of NW FinFETs.
Sabry (2011)	[90]	Quantum transport technique in FinFETs.
Deyasi (2018)	[91]	Gate structure study in GAA FinFETs.
Hsiao (2019)	[19]	Elastic and inelastic scattering in GAA FinFETs.
Zhang (2019)	[92]	FET current pattern study at atomic scale.
Huang (2022)	[93]	Development of 3D NOR gate based memory.
Zhang (2022)	[94]	Scallop shape FinFETs for improved SCEs.
Cheng (2022)	[95]	SiGe vertically stacked GAA FinFETs.

110 μA/μm and by conducting writing-erasing test, they observed writing speed of 10 μs and erasing speed of 100 ms.

Recently, Zhang *et al.* [94] investigated the performance of scallop-shaped FinFETs and attained an improved driving current compared to conventional FinFETs. Based on the observed characteristics they claimed that, scallop-FinFET is a promising candidate beyond current FinFET technology. Cheng *et al.* [95] explored fabrication and characterization of vertically stacked 4-level nanowire

transistors and reported subthreshold slope of 77 mV/dec, drain induced barrier–lowering of 19 mV/V and $g_m = 83.35\ \mu S/\mu m$ with improved SCEs.

2.4 Analytical Models

A model representing a semiconductor device response usually consists upon a mathematical expression based on the device material properties and its geometry. The model will be an acceptable one if it can generate the device characteristics, as a function of applied bias, same as that of actual device data. A device model can either be a mathematical relationship based upon the device physics or an empirical relation dependent on the device geometrical parameters. A physics based model is referred to as an analytical model, which uses a set of equations that best describe the behavior of a given device [25]. Such a model provides a reasonably good understanding about the physical operation of the device. Involving device physics, in a comprehensive way, in model development, usually leads to a complex mathematical formulation, and an analytical solution of such a formulation becomes a tedious job, which is usually not preferred by a design engineer.

On the other hand, an empirical technique, based on the device geometry, can be employed to predict its behavior. However, such a technique provides limited understanding pertaining to the device's electrical response as a function of applied bias. In an empirical technique, the device geometrical parameters are used in a mathematical expression in such a way that, by changing the device applied bias, the response received from the developed empirical expression is the same as that of the device experimental characteristics [2, 102]. Thus, an empirical technique provides a reasonable ease to model the device characteristics and therefore it is a preferred approach in CAD applications.

In general, in an empirical model there are usually fitting variables and involvement of large number of fitting variables is considered a negative feature of an empirical model. It is therefore always preferred to develop an empirical expression to generate a device characteristics by involving: a) device geometrical variables and for

TABLE 2.4: DC model expressions for FinFET $I-V$ characteristics.

Author	Ref	$I-V$ Model
Taur (2004)	[96]	$I_{ds} = 2\mu\frac{W}{L_g}C_{ox}\left(2V_T\right)^2\left[\beta tan\beta - \frac{\beta^2}{2} + r\beta^2 tan^2\beta\right]$
Conde (2005)	[97]	$I_{ds} = 2\mu\frac{W}{L_g}C_{ox}\left[V_{GF}\left(\psi_d - \psi_{so}\right) - \frac{1}{2}\left(\psi_d^2 - \psi_{so}^2\right)\right]$ $+\mu\frac{W}{L_g}C_{ox}4V_T\left(\psi_d - \psi_{so}\right)$ $+t_{si}k_bTn_i\left[e^{\beta\left(\psi_{0L}-V_{ds}\right)} - e^{\beta\psi_0}\right]$
Nikolaos (2012)	[98]	$I_{ds} = 2\mu\frac{W}{L_g}\frac{\epsilon_{ox}}{T_{ox}}\left(2V_T\right)^2\left[q_{is} - q_{id} + \frac{1}{2}\left(q_{is}^2 - q_{id}^2\right)\right]$
Paydavosi (2013)	[99]	$I_{ds} = 2\mu\frac{W}{L}\left[f\left(\psi_s\right) - f\left(\psi_d\right)\right]$ $f\left(\psi_s\right) = \frac{Q_{inv}^2}{2C_{ox}} + 2V_TQ_{inv} - V_T\left(5V_T\frac{\epsilon_{si}}{t_{si}} + Q_{bulk}\right)$ $\times\ln\left(5V_T\frac{\epsilon_{si}}{t_{si}} + Q_{bulk} + Q_{inv}\right)$ $f\left(\psi_d\right) = \frac{Q_{inv}^2}{2C_{ox}} + 2V_TQ_{inv} - V_T\left(5V_T\frac{\epsilon_{si}}{t_{si}} + Q_{bulk}\right)$ $\times\ln\left(5V_T\frac{\epsilon_{si}}{t_{si}} + Q_{bulk} + Q_{inv}\right)$
Kumari (2017)	[100]	$I_{ds} = \frac{k_BT\mu n_i\left[1 - exp(\frac{-qV_{ds}}{k_BT})\right]}{A+B}$ $A = \int_0^{L_u}\frac{1}{\int_0^{H_{fin}}\int_0^{T_{fin}} exp\left(\frac{q\psi_{tch1}}{kT}\right)dxdz}dy$

Ahmed (2019) [101]	$B = \int_{L_u}^{L_g} \frac{1}{\int_0^{H_{fin}} \int_0^{T_{fin}} exp\left(\frac{q\psi_{tch2}}{k_B T}\right) dxdz} dy$
	$I_{ds} = 2\mu(V)\frac{W}{L_g}(\acute{\psi}_d - \acute{\psi}_s)$
	$\acute{\psi}_s \approx -\frac{Q_{invs}^2}{2C_{ox}} - 2V_T Q_{invs} - 2V_T Q_{bulk} \ln(Q_{invs} + 2Q_{bulk})$
	$+2V_T Q_{\acute{z}s} + 2V_T \frac{Q_{bulk}}{Q_{invs} + 2Q_{bulk}} Q_{\acute{z}s}$
	$\acute{\psi}_d \approx -\frac{Q_{invd}^2}{2C_{ox}} - 2V_T Q_{invd} - 2V_T Q_{bulk} \ln(Q_{invd} + 2Q_{bulk})$
	$+2V_T Q_{\acute{z}d} + 2V_T \frac{Q_{bulk}}{Q_{invd} + 2Q_{bulk}} Q_{\acute{z}d}$

the case of FinFET they are: L_{fin}, T_{fin}, H_{fin}, L_g; b) applied bias V_{gs}, V_{ds}, and c) material electrical properties such as mobility μ, carrier velocity v_d etc.

Taur *et al.* [96], in 2004, presented an analytical model for DG FETs. The model consists of closed form solution of Poisson and current continuity equations and operates for all region of operations. They demonstrated the validity of their model by comparing the modeled output characteristics with 2D numerical solution without involving any fitting variables.

Conde *et al.* [97] presented a DC model for undoped trigate FinFETs. The study proposed a Poisson based single explicit analytical equation valid for all bias conditions and counts for drift and diffusion transports. The model is valid for long channel devices and showed deterioration when applied to short channel FinFETs [97].

In 2012, Nikolaos *et al.* [98] presented an analytical solution to predict DC characteristics of lightly doped FinFETs, taking into account quantum mechanical and

TABLE 2.5: Parameters used in the development of DC analytical models by different researchers.

Model	Ref.	L_g	T_{fin}	H_{fin}	V_{th}	T_{ox}	N	V_T	μ	ΔL_g	N_i
Taur (2004)	[96]	✓	✓	×	×	✓	×	✓	✓	×	✓
Conde (2005)	[97]	✓	✓	×	✓	✓	✓	✓	✓	×	✓
Raj (2008)	[103]	✓	✓	×	✓	✓	×	✓	✓	×	×
Yesayan (2011)	[104]	✓	✓	✓	×	✓	×	✓	✓	✓	×
Gosh (2012)	[105]	✓	✓	×	✓	✓	×	✓	✓	✓	✓
Fasarakis (2012)	[98]	✓	✓	✓	✓	✓	×	✓	✓	✓	×
Paydavosi (2013)	[99]	✓	✓	×	✓	✓	✓	✓	✓	×	✓
Duarte (2013)	[106]	✓	✓	×	✓	✓	✓	✓	✓	×	×
Kumari (2017)	[100]	✓	✓	✓	×	✓	✓	✓	×	✓	✓
Ahmed (2019)	[101]	✓	✓	✓	×	✓	×	✓	✓	×	✓

short channel effects. The proposed model used unified expressions for inversion charge and drain current which are valid for all regions of operation.

In 2013, Paydavosi *et al.* [99] presented first industry-standard compact model to simulate double, triple and GAA FinFETs. All important real device effects, such as short channel effects, quantum mechanical effects, mobility degradation and parasitic components effects are included in the model. In 2017, Kumari *et al.* [100] used a quasi 3D analytical model to predict FinFETs characteristics. In 2019, Ahmed *et al.* [101] developed a surface potential model of FinFET using a Poisson equation. A summary of FinFETs model expressions discussed hitherto are presented in Table 2.4. It is observed that most of the reported models, other than Ahmed [101], used a 2D Poisson equation, whereas a FinFET is a 3D device and to predict an accurate device response it is important that the 3D geometry should be taken into consideration.

A comprehensive literature survey is conducted for geometrical parameters that are used in various reported models. A number of researchers tried to present device models by incorporating device geometry, the detail of which is listed in Table 2.5. As evident from the table, almost all the researchers used L_g, T_{fin} and V_{th}, however, H_{fin} is mostly ignored because they simplified the problem by considering 2D geometry of the device. Therefore, the results generated by these models are prone to error when z-directed field increases with the decrease in device dimensions.

2.5 Estimation of FinFETs Characteristics by AI

In this era, computational power has observed phenomenal growth and use of computational based intelligence has attained an important role in every field of life including medicines, engineering, traffic control, town planning, oceanography, forestry etc. Such an intelligence where human decision making and planning is assisted by a machine, which is trained by an expert using appropriate configuration, design and data, is called artificial intelligence (AI). Training a computational

technique by a pre-defined scheme, using appropriate data, enables the machine to predict futuristic response with reasonable accuracy and hence the technique save a lot of resources without compromising on the accuracy of the targeted decision. Owing to these, AI based prediction is getting popularity in almost every field of life including semiconductor technology.

Device fabrication requires a high-tech industry and apart from that, to get a finish device, starting from its substrate to the end product, is a time consuming process. Changing a device geometrical variables, results into changed characteristics. Such a change in the device characteristics would be possible to predict, prior to its fabrication, if an appropriate trained AI tool is available. In recent past, AI based solutions have attracted strong attention and have been applied successfully in device modeling. In this process, a high-end computational resource would be required to train artificial neural networks (ANN), wherein a large number of neural units and/or regression weights are set and calibrated by multiple iterations (Epochs). Once the training is completed successfully with a good degree of accuracy, the AI system, afterwards can work efficiently with conventional computational resources. AI based prediction requires less memory, is more efficient and achieves a good level of accuracy, in relatively less time, compared to analytical and numerical techniques. However, AI model training requires big volume of data and quite a few iterations of training to get an acceptable accuracy. Table-2.6 summarizes AI based modeling techniques reported so far in the last two decades.

In 2009, Alam *et al.* [107] developed an ANN technique for small signal analysis of FinFET and based on the proposed model, they also designed a low noise amplifier. For the proof of the concept, they compared ANN results with a standard circuit simulation tool known as advance design software (ADS). In 2011, Marinkovic *et al.* [108], modeled S-parameters of different technologies such as GaAs HEMTs, GaN HEMTs and Si FinFETs for operating frequencies of 2 to 50 GHz using an AI technique. The AI based estimated modeled parameters were obtained as a function of bias, frequency, temperature and the device geometry. To validate their technique, they compared AI results with experimental data which showed a reasonable compliance. Additionally, the reported technique was also applied

TABLE 2.6: A summary of AI based FETs techniques developed to predict the device characteristics.

Author	Ref.	Description
Alam (2009)	[107]	Trained AC parameter of nano FinFETs.
Marinkovic (2011)	[108]	Trained RF performance of Si FinFETs.
Chen (2014)	[109]	Extrinsic capacitances of nano FinFETs.
He (2017)	[110]	Trained electrical characteristics of nano FinFETs.
Choi (2020)	[111]	Physical parameters optimization of Si MOSFETs.
Mehta (2020)	[112]	DC and AC performance of FinFETs.
Ghoshhajra (2022)	[113]	Improved performance of FinFETs.

successfully both on real and imaginary parts of the S-parameters independently, to same level of accuracy.

In 2014, Chen *et al.* [109] proposed a ML technique for the prediction of extrinsic capacitances of nano FinFETs. The dataset used for the training of the proposed network is taken from a quasi static electromagnetic software [114] by varying the geometrical parameters of FinFETs. In 2017, He *et al.* [110] evaluated DC characteristics of FinFETs using an ANN approach. They compared the results with the experimental data after the completion of training process. However, the validation of the proposed technique, as far as prediction of the device characteristics is concerned, is not reported by the authors. In 2020, Choi *et al.* [111] studied the manufacturing process of FETs and proposed an AI based technique to optimize it. They used a machine learning approach along with an holistic optimization technique in order to reduce the fabrication cost and time.

Mehta *et al.* [112] proposed a machine learning approach to predict the DC and CV characteristics of FinFETs, by taking datasets from simulated devices

using TCAD. They demonstrated the possibility to predict the device DC and CV characteristics without involving the device physics. However, they did not show the validity of their model using experimental data. Ghoshhajra. *et al.* [113] in 2022, presented a similar approach to predict the device DC characteristics by creating a mapping technique between input and targeted output characteristics of FinFETs. They employed an ANN, wherein they opted multiple input and single output approach and managed to predict the device DC characteristics with 96.5% accuracy after training their ANN with TCAD simulated data.

Numerous researchers, as listed in Table 2.6, claimed the prediction of FinFETs characteristics using ANN techniques. However, none of them studied the variation of the device characteristics as a function of its physical parameters, in an holistic way, such as: L_g; H_{fin}; T_{fin}; L_{fin}; T_{ox} and N_d. Thus, there is a need to develop a comprehensive ANN model, based on these parameters, capable to predict the device characteristics for any chosen device dimensions.

2.6 Thesis Motivation

Since FinFET technology is relatively new, there are numerous challenges associated to it for optimized device performance and understanding. Based on the research review carried out in the preceding sections, following research gaps, to be investigated in this thesis have been identified:

2.6.1 Research Gaps

a) Heterostructure AlGaN/GaN FinFETs are popular both for high frequency and high power applications. The output characteristics of AlGaN/GaN FinFETs are mainly driven by the 2DEG created at the interface. The current associated with the 2DEG could be referred to as I_{2D}, which mainly determines the depletion mode operation of such devices. On the other hand, in enhancement mode, the literature shows that the device is operational at unusually higher gate bias $V_{gs} \geq 2$ V.

Maintaining its characteristics at such a high gate bias indicates that, apart from 2DEG, some parallel conducting channels are also appearing, plausibly because of carriers inversion layer, which is potentially contributing into the drain current called I_{inv}. Thus, the total drain current would be $I_{ds} = I_{2D} + I_{inv}$. To evaluate I_{ds} of such devices where inversion and depletion both processes are taking place by varying the gate potential, there is a need to re-visit the device basic understanding. The literature survey showed that there is no such mathematical tool or model available, which can assess I_{ds} involving both I_{2D} and I_{inv} in a single FinFET. Thus, any attempt to develop such a model would be a contribution towards the understanding of nanoscale FinFETs capable to operate both in inversion as well as in depletion modes simultaneously.

b) To accommodate high frequency operation and to minimize SCEs, trigate FinFETs in nanoscale regime are fabricated. When $L_g \leq 10$ nm, the carrier transport is ballistic in nature and a solution of 3D Schrödinger wave equation as a function of applied bias is required to represent the transportation of carriers. The number density of these carriers can be known by solving a 3D Poisson equation under appropriate boundary conditions. Coupling 3D Schrödinger equation with 3D Poisson equation can lead to the evaluation of $I_{ds}(V_{ds}, V_{gs})$. So such a 3D technique to asses carriers responsible for current contribution should be more accurate in nature because it reflects the true geometry of the device. According to our assessment no such attempt has been reported in the literature where 3D Schrödinger wave equation and 3D Poisson equation have been solved simultaneously for nanoscale FinFETs with its experimental verification. Any such development will enhance the fundamental understanding of FinFET channel operation at nanoscale regime.

c) As discussed in Section 2.5, researchers in these days are actively involved in predicting FinFETs characteristics by developing ANN models. However, according to our survey, no ANN based model has yet been reported which involves all major device physical parameters such as L_g, H_{fin}, L_{fin} etc, to predict its characteristics. The development of any such model by considering all possible physical

parameters, which are required to be tunned by a design engineer for target characteristics, would be beneficial for the industry. It would save industrial time and resources, provided the model has the ability to predict the device characteristics as a function of target physical variables prior to its fabrication. In this respect, it is realized that the developed AI tool should be robust enough to predict the device output and transfer characteristics as a function of its fabrication parameters to a good degree of accuracy. Additionally, keeping in view the basic philosophy of AI, it can comfortably be claimed that, it would be an efficient technique compared to other such tools which are based on numerical solutions e.g., TCAD and COMSOL.

2.6.2 Problem Statement & Methodology

Based on the research gaps presented in the preceding section, following problem statements and associated research methodologies have been finalized to carry out the research work to be presented in this thesis.

a) To develop a comprehensive model to predict DC characteristics of heterojunction FinFETs both for depletion and inversion modes of operation

In this part of research, it is proposed that a model which can predict the DC characteristics of nanoscale heterojunction FinFETs both for depletion as well as for inversion modes of operation simultaneously, will be developed. It is an established fact that for depletion mode devices at $V_{gs} = 0$ V, $I_{ds} \neq 0$ A and at $V_{gs} = V_{th}$, $I_{ds} = 0$ A, and when the device is operated in enhancement mode, under such scenario, V_{gs} will have a polarity opposite to that of depletion mode V_{gs} polarity. However, V_{gs} in enhancement mode of operation, shall allow a limited variation, i.e., $V_{gs} \lesssim \phi_B$ where ϕ_B is the built-in potential. If the device maintains its operation at $V_{gs} > \phi_B$, this is an indication that a new conducting path is created inside the device which is contributing in the flow of current beside depletion mode current. Such a conducting path may be associated to the accumulation of inversion carriers at the interface of the gate, connecting

the drain-source terminal. Under such circumstances, it can be assumed that $I_{ds} = I_{2D} + I_{inv}$. To develop a model by incorporating this concept, one can proceed first to evaluate I_{2D} by considering carrier concentration (n_s) defining 2DEG of the heterojunction. Once n_s is known for the given geometry, the linear as well as the saturation current can be assessed using device physical dimensions and field distribution inside the channel. On the other hand, inversion mode current can be evaluated independently by considering the device as MOS structure where at the interface, inversion layer is created, contributing into the flow of current. At the end of evaluation, both the concepts, 2DEG and MOS, can be coupled together to develop a unified model which could be referred to as depletion/inversion model of FinFETs. For both the cases i.e., depletion and inversion, a standard Poisson equation shall be solved using appropriate boundary conditions and the accuracy of the solution along with the validity of the developed model can eventually be assessed by comparing the modeled and experimental data of devices with known dimensions.

b) To develop a 3D analytical model based on ballistic transport mechanism for output characteristics of nano-FinFETs

In this part of research, it is proposed that by involving ballistic carriers transport, which contributes significantly in nano FinFETs, one can develop a 3D model to predict output characteristics of such devices. In ballistic carriers transport, the carriers are represented by a wave function, so a 3D Schrödinger wave equation is required to be solved involving the device geometry and Fermi energy variations from source to drain. Since, the Schrödinger wave equation depends upon the potential energy of the system, which changes because of the applied potential, it is considered to be a difficult task to arrive at some analytical solution of the 3D Schrödinger wave equation representing the FinFET channel. Hence, an appropriate numerical technique will be applied to achieve a workable solution. On the other hand, the carriers, which are contributing in the channel current, would be evaluated possibly by solving a 3D Poisson equation for the given device geometry and bias conditions. Coupling Schrödinger-Poisson solutions, the output current as a function of applied bias will then be evaluated. The validity of the model

will be ensured by comparing the modeled and experimental characteristics for a range of FinFETs.

c) To develop an efficient and easy to handle AI technique to predict FinFETs characteristics

The semiconductor technology is considered to be an expensive technology and in order to cut the device cost, there is always a need before arriving at the final recipe, to predict the target device characteristics prior to its fabrication. Device characteristics prediction can be realized by designing an intelligent AI based system. To develop an ANN system for any given problem, a dataset of reasonable size is required, to train the network for future prediction. In this respect, it is proposed that a dataset of DC characteristics can be generated using an established software tool (COMSOL, TCAD etc) by varying the device physical dimensions such as L_g, H_{fin}, T_{fin}, L_{fin}, etc. Distinct subsets of the data will be used for training and testing of the network to achieve an acceptable accuracy. After successful training, the network will be able to predict the device characteristic by using an input vector comprising of the same parameters as that of training. The accuracy of ANN model will be checked by using standard tool such as COMSOL. It is a known fact that the simulation tools based on numerical solutions require high computational resources and they are heavy in time. However, an ANN based system, after achieving the required training accuracy, should be able to predict the device characteristics in exceptionally less time. Hence, the technique can potentially be employed to reduce product cost and industrial process time.

2.7 Summary

In this chapter, a comprehensive literature survey of FinFETs, their operations, associated materials and device analytical models are presented. It has been shown that FinFET geometry and fabrication material are the two striking parameters which determine its characteristics. It has also been established, by analyzing numerous research studies of heterostructure FinFETs, that 2DEG created by

two dissimilar semiconductors offers improved FinFETs characteristics. Transport mechanism of carriers has also been discussed exhaustively for nanoscale FinFETs, which plays an important role in determining their operations. Moreover, several mechanisms which influence the transportation of carriers in FinFETs and their ultimate impact on output current have been discussed. Models developed by various researchers involving 2D and 3D device geometry are also presented along with their limitations. The advancements made by AI in semiconductor industry in the recent past has been discussed especially, with respect to FETs technologies. It has been observed that AI models developed so far have limitations. This is because they do not incorporate all crucial geometrical parameters that define the performance of FinFETs. Hence these models are prone to error. Lastly, based on the conducted literature survey, some research gaps have been identified and hypotheses for the proposed research and associated methodologies have been presented.

Chapter 3

A Unified Depletion/Inversion Model for Heterojunction Trigate FinFETs DC Characteristics

3.1 Introduction

In recent years, FinFETs have become the gold standard in the electronic industry due to their superior properties in comparison to conventional FETs [115, 116]. Their trigate nature suppresses the short channel effects [117], which consequently improves the device transconductance, reduces its leakage current and enhances the device scalability [118–120]. AlGaN/GaN FinFETs have the potential to further supplement FET development owing to their improved 2DEG characteristics and temperature stability [21, 77, 80]. Since they are fabricated using wide bandgap materials, these devices have the potential to offer stable characteristics at elevated temperatures, and thus lead the way for high density electronics [121–125]. The trigate nature of the FinFET incorporates all the advantages of the bulk FinFET, while the AlGaN/GaN heterojunction, which forms the 2DEG, gives higher carrier concentration [126], higher saturation velocity [127] and superior temperature-dependent performance [128].

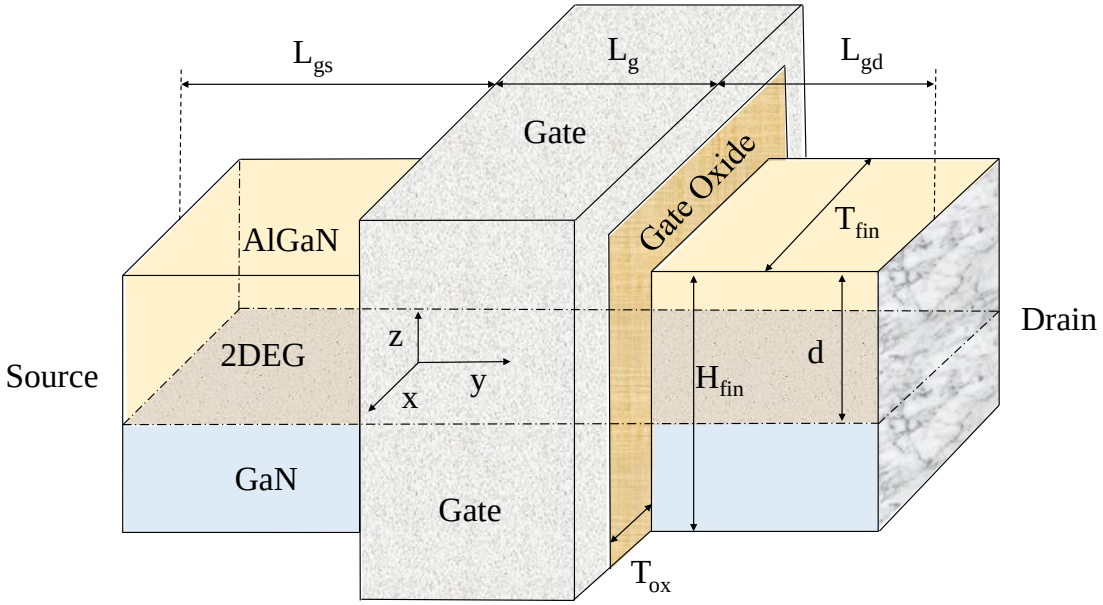

FIGURE 3.1: 3D view of an AlGaN/GaN FinFET channel.

To help the device attain its maximum potential, mathematical models which correlate the effects of the physical dimensions of the device and its characteristic are required. Fig. 3.1 shows a 3D view of an AlGaN/GaN FinFET. To model such a device, the effects of the trigate must be taken into account while evaluating the current flow between the drain and source electrodes. The total current in such a device is the combination of 2DEG and side channel (inversion) currents [32], which must be evaluated separately for accurate computation of drain current.

In this chapter, a comprehensive $I-V$ model is proposed, which can predict the output and transfer characteristics of trigate AlGaN/GaN FinFETs both in the depletion as well as in the inversion mode of operations. The proposed model uses a modified definition of n_s, presented in Ref. [11], to cater for the effects of the side gates on 2DEG depletion. Inversion current is modeled using the potential distribution acquired by the solution of a 2D Poisson equation. The total current is the sum of both the inversion and 2DEG currents. To the best of our knowledge, there is no such model reported in literature which can assess both depletion/inversion characteristics simultaneously. Authors of Ref. [78, 79, 129] have established models based on the physics of the device to assess the effects of FinFET geometry on threshold voltages, but not the entire $I-V$ characteristics.

In Ref. [82], an attempt has been made to present an analytical model for trigate AlGaN/GaN FinFETs which have no oxide layer beneath the gate electrode. Such a device cannot operate at a relatively high forward bias because of high leakage current and, as a result, there is no possibility of inversion layer formation at the oxide-metal interface. Hence, a model developed for such devices will have limitations in predicting $I-V$ characteristics under inversion. Therefore, the model presented in Ref. [82] which involves the 2DEG current alone, can predict $I-V$ characteristics under the depletion mode only and ceases to work when the device operates in the inversion mode.

3.2 AlGaN/GaN FinFET Model

To evaluate the drain to source current of an AlGaN/GaN FinFET, consider Fig. 3.1. The band diagram of the heterostructure FinFET is given in Fig. 3.2, Because of the bandgap discontinuity between AlGaN and GaN layers, 2DEG is created at the interface, which will be available for conduction and its thickness can be controlled by the gate. Hence the structure of the device by and large allows operation in the depletion mode and the device under consideration is an n-type channel. In this mode, 2DEG would be the major contributor to the channel current. As V_{gs} increases, 2DEG begins to un-deplete, while activating the inversion process, which will eventually define the side channels. Thus, the total current in such a FinFET would be a combination of both 2DEG and inversion currents represented by

$$I_{ds} = I_{inv} + I_{2D} \tag{3.1}$$

While proceeding with the model, it is assumed that I_{inv} and I_{2D} are independent of each other and can hence be modeled separately. To get total I_{ds} of a trigate AlGaN/GaN FinFET, both currents can be summed together as given by Eq. (3.1). It is further assumed that; a) inversion only occurs on the two side gates of trigate FinFET; b) 2DEG gets depleted independently from the three sides of the gate and c) carriers of 2DEG and those in the inversion layer move with their

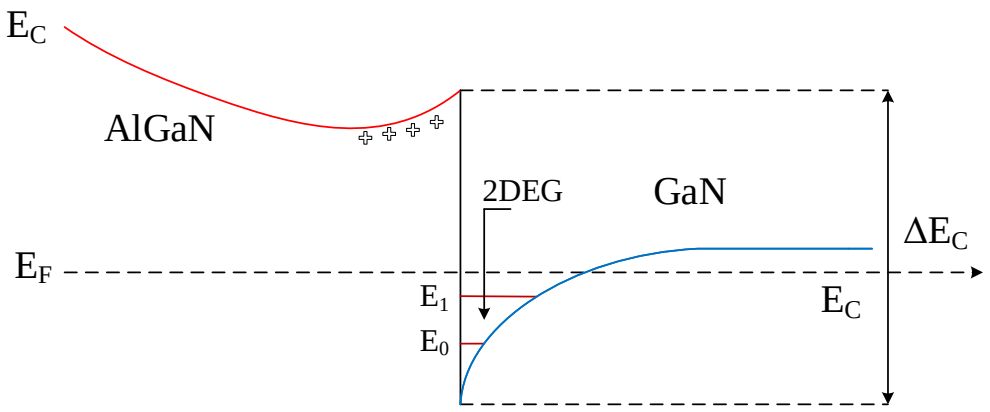

FIGURE 3.2: Energy band diagram of Heterostructure FinFETs.

respective mobilities. The proposed model is a steady-state model since it does not predict transient response of the device and its validity is for $V_{ds} \geq 0$ and $V_{gs} \geq V_{th}$.

3.2.1 2DEG Current

Consider the $x-z$ cross-section of the device as illustrated by Fig. 3.3, wherein it is evident that 2DEG is confined in the $x-y$ dimension and the gate of the device depletes the 2DEG carriers from the $x-z$ plane. Hence, the y dimension has no role in determining the current of the device. Consequently, the Poisson equation in 2D can be applied on the device geometry as shown below

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial z^2} = -\frac{q}{\epsilon_A} N_d \tag{3.2}$$

Since 2DEG acts as a sheet with infinitesimal width in the z direction, and with the assumption that both the top and side gates act on it independently, the applied voltage on the 2DEG can be divided as

$$V = V_1(x) + V_2(z) \tag{3.3}$$

Since

$$\frac{\partial^2 V_2}{\partial z^2} = -\frac{qN_d}{3\epsilon_A} \tag{3.4}$$

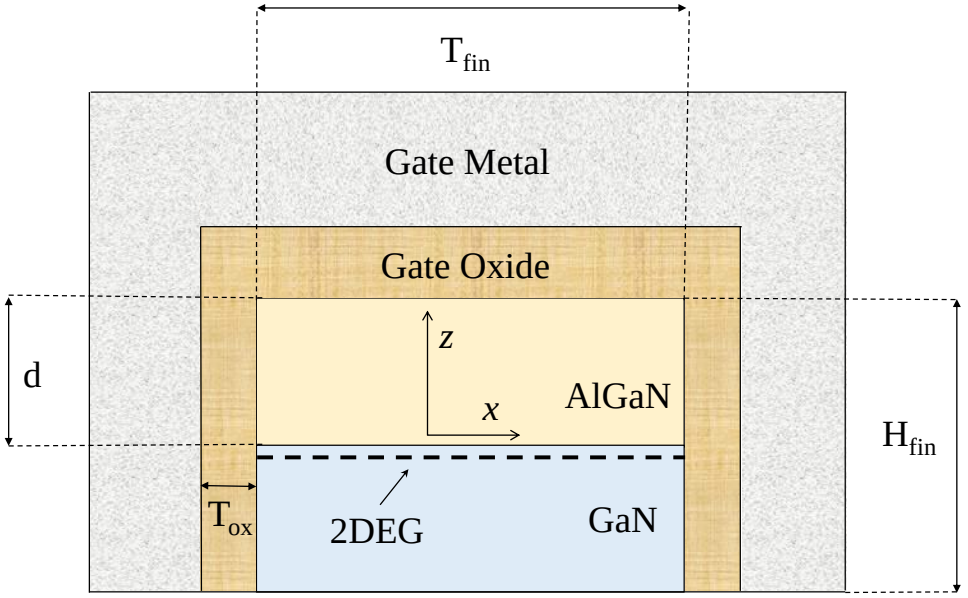

FIGURE 3.3: $x-z$ cross-sectional view of an AlGaN/GaN FinFET.

Integration of above equation results in

$$\frac{\partial V_2}{\partial z} = -\frac{qN_d}{3\epsilon_A}z + c_1 \tag{3.5}$$

and

$$\left.\frac{\partial V_2}{\partial z}\right|_{z=0} = \frac{q}{\epsilon_{eff}}(\sigma - n_s) \tag{3.6}$$

where, σ is the sheet charge density and ϵ_{eff} is the effective permittivity of 2DEG as defined in Ref. [130]. c_1 can be found from above equation as,

$$c_1 = \frac{q}{\epsilon_{eff}}(\sigma - n_s) \tag{3.7}$$

so using c_1, Eq. (3.5) becomes,

$$\frac{\partial V_2}{\partial z} = -\frac{qN_d}{3\epsilon_A}z + \frac{q}{\epsilon_{eff}}(\sigma - n_s) \tag{3.8}$$

Integrating Eq. (3.8) once again to get V_2,

$$V_2 = -\frac{qN_d}{6\epsilon_A}z^2 + \frac{q}{\epsilon_{eff}}(\sigma - n_s)z \tag{3.9}$$

Now from Eqs. (3.4) and (3.2), one can write

$$\frac{\partial^2 V_1}{\partial x^2} - \frac{qN_d}{3\epsilon_A} = -\frac{qN_d}{\epsilon_A} \tag{3.10}$$

therefore,

$$\frac{\partial^2 V_1}{\partial x^2} = -\frac{2qN_d}{3\epsilon_A} \tag{3.11}$$

Integrating Eq. (3.11),

$$\frac{\partial V_1}{\partial x} = -\frac{2qN_d}{3\epsilon_A}x + c_2 \tag{3.12}$$

Using the boundary conditions

$$\left.\frac{\partial V_1}{\partial x}\right|_{x=T_{fin}/2} = \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big) \tag{3.13}$$

c_2 can be found by substituting Eq. (3.13) into Eq. (3.12)

$$c_2 = \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big) + \frac{2qN_dT_{fin}}{3\epsilon_A \times 2} \tag{3.14}$$

Using c_2 in Eq. (3.12) and integrating it once again to find V_1

$$V_1 = -\frac{qN_d}{3\epsilon_A}x^2 + \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big)x + \frac{qN_dT_{fin}}{3\epsilon_A}x \tag{3.15}$$

Using V_1 from Eq. (3.15) and V_2 from Eq. (3.9) into Eq. (3.3) to find the applied voltage on 2DEG,

$$\begin{aligned} V = -\frac{qN_d}{3\epsilon_A}x^2 + \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big)x + \frac{qN_dT_{fin}}{3\epsilon_A}x - \\ \frac{qN_d}{6\epsilon_A}z^2 + \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big)z \end{aligned} \tag{3.16}$$

Now, considering the device geometry, V at $z = d$ and $x = T_{fin}/2$

$$V = \phi_b - V_{gs} + V\big(y\big) + \left(\frac{E_F - \Delta E_c}{q}\right) \tag{3.17}$$

Here, $V\big(y=0\big)=V_s$ and $V\big(y=L_g\big)=V_d$. Now, comparing Eqs. (3.17) and (3.16)

$$\phi_b - V_{gs} + V\big(y\big) + \left(\frac{E_F - \Delta E_c}{q}\right) = -\frac{qN_d}{12\epsilon_A}T_{fin}^2 + \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big)T_{fin} + \frac{qN_dT_{fin}}{6\epsilon_A}T_{fin} - \frac{qN_d}{6\epsilon_A}d^2 + \frac{q}{\epsilon_{eff}}\big(\sigma - n_s\big)d \tag{3.18}$$

$$n_s = \frac{\epsilon_{eff}}{q\big(T_{fin}/2+d\big)}\left[V_{gs} - V_{th} - \frac{E_F}{q} - V\big(y\big)\right] \tag{3.19}$$

here,

$$V_{th} = \phi_b - \frac{\Delta E_c}{q} + \frac{qN_d}{6\epsilon_A}d^2 - \frac{qN_d}{12\epsilon_A}T_{fin}^2 - \frac{\sigma q\big[T_{fin}/2+d\big]}{\epsilon_{eff}} \tag{3.20}$$

and E_F can be expressed as a function of n_s as [11]

$$E_F = \zeta_1 + \zeta_2 n_s^{1/2} + \zeta_3 n_s \tag{3.21}$$

where $\zeta_{1,2,3}$ are temperature-dependent parameters. So Eq. (3.19) can be written as,

$$n_s = \frac{\epsilon_{eff}}{q\big(T_{fin}/2+d\big)}\left[V_{gs} - V_{th} - \frac{\zeta_1}{q} - \frac{\zeta_2 n_s^{1/2}}{q} - \frac{\zeta_3}{q}n_s - V\big(y\big)\right] \tag{3.22}$$

Let $\lambda_1=\zeta_1/q$; $\lambda_2=\zeta_2/q$; $\lambda_3=\zeta_3/q$, which modifies Eq. (3.22) as

$$n_s = \frac{\epsilon_{eff}}{q\big(T_{fin}/2+d\big)}\left[V_{gs} - V_{th} - \lambda_1 - \lambda_2 n_s^{1/2} - \lambda_3 n_s - V\big(y\big)\right] \tag{3.23}$$

Using quadratic manipulation

$$n_s = \left[\frac{-\lambda_2 \pm \sqrt{\lambda_2^2 + 4\lambda_4\big(V_{gs} - V_{th} - V\big(y\big) - \lambda_1\big)}}{2\lambda_4}\right]^2 \tag{3.24}$$

where,

$$\lambda_4 = \lambda_3 + \frac{q\big(T_{fin}/2+d\big)}{\epsilon_{eff}} \tag{3.25}$$

Eq. (3.24) is referred to as a modified definition of n_s for trigate FinFET and can be used to assess 2DEG current as

$$I_{2\mathrm{D}} = qWn_s\upsilon_d\big(y\big) \tag{3.26}$$

where,

$$\upsilon_d(y) = \begin{cases} \dfrac{\mu_0 E_y}{1 + E_y/2E_{sat}}, & \text{for} \quad E_y = dV(y)/dy < 2E_{sat} \\ \upsilon_{sat}, & \text{for} \quad E_y = dV(y)/dy > 2E_{sat} \end{cases} \tag{3.27}$$

3.2.1.1 Linear Region Current

In the linear region of operation, the device behaves as a resistor such that the current is directly proportional to the applied field which falls in the direction of the current. Keeping in view, the geometry shown in Fig. 3.1, the field component E_y is responsible to control the current flowing between drain & source, and the total linear current for this region of operation can then be obtained by integrating the current expression over the gate length, L_g, as shown below

$$\int_o^{L_g} I_{2D(l)} dy = \int_o^{L_g} qWn_s \frac{\mu_0 E_y}{1 + E_y/2E_{sat}} dy \tag{3.28}$$

$$I_{2D(l)} L_g = \int_o^{L_g} qWn_s \frac{\mu_0 E_y 2E_{sat}}{2E_{sat} + E_y} Eydy \tag{3.29}$$

As $E_y = dV/dy$; $V_L = E_{sat}L_g$; $\upsilon_{sat} = \mu_0 E_{sat}$; $V_{ds} = E_y L_g$, changing limits,

$$I_{2D(l)} L_g = qW \int_o^{L_g} n_s \frac{2\upsilon_{sat}}{2V_L + V_{ds}} \frac{dV}{dy} dy \tag{3.30}$$

Let $\alpha = qW\upsilon_{sat}/\lambda_4$ so, Eq. (3.30) becomes

$$I_{2D(l)} L_g = \frac{2\lambda_4 \alpha}{2V_L + V_{ds}} \int_0^{V_{ds}} n_s dV \tag{3.31}$$

Assume, $V_{g1} = V_{gs} - V_{th} - \lambda_1$ and substituting n_s from Eq. (3.24) to Eq. (3.31)

$$I_{2D(l)} L_g = \frac{2\lambda_4 \alpha}{2V_L + V_{ds}} \int_0^{V_{ds}} \left[\frac{-\lambda_2 \pm \sqrt{\lambda_2^2 + 4\lambda_4 \left[V_{g1} - V(y)\right]}}{2\lambda_4} \right]^2 dV \tag{3.32}$$

$$I_{2D(l)} = \frac{\alpha}{2\lambda_4(2V_L + V_{ds})} \int_0^{V_{ds}} \left(\lambda_2^2 + 4\lambda_4 \left[V_{g1} - V(y)\right] + \lambda_2^2 - 2\lambda_2 \sqrt{\lambda_2^2 + 4\lambda_4 \left[V_{g1} - V(y)\right]} \right) dV \tag{3.33}$$

$$I_{2D(l)} = \frac{\alpha}{2V_L + V_{ds}} \Bigg(\left[\frac{\lambda_2^2}{\lambda_4} V(y) + 2V_{g1} V(y) - V(y)^2 \right] \Bigg|_0^{V_{ds}} - \int_0^{V_{ds}} \frac{\lambda_2}{\lambda_4} \sqrt{\lambda_2^2 + 4\lambda_4 V_{g1} - 4\lambda_4 V(y)} dV \Bigg) \tag{3.34}$$

As it is known that,

$$\int \sqrt{ax+b} dx = \left(\frac{2b}{3a} + \frac{2x}{3} \right) \left(\sqrt{ax+b} \right) \tag{3.35}$$

$$I_{2D(l)} = \frac{\alpha}{2V_L + V_{ds}} \Bigg(\frac{\lambda_2^2}{\lambda_4} V_{ds} + 2V_{g1} V_{ds} - V_{ds}^2 - \Bigg[\left(\frac{\lambda_2^2 + 4\lambda_4 V_{g1}}{-6\lambda_4} + \frac{2V(y)}{3} \right) \left(\frac{\lambda_2^2}{\lambda_4} \right) \sqrt{1 + \frac{4\lambda_4 V_{g1}}{\lambda_2^2}} \Bigg] \Bigg|_0^{V_{ds}} \Bigg) \tag{3.36}$$

Using the approximation, $[4\lambda_4 V(y) << \lambda_2^2 + 4\lambda_4 V_{g1}]$

$$I_{2D(l)} = \frac{\alpha}{2V_L + V_{ds}} \left(V_{ds} \left[2V_{g1} + \frac{\lambda_2^2}{\lambda_4} \left(1 - \frac{2}{3} \sqrt{1 + \frac{4\lambda_4 V_{g1}}{\lambda_2^2}} \right) \right] - V_{ds}^2 \right) \tag{3.37}$$

$$I_{2D(l)} = \frac{\alpha(2V_{ds} V_{g2} - V_{ds}^2)}{2V_L + V_{ds}} \tag{3.38}$$

where

$$V_{g2} = V_{g1} + \frac{\lambda_2^2}{2\lambda_4} \left(1 - \frac{2}{3} \sqrt{1 + \frac{4\lambda_4 V_{g1}}{\lambda_2^2}} \right) \tag{3.39}$$

3.2.1.2 Saturation Region Current

In saturation region of operation, the V_{ds} reaches $V_{ds(sat)}$ and at that point velocity of carrier attain its maximum velocity referred to as v_{sat}. The device in this region of operation becomes independent of V_{ds} and behaves as current source. The current density (J) for this region of operation becomes $J = Qnv_s$, which can be translated into saturation current as given below

$$I_{2D(S)} = qWv_{sat} n_s \Big|_{V_{ds} = V_{d(sat)}} \tag{3.40}$$

Now using n_s from Eq. (3.24) and applying the limits

$$I_{2D(S)} = \frac{qwv_{sat}\lambda_4}{\lambda_4}\left(\frac{-\lambda_2 + \sqrt{\lambda_2 + 4\lambda_4(V_{g1} - V_{d(sat)})}}{2\lambda_4}\right)^2 \tag{3.41}$$

Using α and quadratic manipulation

$$I_{2D(S)} = \frac{\alpha}{4\lambda_4}\left[2\lambda_2^2 + 4\lambda_4 V_{g1} - 4\lambda_4 V_{d(sat)} - 2\lambda_2\sqrt{\lambda_2^2 + 4\lambda_4 V_{g1} - 4\lambda_4 V_{d(sat)}}\right] \tag{3.42}$$

Using approximation, $\left[4\lambda_4 V_{d(sat)} << \lambda_2^2 + 4\lambda_4 V_{g1}\right]$, yields

$$I_{2D(S)} = \alpha\left(V_{g1} + \frac{\lambda_2^2}{2\lambda_4}\left[1 - \sqrt{1 + \frac{4\lambda_4 V_{g1}}{\lambda_2^2}}\right] - V_{d(sat)}\right) \tag{3.43}$$

Using Eq. (3.39), $I_{2D(S)}$ becomes

$$I_{2D(S)} = \alpha(V_{g2} - V_{d(sat)}) \tag{3.44}$$

Comparing Eqs. (3.44) and (3.38) at $V(y) = V_{d(sat)}$

$$\alpha[V_{g2} - V_{d(sat)}] = \frac{\alpha[V_{d(sat)}V_{g2} - V_{d(sat)}^2]}{2V_L + V_{d(sat)}} \tag{3.45}$$

So,

$$V_{d(sat)} = \frac{2V_{g2}V_L}{(V_{g2} + 2V_L)} \tag{3.46}$$

which, by using Eq. (3.44), gives

$$I_{2D(S)} = \frac{\alpha V_{g2}^2}{V_{g2} - 2V_L} \tag{3.47}$$

For $V_{ds} > V_{d(sat)}$, channel length modulation occurs which can be represented as

$$I_{2D(S)} = \frac{\alpha V_{g2}^2}{V_{g2} + (2V_L - E_{sat}\Delta L_g)} \tag{3.48}$$

where ΔL_g is the channel length modulation [11].

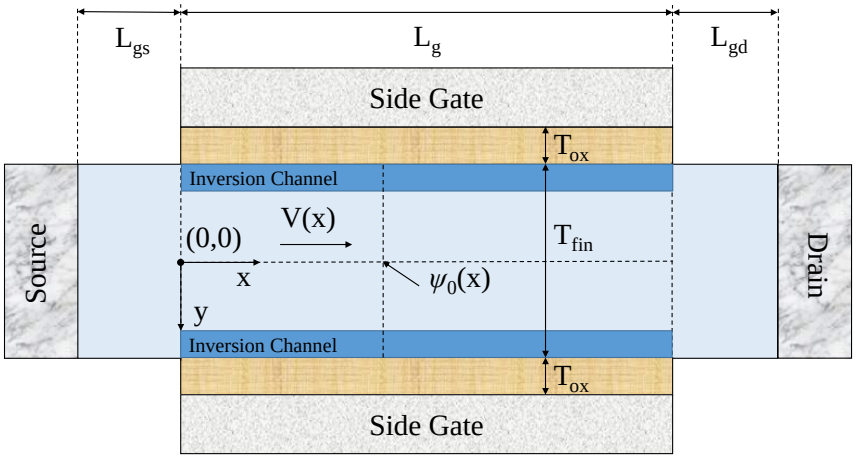

FIGURE 3.4: $x-y$ cross-sectional view of an AlGaN/GaN FinFET wherein the formation of the inversion layer is shown at the two side gates of the device.

3.2.2 Inversion Current

For a given n_s, the total magnitude of I_{ds} can be controlled by the width, W, of the device; whereas, the ratio H_{fin}/T_{fin} determines the ratio of $I_{2\mathrm{D}}$ and I_{inv} in I_{ds}. If H_{fin}/T_{fin} is higher, there would be a considerable ratio of I_{inv} in the total current and vice versa. It is assumed that inversion only occurs in GaN, which creates two side channels that generate a conducting path between the drain and the source. A schematic showing the formation of the two side channels is given in Fig. 3.4. In a MOS structure, there is a depletion layer which appears inside the semiconductor because of the emission of carriers from the semiconductor to the metal-oxide layer. The thickness of the depletion at equilibrium is determined by the potential resulting from the difference of work functions of the MOS structure [8]. In such a structure, if the gate bias is increased towards a direction which causes a reduction in the depletion, then at zero depletion there is a possibility that carriers of opposite polarity from the bulk could be attracted to the semiconductor-oxide interface. This will generate a channel between the drain and the source as shown in Fig. 3.4. This process is referred to as channel inversion. Consider the $x-y$ crossection of the device as shown in Fig. 3.4. Since the top gate is ignored, the 3D potential equation is reduced to

$$\frac{\partial^2\psi}{\partial y^2} = \frac{q}{\epsilon_G} n_i \exp\left(\frac{\psi - V(x)}{V_T}\right) \tag{3.49}$$

where

$$V_T = \frac{k_B T}{q} \tag{3.50}$$

Seeing as the device is symmetric about the y-axis, the domain $0 \leq y \leq T_{fin}/2$ is considered and multiplied by a factor of 2, so

$$\frac{\partial^2 \psi}{\partial y^2} = 2\frac{q}{\epsilon_G} n_i \exp\left(\frac{\psi - V(x)}{V_T}\right) \tag{3.51}$$

Integrating Eq. (3.51),

$$\left(\frac{d\psi}{dy}\right)^2 = \frac{2V_T q n_i}{\epsilon_G} \exp\left(\frac{\psi - V(x)}{V_T}\right) + c \tag{3.52}$$

where c is a constant. Eq. (3.52) is subject to the following boundary conditions

$$\left.\frac{\partial \psi}{\partial y}\right|_{y=0} = 0 \qquad \text{and} \qquad \psi(y=0) = \psi_0 \tag{3.53}$$

Now,

$$\frac{d\psi}{dy} = \sqrt{\frac{2V_T q n_i}{\epsilon_G}\left[\exp\left(\frac{\psi - V(x)}{V_T}\right) - \exp\left(\frac{\psi_0 - V(x)}{V_T}\right)\right]} \tag{3.54}$$

Integrating the above equation

$$\int dy = \frac{\int \partial\psi}{\sqrt{\frac{2V_T q n_i}{\epsilon_G}\left[\exp\left(\frac{\psi - V(x)}{V_T}\right) - \exp\left(\frac{\psi_0 - V(x)}{V_T}\right)\right]}} \tag{3.55}$$

Simplification yields

$$y\sqrt{2\frac{V_T q n_i}{\epsilon_G}} = \frac{\int \partial\psi(x)}{\left(\left[\sqrt{\exp\left(\frac{\psi - V(x)}{V_T}\right)}\right]^2 - \left[\sqrt{\exp\left(\frac{\psi_0 - V(x)}{V_T}\right)}\right]^2\right)^{1/2}} \tag{3.56}$$

To simplify Eq. (3.56) further, let

$$\sqrt{\exp\left(\frac{\psi - V(x)}{V_T}\right)} = a\sec\theta \tag{3.57}$$

and

$$\sqrt{\exp\left(\frac{\psi_0 - V(x)}{V_T}\right)} = a \tag{3.58}$$

Partial differential of Eq. (3.57) gives

$$\frac{1}{2}\left[\exp\left(\frac{\psi - V(x)}{V_T}\right)\right]^{-1/2} \exp\left(\frac{\psi - V(x)}{V_T}\right) \times \frac{\partial\psi}{V_T} = a\sec\theta\tan\theta\ \partial\theta \tag{3.59}$$

Combining Eqs. (3.57), (3.58) and (3.59) reveals

$$\partial\psi = 2V_T\tan\theta\ \partial\theta \tag{3.60}$$

So, Eq. (3.56) becomes

$$y\sqrt{2\frac{V_T q n_i}{\epsilon_G}} = \int \frac{2V_T\tan\theta}{\sqrt{a^2\sec^2\theta - a^2}}\partial\theta \tag{3.61}$$

As $a^2\sec^2\theta - a^2 = a^2\tan^2\theta$, so

$$y\sqrt{2\frac{V_T q n_i}{\epsilon_G}} = \int \frac{2V_T\tan\theta}{a\tan\theta}\partial\theta = \frac{2V_T\theta}{a} + c_4 \tag{3.62}$$

The expression for θ can be found from Eqs. (3.57) and (3.58) as,

$$\sec^{-1}\left[\sqrt{\exp\left(\frac{\psi - \psi_0}{V_T}\right)}\right] = \theta \tag{3.63}$$

In Eq. (3.62), $c_4 = 0$, using boundary conditions given by Eq. (3.53),

$$\sqrt{2\frac{q n_i a^2}{V_T\epsilon_G}} \times \frac{y}{2} = \theta \tag{3.64}$$

Using the substitution method,

$$\sqrt{2\frac{q n_i a^2}{V_T\epsilon_G}} \times \frac{y}{2} = \sec^{-1}\left[\sqrt{\exp\left(\frac{\psi - \psi_0}{V_T}\right)}\right] \tag{3.65}$$

By taking cosine and natural log of both sides one can write

$$q\frac{\psi-\psi_0}{2k_BT} = -\ln\left[\cos\left(y\times\sqrt{\frac{q^2n_i}{2\epsilon_Gk_BT}\exp\frac{(\psi_0-V(x))}{V_T}}\right)\right] \tag{3.66}$$

Now, at the oxide interface

$$Q_i = \epsilon_{ox}\frac{V_{gs}-V_{fb}-\psi(T_{fin}/2)}{T_{ox}} = \epsilon_G\frac{\partial\psi}{\partial y}\bigg|_{y=T_{fin}/2} \tag{3.67}$$

here, $C_{ox} = \epsilon_{ox}/T_{ox}$.

Combining Eqs. (3.54) and (3.67),

$$\begin{aligned} C_{ox}\left[V_{gs}-V_{fb}-\psi(T_{fin}/2)\right] &= \Bigg[2\epsilon_Gk_BTn_i \\ \times\left[\exp\left(\frac{\psi(T_{fin}/2)-V(x)}{V_T}\right)-\exp\left(\frac{\psi_0-V(x)}{V_T}\right)\right]\Bigg]^{\frac{1}{2}} \end{aligned} \tag{3.68}$$

Let

$$\beta = \sqrt{\frac{q^2n_i}{2\epsilon_Gk_BT}\exp\left(\frac{\psi_0-V(x)}{V_T}\right)}\times\frac{T_{fin}}{2} \tag{3.69}$$

So, $\psi(T_{fin}/2)$ from Eq. (3.66) become,

$$\psi(T_{fin}/2) = \psi_0 - 2V_T\ln\big(\cos\beta\big) \tag{3.70}$$

To find ψ_0, consider Eq. (3.69)

$$\beta\times\frac{2}{T_{fin}}\times\sqrt{\frac{2\epsilon_Gk_BT}{q^2n_i}} = \sqrt{\exp\left(\frac{\psi_0-V(x)}{V_T}\right)} \tag{3.71}$$

Taking natural log of Eq. (3.71)

$$\ln\big(\beta\big)+\ln\left[\frac{2}{T_{fin}}\times\sqrt{\frac{2\epsilon_Gk_BT}{q^2n_i}}\right] = \frac{1}{2}\left(\frac{\psi_0-V(x)}{V_T}\right) \tag{3.72}$$

So,

$$\psi_0 = V(x)+2V_T\ln\big(\beta\big)+2V_T\ln\left[\frac{2}{T_{fin}}\times\sqrt{\frac{2\epsilon_Gk_BT}{q^2n_i}}\right] \tag{3.73}$$

By using Eqs. (3.70) and (3.73), Eq. (3.68) becomes

$$C_{ox}\left[V_{gs}-V_{fb}-V(x)-2V_T\ln(\beta)-2V_T\ln\left(\frac{2}{T_{fin}}\sqrt{\frac{2\epsilon_G k_B T}{q^2 n_i}}\right)+2V_T\ln(cos\beta)\right]= \sqrt{2\epsilon_G K_B T n_i\left[\frac{\beta^2 cos^2\beta\left(\frac{2}{T_{fin}}\sqrt{\frac{2\epsilon_G k_B T}{q^2 n_i}}\right)^2}{V_T}-\frac{\beta^2\left(\frac{2}{T_{fin}}\sqrt{\frac{2\epsilon_G k_B T}{q^2 n_i}}\right)^2}{V_T}\right]} \tag{3.74}$$

After simplification

$$C_{ox}\left[V_{gs}-V_{fb}-V(x)-2V_T\ln(\beta)-2V_T\ln\left(\frac{2}{T_{fin}}\sqrt{\frac{2\epsilon_G k_B T}{q^2 n_i}}\right)+2V_T\ln(cos\beta)\right]= \frac{2}{T_{fin}}\times 2\epsilon_G V_T\times\beta tan\beta \tag{3.75}$$

Further simplification yields,

$$\frac{(V_{gs}-V_{fb}-V(x))}{2V_T}-\ln\left(\frac{2}{T_{fin}}\times\sqrt{\frac{2\epsilon_G V_T}{q n_i}}\right)=\ln(\beta)-\ln(cos\beta)+\frac{2\epsilon_G}{T_{fin}C_{ox}}\times\beta tan\beta \tag{3.76}$$

To evaluate the inversion current, consider

$$I_{inv}=\mu W Q_i\frac{dV}{dx} \tag{3.77}$$

Integrating Eq. (3.77) over the entire channel

$$\int_0^{L_g} I_{inv}dx=\mu W\int_0^{V_{ds}} Q_i(V)dV \tag{3.78}$$

$$I_{inv}=\frac{\mu W}{L_g}\int_{\beta_s}^{\beta_d} Q_i(B)\frac{dV}{d\beta}d\beta \tag{3.79}$$

Here, β_s and β_d are solutions of Eq. (3.76) for the source and drain regions, respectively. Using Eq. (3.67), one can write

$$Q_i(\beta)=\epsilon_G\frac{\partial\psi}{\partial y}\bigg|_{y=T_{fin}/2} \tag{3.80}$$

Using Eqs. (3.67), (3.74), and (3.75) in Eq. (3.80)

$$Q_i(\beta) = 2\epsilon_G \times \frac{4}{T_{fin}} V_T \beta \tan\beta \tag{3.81}$$

Differentiating Eq. (3.76)

$$\frac{dV(x)}{d\beta} = \frac{2V_T}{\beta} + 2V_T tan\beta + \frac{4\epsilon_G \times V_T}{T_{fin}C_{ox}} \times \frac{d}{d\beta}\left(\beta tan\beta\right) \tag{3.82}$$

Combining Eqs. (3.79), (3.81) and (3.82)

$$I_{inv} = \frac{\mu W}{L_g} \times \frac{4\epsilon_G}{T_{fin}} \times \left(2V_T\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\epsilon_G}{T_{fin}C_{ox}} \times \left(\beta\tan\beta\right)^2\right]_{\beta_d}^{\beta_s} \tag{3.83}$$

3.3 Result and Discussion

To validate the proposed model, devices having physical parameters as shown in Table 3.1 are selected. All physical dimensions of device T_1 and T_2 are identical except for H_{fin}. The thickness of the fin is of paramount importance in AlGaN/-GaN FinFETs which is meant to operate both in inversion as well as in depletion modes. If the thickness of the fin is comparable to two times the thickness of the AlGaN layer, the side gates will fully deplete the 2DEG at $V_{gs} = 0$ V and the device will only function as a normally off device (inversion mode only) [24]. Hence to allow the device to operate in both the depletion as well as in the inversion modes, it is important that T_{fin} must be appropriately scaled relative to the AlGaN layers of the device. Other device constants used for the simulation are reported in Table 3.2. Mobility, μ_0, is evaluated using numerical optimization and the value so achieved is comparable to data reported previously [23, 42, 131].

Fig. 3.5 shows the potential distribution inside the channel of the device T_1. The figure has been plotted using a MATLAB code developed for the purpose by employing Eq. (3.76). The dimensions of the fins are normalized, each by their respective length for simplicity. The figure shows three cross-sections of the channel. The plane to the left is the $x-y$ cross-section at $z = 0$, which represents

the 2DEG potential. It is plotted for two different V_{ds} and V_{gs} scenarios. Similarly, the plane to the right shows the potential variation along the $x-z$ cross-section. This cross-section is taken at $y = 0.7L_g$ and shows the effect of drain potential on the device. The plane in the middle shows the source side potential at $y = 0.3Lg$ and its variation with the side gates and the source terminal.

To predict $I-V$ characteristics of AlGaN/GaN FinFETs using the proposed model, V_{th} of the device is first evaluated using Eq. (3.20). This gives the minimum V_{gs} after which the device begins to conduct. For the region $V_{th} \leq V_{gs} \leq V_{fb}$,

TABLE 3.1: Physical parameters of different devices used in this study.

Parameters	$\boldsymbol{T_1}$[24]	$\boldsymbol{T_2}$[23]	$\boldsymbol{T_3}$[83]
L_g (μm)	5	5	0.1
L_{gs} (μm)	2	2	2.5
L_{gd} (μm)	17	17	2.5
T_{fin} (nm)	150	150	250×8
H_{fin} (nm)	250	120	200
T_{ox} (nm)	20	20	10
d (nm)	15	15	25
GaN (nm)	60	60	175
W (μm)	15	15	2
V_{fb} (V)	-0.4	-1.4	-1.5
V_{th} (V)	-5	-2	-4
μ_0 ($m^2V^{-1}s^{-1}$)	0.17	0.17	0.14
Oxide	Al_2O_3	Al_2O_3	HfO_2
ϵ_{ox}	9.1ϵ	9.1ϵ	25ϵ

TABLE 3.2: Physical constants used in this study.

Parameters	**Value**
n_i ($\times 10^{21}$ m^{-3})	1
k_B ($J.K^{-1}$)	1.38
T (K)	300
q ($\times 10^{-19}$ C)	1.6
ϵ ($\times 10^{-12}$ Fm^{-1})	8.85
ϵ_A	8.8ϵ
ϵ_G	8.9ϵ

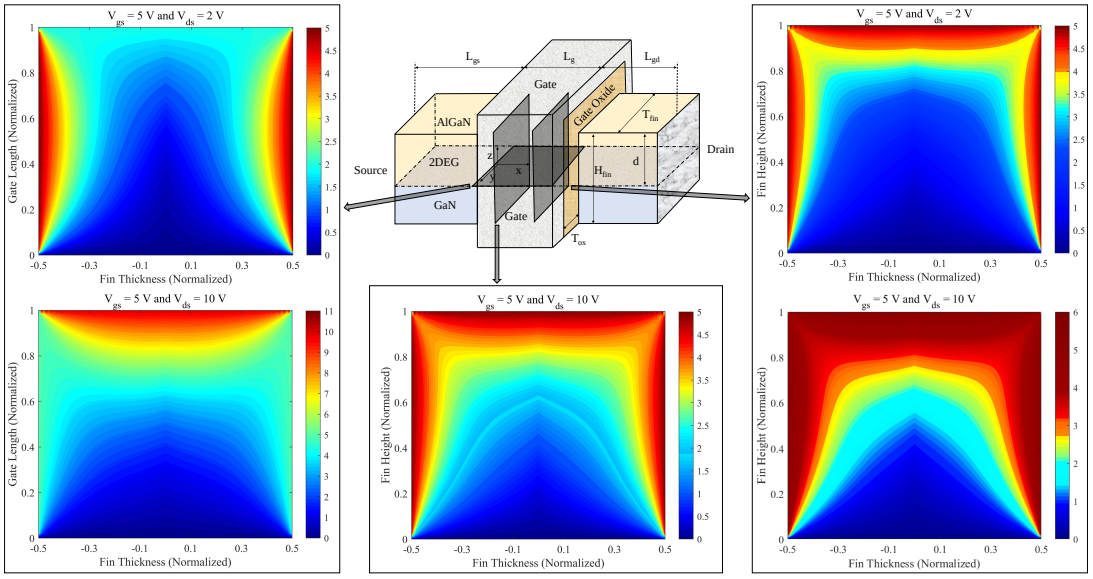

FIGURE 3.5: Potential profile at various points of an AlGaN/GaN FinFET (Device T_1).

the device operates in the depletion mode, where 2DEG is the main contributor towards the current flowing through the channel, and Eqs. (3.38), (3.46) and (3.47) describe the relationship between the 2DEG current and the applied voltages. Eq. (3.38) describes the linear region current; whereas, Eq. (3.47) represents the saturation current. To evaluate the switching point between the two, Eq. (3.46) is used which provides the value of V_{ds}, after which the channel of the device saturates for a given V_{gs}.

At $V_{gs} = V_{fb}$, 2DEG is completely un-depleted and this defines the upper limit of conventional HEMT devices' drain current. This is because a further increase in V_{gs} will exponentially increase gate leakage and the gate will cease to have any control on the device. However, due to the presence of the oxide layer in AlGaN/GaN FinFETs, gate leakage is minimized above $V_{gs} > V_{fb}$. Consequently, inversion occurs in the GaN layer and the device begins to operate as a regular GaN MOSFET.

In the proposed model, inversion current is given by Eq. (3.83), wherein β is a function of the applied potentials (V_{gs}, V_{ds}) of the device. In this manner, using both the depletion and inversion parts of the model simultaneously, the $I - V$

characteristics of an AlGaN/GaN FinFET can be assessed for a wider range of applied V_{gs}.

The presented model is applied on the devices given in Table 3.1 while the model parameters are optimized using a cost function defined by the following equation [2].

$$\text{RMSE} = \sqrt{\sum_{Q=1}^{N}\left\{\sum_{P=1}^{M}\left(I_{ds(\text{exp})}^{P,Q} - I_{ds(\text{mod})}^{P,Q}\right)^2 \Big/ \sum_{P=1}^{M} I_{ds(\text{exp})}^{P,Q}\right\}} \leq E_{r(min)} \tag{3.84}$$

Here, $I_{ds(\text{exp})}$ is the observed while $I_{ds(\text{mod})}$ is the modeled drain currents. $E_{r(min)}$ is the minimum error value, and the variables P, Q represent variation in the drain and gate voltages, respectively.

Fig. 3.6 (a), (b) and (c) are plotted to show the results of the proposed model in comparison with experimental data. It is pertinent to mention that the devices presented in Table 3.1 are evaluated for both positive and negative values of V_{gs} in order to ensure their operation in both depletion and inversion modes. Examining Fig. 3.6, it is apparent that the proposed model demonstrates reasonable accuracy in predicting $I-V$ characteristics of the chosen devices across the applied V_{gs} and V_{ds}.

The experimental and modeled output conductance of the chosen devices is shown in Fig. 3.7. The modeled characteristics follow the experimental data reasonably well which, once again, speaks that the proposed model couples the depletion and inversion operation of the selected devices with a good degree of accuracy.

To further investigate the effect of inversion on AlGaN/GaN FinFETs, Fig. 3.8 is plotted. Fig. 3.8(a) and (b) exhibit multiple peaks in the transconductance characteristics which is not a usual response of FETs. It is assumed that 2DEG and inversion currents are coming into action independently; which could possibly cause generation of multiple peaks in the device transfer characteristics. A plausible explanation could be that for long channel devices (T_1&T_2), the first

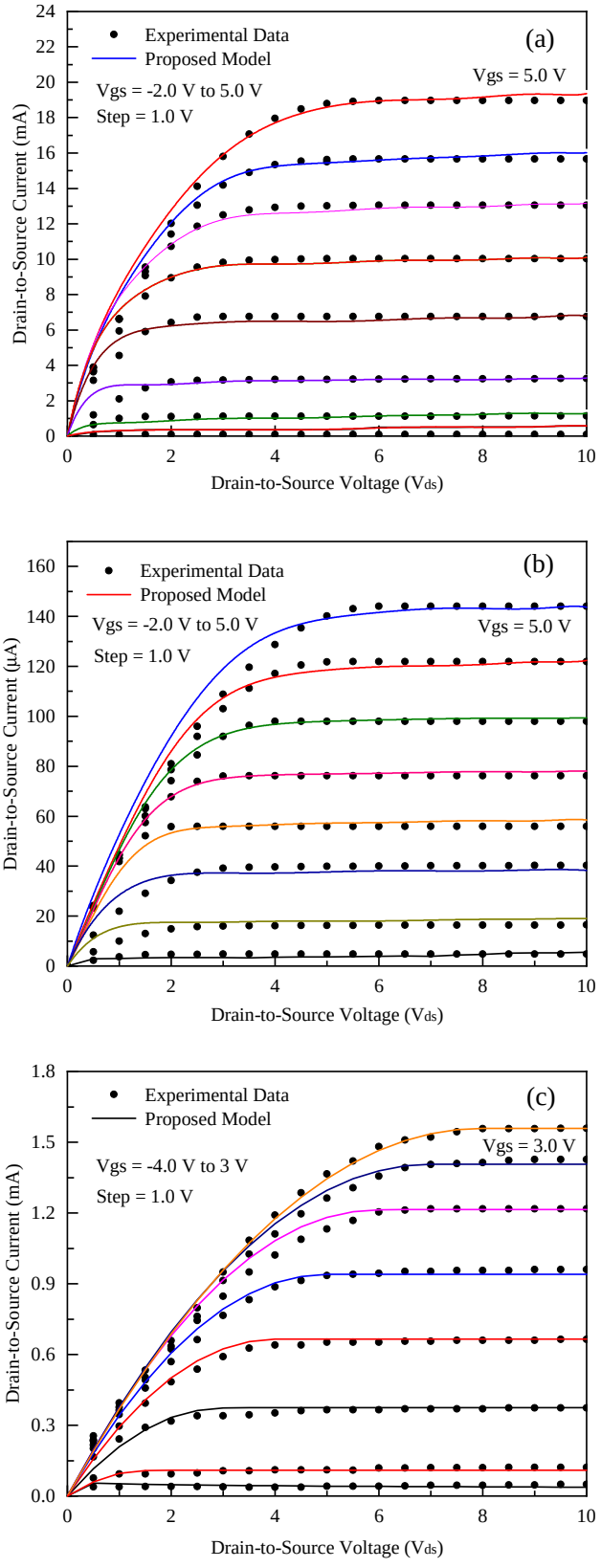

FIGURE 3.6: Modeled and experimental drain current of AlGaN/GaN FinFETs of Table 3.1: (a) T_1 (b) T_2 (c) T_3. Operation of the devices at high V_{gs} indicates the formation of inversion layer and its subsequent contribution in the drain current.

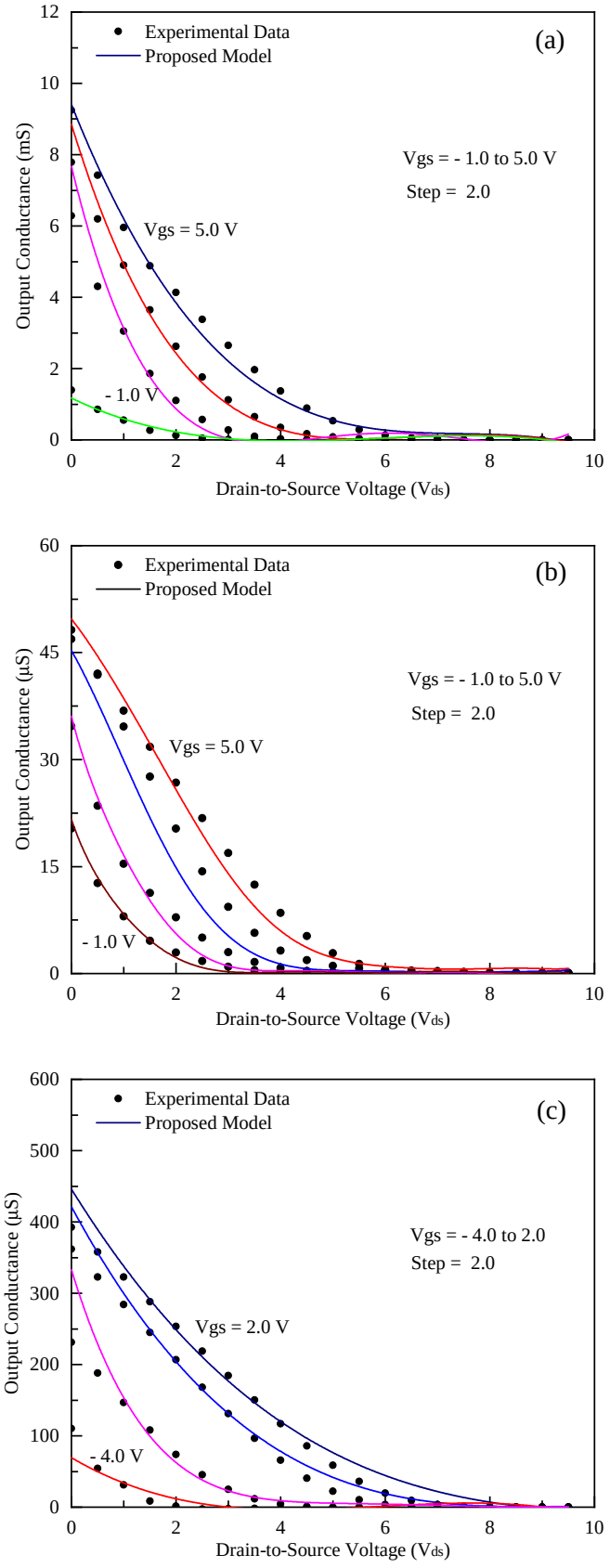

FIGURE 3.7: Modeled and experimental output conductance of AlGaN/GaN FinFETs described in Table 3.1: (a) T_1 (b) T_2 (c) T_3.

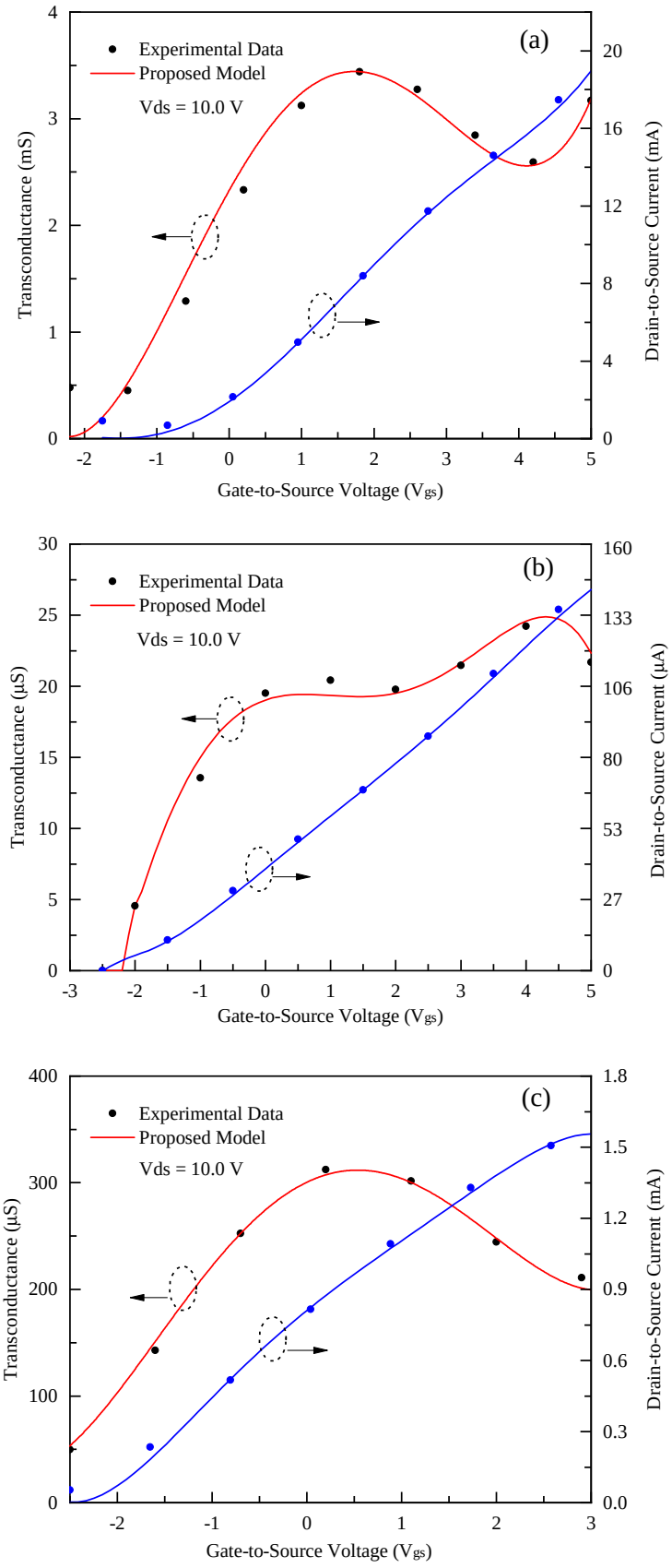

FIGURE 3.8: Transconductance and drain current versus gate voltage of AlGaN/GaN FinFETs: device (a) T_1 (b) T_2 (c) T_3.

peak is associated with 2DEG current wherein the the transconductance, g_m peak decreases under relatively high negative gate biases because of the usual nonlinear behavior of the depletion under the applied gate bias. On the other hand, at a relatively higher positive gate bias, I_{inv} also starts contributing to I_{ds} and g_m begins to rise once again, causing another peak in the transfer characteristics of the device. In the case of Fig. 3.8(c), the device has $L_g = 100$ nm, which is significantly lower than the other two devices that did not exhibit multiple peaks; possibly due to the dominant fringing gate field which is routinely observed in short channel FETs.

The plots of Fig. 3.8 demonstrate that the proposed model follows the rise and fall in g_m with relative ease; further confirming its position as a comprehensive model to predict DC characteristics of AlGaN/GaN FinFETs for both depletion and inversion mode of operations. It may be noted that the proposed model is a steady-state model and hence does not predict AC response of the device. Furthermore, it deals with the device under its usual operation and does not predict the device response in break down or sub-threshold regimes. The model could further be extended to evaluate the response of the device at elevated temperatures.

3.4 Summary

In this chapter, an $I-V$ model for trigate AlGaN/GaN FinFET is presented which is capable of predicting the DC characteristics of the device in both depletion and inversion mode of operations. The model is validated using experimental data wherein it showed reasonable accuracy. The model is divided into two parts: the depletion and inversion parts. The depletion part of the model assesses current using the modified definition of 2DEG carrier concentration, n_s, by accommodating the effects of the trigate nature of the device. The inversion part of the model uses Poisson distribution to evaluate the channel potential which is then translated into channel current. The total drain to source current, I_{ds}, is the addition of both the currents predicted by the depletion and inversion parts of the model.

It is shown that 2DEG current is the main contributor to I_{ds} for the gate bias $V_{th} \leq V_{gs} \leq V_{fb}$, whilst a further increase in V_{gs} potential beyond V_{fb} will generate an additional component of the current due to the inversion of carriers generated by the two side gates of AlGaN/GaN FinFETs.

Chapter 4

A Schrödinger-Poisson Model for Output Characteristics of Trigate Ballistic Si FinFETs

4.1 Introduction

To cope with the ever growing demands of the electronic industry, FET shrinkage was successfully carried out up to 100 nm but further down scaling was halted due to rise of adverse effects, such as high leakage current, high power dissipation, increased sub threshold swing and hot carriers injection [16, 132]. Therefore, in recent era, nanoscale technology has become a topic of great interest for researchers working to improve the performance of FETs with reduced dimensions [133]. One of the most promising candidates for reducing short channel effects are fin field effect transistors (FinFETs) [59]. Due to their very design, FinFETs exhibit more control upon the channel characteristics and thus open doors for further device scaling [62]. FinFETs offer promising characteristics both at low power to allow further device concentration per unit area, and at a high frequency [134–136] to accommodate the ever expanding communication needs.

Apart from the dynamic $I-V$ characteristics models [137], there are several DC models to represent charge transport in electronic devices which include Boltazman transport, hydrodynamic transport and drift-diffusion transport models [138]. However, short channel devices having L_g below 10 nm, there is significant tunneling between source and drain and the dual nature of particles becomes prominent [139]. The particles in such devices begin to behave as waves governed by the Schrödinger wave equation [140]. In recent years, several quantum models have been reported for such devices in literature which aim to investigate the effects of quantum mechanical transport on the device characteristics [19, 88, 91]. These models apply techniques such as non-equilibrium green function (NEGF) to assess quantum mechanical effects in nano devices [86, 89, 141–143].

Venugopala *et al.* developed a computational technique [142] to assess drain current of nanoscale FETs using a two dimensional quantum-mechanical ballistic model wherein the main consideration was carriers scattering while traveling from source to drain electrodes. With this technique, authors demonstrated that carriers of devices with ballistic transport experience less scattering thus offering current density of relatively higher magnitude. On the other hand, a 3D ballistic transport model, by considering electron-phonon interaction, was developed by Jin *et al.* using an NEGF [144]. They formulated their model using a 15 nm long nanowire FET and presented simulation results without any experimental validation. Their work demonstrated that electron-phonon scattering did have a tangible impact on the device characteristics. The simulated data exhibited a significant reduction in drain current (from 16 μA to 10 μA) when electron-phonon scattering was taken into consideration.

To solve NEGF, a real space method is considered an appropriate approach; however, it is computational extensive and for nanoscale devices, it is reported that coupled mode approach is efficient and accurate enough to predict quantum transport in nano FETs [84, 145]. In most of the NEGF formalism, the nano FETs characteristics were simulated to demonstrate the validity of the developed techniques; however, the attained characteristics were not compared with experimental data to ensure the applicability of these models [84, 144].

In this part of the research, we have developed a Schrödinger-Poisson model capable of predicting the output characteristics of Si trigate FinFETs by involving quantum-mechanical ballistic transport. In the proposed model, a 3D NEGF along with Poisson equation is solved, which predicts the difference of Fermi energies of the drain and source contacts and hence the flow of electrons. The model is compared with a 2D quantum model [146] and also validated against experimental data. The model shows great promise in predicting the device output and transfer characteristics with a high degree of accuracy. According to our conservative

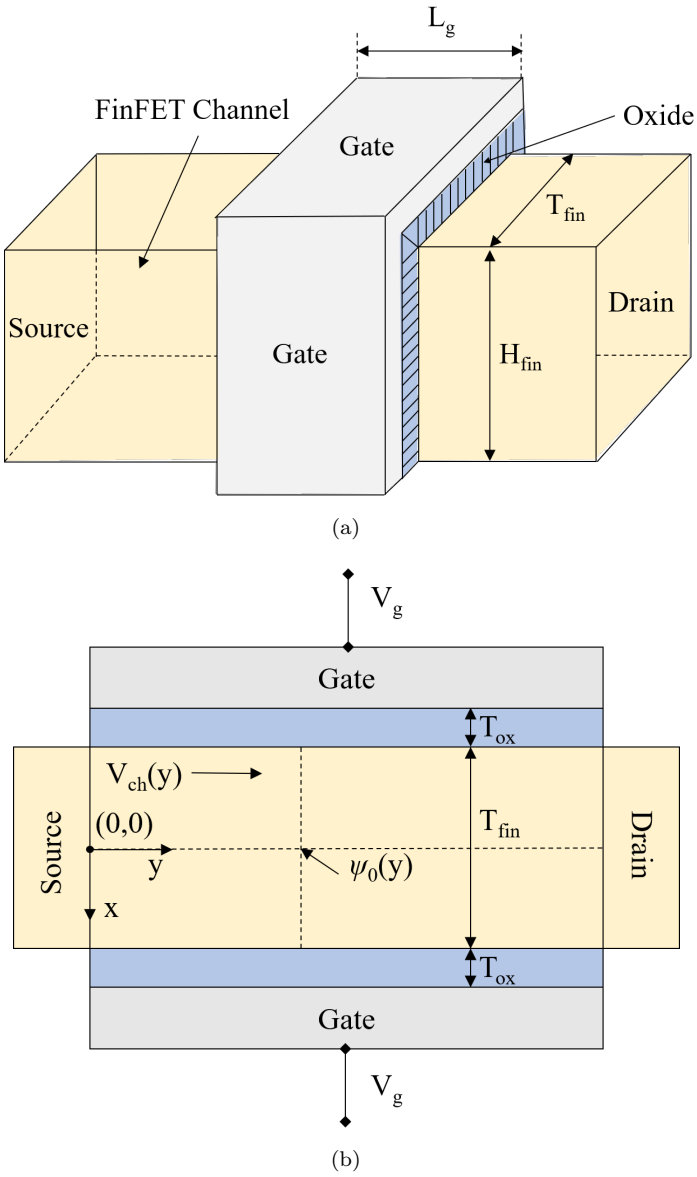

FIGURE 4.1: a) Channel of a trigate FinFET, b) $x-y$ crossection of a trigate FinFET.

estimate, no such comprehensive data is reported in literature where experimental verification of a NEGF for nanoscale FinFETs is performed.

4.2 Model Development

The proposed model is developed using a representative geometry of a FinFET as illustrated in Fig. 4.1, This structure presents a n-type depletion mode FinFETs. A 3D view of the channel is shown in Fig. 4.1 (a) while Fig. 4.1 (b) shows the 2D $x-y$ crossection. Metal gate is placed on the channel using oxide layer having thickness T_{ox}. The channel thickness as defined by Si is T_{fin}, whereas its height is H_{fin} as shown in Fig. 4.1 (a). Under biased conditions, the source is connected to the ground and the drain to $V_d > 0$, which generates a potential in the channel represented by $V_{ch}(y)$. Potential at the middle of the channel is represented by $\psi_0(y)$ which is independent of x. It is assumed that the current flow is ballistic i.e., $Lg << l$ where l is the mean free path, and only the conduction band electrons contribute towards the current flow. Also, there is no inter-valley mixing of carriers involved in the conduction. It is also assumed that there is no scattering at drain and source contacts and the variation in potential is slow, such that the system attains steady state at each bias point. Poisson and Schrödinger equations are solved to predict the output characteristics of trigate FinFETs and the details of which are explained below.

4.2.1 Schrödinger Equation

The fundamental equation that governs the model is the time-dependent Schrödinger equation which is given as [140]

$$j\hbar\frac{\partial \boldsymbol{\psi}}{\partial t} = \left(-\frac{\hbar^2}{2m}\Delta + \mathbf{V}\right)\boldsymbol{\psi} \tag{4.1}$$

In Eq. (4.1), Δ is the Laplacian operator and its dimensionality depends upon the application of the equation and $\mathbf{V}$ is the potential energy. Assuming that in

FinFET channel, electrons behave as they would in vacuum, but with a different mass referred to as effective mass, m^*. For such a system, Eq. (4.1) can be written as

$$j\hbar\frac{\partial \boldsymbol{\psi}}{\partial t} = \left(-\frac{\hbar^2}{2m^*}\Delta + \mathbf{U}\right)\boldsymbol{\psi} \tag{4.2}$$

Considering that the system in which Eq. (4.2) shall be applied is time independent, and for such a system the equation reduces to

$$\left(-\frac{\hbar^2}{2m^*}\Delta + \mathbf{U}\right)\boldsymbol{\psi} = \mathbf{E}\boldsymbol{\psi} \tag{4.3}$$

which can be written as

$$\mathbf{H}\boldsymbol{\psi} = \mathbf{E}\boldsymbol{\psi} \tag{4.4}$$

where,

$$\mathbf{H} = \left(-\frac{\hbar^2}{2m^*}\Delta + \mathbf{U}\right) \tag{4.5}$$

The analytical solution of Eq. (4.4) is impractical as the solution changes due to its dependence upon channel potential energy, $\mathbf{U}$. The magnitude of $\mathbf{U}$ can be determined by the charge distribution inside a FinFET channel. Such a charge distribution can be statistically assessed by Fermi dirac distribution function. Thus, this distribution shall be dependent upon the external gate and drain applied potential, which shall be determined in the later part of the developed model. One of the possible ways of addressing this issue is to solve the equation numerically. Apply a finite difference method [147], a 3D representation of Eq. (4.4) can be

$$\mathbf{E}\boldsymbol{\psi}_{xyz} = \mathbf{H}\boldsymbol{\psi}_{xyz} = \left[-\frac{\hbar^2}{2m^*}\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}\right) + \mathbf{U}\right]\boldsymbol{\psi}_{xyz} \tag{4.6}$$

Considering solution

$$\boldsymbol{\psi}_{xyz} = \psi_o e^{jk_x xa + jk_y ya + jk_z za} \tag{4.7}$$

By assuming that there is no variation in the channel material and the wave function does not penetrate into the oxide layer, one can, by considering nearest

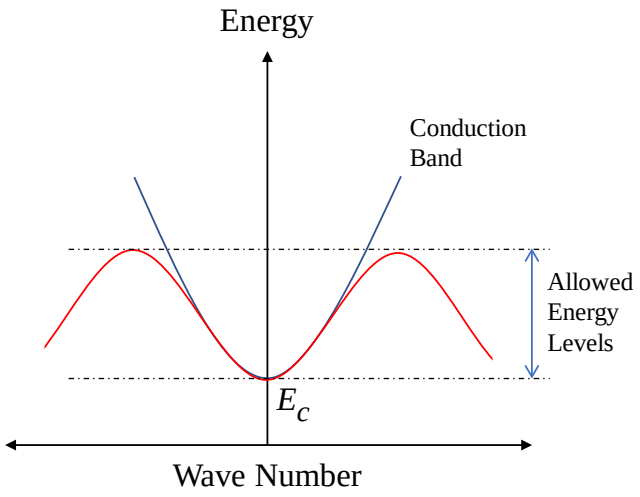

FIGURE 4.2: Allowed energy levels in the conduction band of a FinFET.

neighbors, substitute Eq. (4.7) in Eq. (4.6) to have

$$(\mathbf{E}-\mathbf{U})\psi_{xyz} = \epsilon\boldsymbol{\psi}_{xyz} + t_o(-\boldsymbol{\psi}_{x-1yz} - \boldsymbol{\psi}_{x+1yz} - \boldsymbol{\psi}_{xy-1z} - \boldsymbol{\psi}_{xy+1z} - \boldsymbol{\psi}_{xyz+1} - \boldsymbol{\psi}_{xyz-1}) \tag{4.8}$$

where, $\epsilon = E_c + 6t_o$ and

$$t_o = \frac{\hbar^2}{2m^* a^2} \tag{4.9}$$

Combining Eq. (4.7) and Eq. (4.8), we get

$$\mathbf{E} = \epsilon - 2t_o\cos(k_x a) - 2t_o\cos(k_y a) - 2t_o\cos(k_z a) + \mathbf{U} \tag{4.10}$$

Eq. (4.10) governs the energies of the conduction band. Only those energies are allowed which satisfy the equation. The conduction band of a biased FinFET is modeled by a shifted flipped cosine wave as shown in Fig. 4.2. Considering the channel with equidistant lattice, the Hamilton operator ($\mathbf{H}$) can be discretized using finite difference method which allows Eq. (4.6) in matrix form as

$$\mathbf{E}\boldsymbol{\psi} = \begin{bmatrix} \mathbf{A_1} & \mathbf{A_2} & \mathbf{A_2} & 0 & 0 & \dots & 0 \\ \mathbf{A_2} & \mathbf{A_1} & \mathbf{A_2} & \mathbf{A_2} & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \ddots & 0 \\ 0 & \ddots & 0 & \mathbf{A_2} & \mathbf{A_2} & \mathbf{A_1} & \mathbf{A_2} \\ 0 & 0 & \ddots & 0 & \mathbf{A_2} & \mathbf{A_2} & \mathbf{A_1} \end{bmatrix} \boldsymbol{\psi} \tag{4.11}$$

where $\mathbf{A_1}$ and $\mathbf{A_2}$ are given as,

$$\mathbf{A_1} = \begin{bmatrix} \epsilon & -t_o & 0 & \dots & 0 \\ -t_o & \epsilon & -t_o & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & 0 & -t_o & \epsilon & -t_o \\ 0 & 0 & 0 & -t_o & \epsilon \end{bmatrix} \tag{4.12}$$

$$\mathbf{A_2} = \begin{bmatrix} -t_o & 0 & 0 & \dots & 0 \\ 0 & -t_o & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & 0 & 0 & -t_o & 0 \\ 0 & 0 & 0 & 0 & -t_o \end{bmatrix} \tag{4.13}$$

The Hamiltonian matrix defined in Eq. 4.11 consists of diagonal and off-diagonal terms. In the grid, each diagonal element corresponds to a specific point and coupling between the points is represented by off-diagonal elements. Combined definition of Hamiltonian with ohmic contacts is an eigenvalue problem in quantum mechanics. Solving such a problem, the device eigenstates and eigenvalues are determined when isolated from the outside world, i.e., when the system is closed. To model electron transport, an effective mass Hamiltonian is used. The effective mass approximation is valid for the cases where potential relative to the atomic scale is changing slowly and the proposed model was developed under same constraints.

4.2.2 Current Equation

To find the current flow through the channel of a FinFET, consider Eq. (4.4) once again which describes the channel under the conditions when there is no in/out

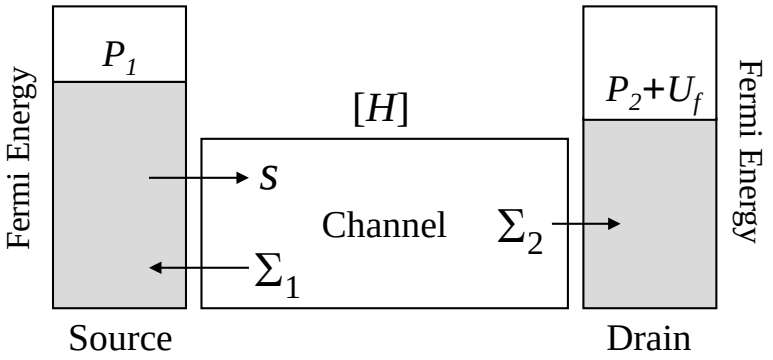

FIGURE 4.3: Inflow and outflow of charges in a FinFET channel.

flow of electrons. Thus, to describe the current flow, the same is modified as

$$\mathbf{E}\boldsymbol{\psi} = \mathbf{H}\boldsymbol{\psi} + \boldsymbol{\Sigma}\boldsymbol{\psi} + \mathbf{s} \tag{4.14}$$

where, $\boldsymbol{\Sigma}\boldsymbol{\psi}$ describes the outflow of electrons from the contacts. The $\boldsymbol{\Sigma} = \boldsymbol{\Sigma}_1 + \boldsymbol{\Sigma}_2$, represents source and drain energies, respectively, which are responsible for the outflow while $\mathbf{s}$ represents inflow as shown in Fig. 4.3. $\boldsymbol{\Sigma}$ can be found by finding eigenvalues and eigenvectors of $\mathbf{A_1}$. $\boldsymbol{\Sigma}$ can be written as

$$\boldsymbol{\Sigma} = \boldsymbol{\beta} \begin{bmatrix} \mathbf{A_3} & 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \mathbf{A_3} \end{bmatrix} \boldsymbol{\beta}^{+} \tag{4.15}$$

where, $\boldsymbol{\beta}$ is the eigenvector associated with $\mathbf{A_1}$ and $\boldsymbol{\beta}^{+}$ is its conjugate transpose;

$$\mathbf{A_3} = \begin{bmatrix} t_o e^{jk_1 a} & 0 & 0 & \dots & 0 \\ 0 & t_o e^{jk_2 a} & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & 0 & 0 & t_o e^{jk_{(n-1)} a} & 0 \\ 0 & 0 & 0 & 0 & t_o e^{jk_n a} \end{bmatrix} \tag{4.16}$$

where k_i can be found by solving the following equation;

$$\mathbf{E} = \lambda_i - 2t_o \cos(k_i a) \tag{4.17}$$

here, λ_i are the eignvalues of $\mathbf{A_1}$. Eq. (4.14) can be written as

$$\boldsymbol{\psi} = [\mathbf{EI} - \mathbf{H} - \mathbf{\Sigma}]^{-1}\mathbf{s} \tag{4.18}$$

As $\mathbf{E}$ is a column vector, in order to correct the dimensionality of Eq. (4.18), it is multiplied by $\mathbf{I}$, where $\mathbf{I}$ is an identity matrix. Let,

$$\mathbf{G^R} = [\mathbf{EI} - \mathbf{H} - \mathbf{\Sigma}]^{-1} \tag{4.19}$$

So,

$$\boldsymbol{\psi} = \mathbf{G^R s} \tag{4.20}$$

Now, taking the conjugate transpose (+) of Eq. (4.18) gives,

$$\boldsymbol{\psi}^+ = \mathbf{s}^+\mathbf{G^A} \tag{4.21}$$

where,

$$\mathbf{G^A} = \left[[\mathbf{EI} - \mathbf{H} - \mathbf{\Sigma}]^{-1}\right]^+ = [\mathbf{G^R}]^+ \tag{4.22}$$

The electron density matrix can be defined as

$$\mathbf{G^n} = 2\pi\boldsymbol{\psi}\boldsymbol{\psi}^+ \tag{4.23}$$

By combining Eqs. (4.20), (4.21) and (4.23)

$$\mathbf{G^n} = 2\pi\mathbf{G^R s s}^+\mathbf{G^A} \tag{4.24}$$

In Eq. (4.24), $\mathbf{G^n}$, $\mathbf{G^R}$ and $\mathbf{G^A}$ are functions of energy and have units eV^{-1} and $\mathbf{ss}^+$ defines the inflow of electrons, which can be written as

$$\mathbf{\Sigma^{in}} = 2\pi\mathbf{ss}^+ = \mathbf{\Gamma} \tag{4.25}$$

here, $\mathbf{\Sigma^{in}}$ represents the outflow of electrons. Eq. (4.25) is valid because for steady flow, current entering must be equal to current leaving. If there is one source of incoming electrons, and two outflow sources as shown in Fig. 4.3, one can write

$$\mathbf{\Sigma^{in}} = \mathbf{\Gamma}_1\mathbf{f_1}(\mathbf{E}) + \mathbf{\Gamma}_2\mathbf{f_2}(\mathbf{E}) \tag{4.26}$$

here,

$$\mathbf{\Gamma}_i = j[\mathbf{\Sigma}_i - \mathbf{\Sigma}_i^+] \tag{4.27}$$

$\mathbf{\Gamma}_i$ is the anti-Hermitian part of $\mathbf{\Sigma}_i$ and it describes the ease of communication between the channel and the contacts. $\mathbf{f_{1,2}}$ is expressed as [148],

$$\mathbf{f_{1,2}}(\mathbf{E}) = \frac{1}{1 + \exp\left[\dfrac{\mathbf{E} - (P_{1,2} + U_f)}{k_B T}\right]} \tag{4.28}$$

where

$$U_f = \alpha Q(V_g + V_d) \tag{4.29}$$

In Eq. (4.29), α is a fitting factor which incorporates contact resistance, Q is the total charge and is determined by solving a 3D Poisson equation which is discussed in the subsection to follow. To find channel current consider,

$$j\hbar\frac{d}{dt}\boldsymbol{\psi} = [\mathbf{H} + \mathbf{\Sigma}]\boldsymbol{\psi} + \mathbf{s} \tag{4.30}$$

thus,

$$j\hbar\frac{d}{dt}\boldsymbol{\psi}\boldsymbol{\psi}^+ = [(\mathbf{H} + \mathbf{\Sigma})\boldsymbol{\psi}\boldsymbol{\psi}^+ - \boldsymbol{\psi}\boldsymbol{\psi}^+(\mathbf{H} + \mathbf{\Sigma}^+)] + [\mathbf{s}\mathbf{s}^+\mathbf{G^A} - \mathbf{G^R}\mathbf{s}\mathbf{s}^+] \tag{4.31}$$

Eq. (4.31) is obtained using the chain rule for derivatives on Eq (4.30) and making use of Eqs. (4.20) and (4.21). The number of electrons can be obtained by Trace$[\boldsymbol{\psi}\boldsymbol{\psi}^+]$ which represents the sum of all elements on the main diagonal. Substituting Eqs. (4.23) and (4.25) in Eq. (4.31), one gets

$$\frac{d}{dt}\boldsymbol{\psi}\boldsymbol{\psi}^+ = \frac{[\mathbf{H}\mathbf{G^n} - \mathbf{G^n}\mathbf{H}] + [\mathbf{\Sigma}\mathbf{G^n} - \mathbf{G^n}\mathbf{\Sigma}^+] + [\mathbf{\Sigma^{in}}\mathbf{G^A} - \mathbf{G^R}\mathbf{\Sigma^{in}}]}{j2\pi\hbar} \tag{4.32}$$

As Trace$[AB]$ = Trace$[BA]$ and $h = 2\pi\hbar$, therefore

$$\text{Trace}\left(\frac{d}{dt}\psi\psi^{+}\right) = \frac{-i}{h}\text{Trace}\left([\Sigma G^{n} - G^{n}\Sigma^{+}] + [\Sigma^{in}G^{A} - G^{R}\Sigma^{in}]\right) \tag{4.33}$$

By using Eq. (4.27)

$$\text{Trace}\left(\frac{d}{dt}\psi\psi^{+}\right) = \frac{-i}{h}\text{Trace}\left(-i\Gamma G^{n} + \Sigma^{in}[G^{A} - G^{R}]\right) \tag{4.34}$$

To find $G^{A} - G^{R}$ using Eqs. (4.19), (4.22) and (4.27),

$$G^{A} - G^{R} = iG^{R}\Gamma G^{A} \tag{4.35}$$

Now, Eq. (4.34) becomes

$$\text{Trace}\left(\frac{d}{dt}\psi\psi^{+}\right) = \frac{1}{h}\text{Trace}\left(\Sigma^{in}G^{R}\Gamma G^{A} - \Gamma G^{n}\right) \tag{4.36}$$

To find electronic current per unit energy through a contact, multiply Eq. (4.32) with electronic charge, q

$$I_{m} = \text{Trace}\left(q\frac{d}{dt}\boldsymbol{\psi}\boldsymbol{\psi}^{+}\right) = \frac{q}{h}\text{Trace}\left(\mathbf{\Sigma_{m}^{in}G^{R}\Gamma G^{A} - \Gamma_{m}G^{n}}\right) \tag{4.37}$$

Current through one of the contacts of the device is given as,

$$I_{1} = \frac{q}{h}\text{Trace}\left[\mathbf{\Gamma}_{1}\left(\mathbf{f_{1}G^{R}\Gamma G^{A} - G^{n}}\right)\right] \tag{4.38}$$

where, $\mathbf{\Sigma_{1}^{in}} = \mathbf{\Gamma}_{1}\mathbf{f_{1}}$.

Since there are two contacts, drain and source, so $\mathbf{\Gamma} = \mathbf{\Gamma}_{1} + \mathbf{\Gamma}_{2}$. Also using Eq. (4.24) we get

$$I_{1} = \frac{q}{h}\text{Trace}\left[\Gamma_{1}\left(f_{1}G^{R}\{\Gamma_{1} + \Gamma_{2}\}G^{A} - G^{R}\{\Gamma_{1}f_{1} + \Gamma_{2}f_{2}\}G^{A}\right)\right] \tag{4.39}$$

So,

$$I_{1} = \frac{q}{h}\text{Trace}\left[\mathbf{\Gamma}_{1}\mathbf{G^{R}\Gamma}_{2}\mathbf{G^{A}}\right]\left(\mathbf{f_{1} - f_{2}}\right) \tag{4.40}$$

Now, the total current is

$$I_{ds} = \int_{-\infty}^{+\infty} \frac{q}{h} \text{Trace} \left[\mathbf{\Gamma}_1 \mathbf{G}^{\mathbf{R}} \mathbf{\Gamma}_2 \mathbf{G}^{\mathbf{A}} \right] (\mathbf{f_1} - \mathbf{f_2}) \, dE \tag{4.41}$$

The above equation represents $I_{ds}(V_{ds}, V_{gs})$ characteristics of a FinFET wherein, quantum-mechanical ballistic transport of the carriers is considered. It is pertinent to mention that current saturation in short channel FETs is usually attributed to the velocity saturation of carriers. However, no term representing the velocity is involved in the above expression; thus, the only possibility which could be associated with current saturation in quantum-mechanical transport would be the saturation of carrier supply from the source reservoir.

4.2.3 Poisson Equation

To find Q appearing in Eq. (4.29), a 3D Poisson equation is applied on the channel shown in Fig. 4.1b. The equation includes both inversion and bulk carriers and can be written as

$$\frac{\partial^2 \psi_p}{\partial x^2} + \frac{\partial^2 \psi_p}{\partial y^2} + \frac{\partial^2 \psi_p}{\partial z^2} = \frac{q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_p + \phi_B - V_{ch}}{V_T} \right) + \frac{q N_d}{\epsilon_{si}} \tag{4.42}$$

where,

$$\phi_B = V_T \ln\left(\frac{N_d}{n_i} \right) \tag{4.43}$$

and

$$V_T = \frac{k_B T}{q} \tag{4.44}$$

where V_{ch} varies as a function of L_g and towards the source side $V_{ch}(0) = V_s$ and $V_{ch}(L_g) = V_d$. Dividing the solution into parts i.e., ψ_{p1} and ψ_{p2}, such that $\psi_p = \psi_{p1} + \psi_{p2}$. Considering,

$$\frac{\partial^2 \psi_{p1}}{\partial x^2} = \frac{q n_i}{\epsilon_{si}} \exp\left(\frac{\psi_{p1} + \phi_B - V_{ch}}{V_T} \right) + \frac{q N_d}{\epsilon_{si}} \tag{4.45}$$

Integrating Eq. (4.45) twice and applying boundary conditions

$$\left.\frac{\partial^2\psi_{p1}}{\partial x^2}\right|_{x=0} = 0 \qquad \text{and} \qquad \psi_{p1}(x=0,y) = \psi_0(y) \tag{4.46}$$

Poisson equation contain bulk and inversion carriers such that the solution ψ_{p1}

$$\psi_{p1} = \psi_1 + \psi_2 \tag{4.47}$$

Here, ψ_2 represents bulk carriers and ψ_1 is the potential due to inversion of carriers, which can be written as

$$\frac{\partial^2\psi_1}{\partial x^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right) \tag{4.48}$$

Integrating Eq. (4.48),

$$\left(\frac{d\psi_1}{dx}\right)^2 = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right) + c \tag{4.49}$$

Using boundary condition, the above equation becomes

$$\frac{d\psi_1}{dx} = \sqrt{\frac{V_T q n_i}{\epsilon_{si}}\left[\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right) - \exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_T}\right)\right]} \tag{4.50}$$

$$\int \frac{\partial\psi_1}{\sqrt{\frac{V_T q n_i}{\epsilon_{si}}\left[\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right) - \exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_T}\right)\right]}} = \int \partial x \tag{4.51}$$

Further simplification yields

$$\int \frac{\partial\psi_1}{\left(\left[\sqrt{\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right)}\right]^2 - \left[\sqrt{\exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_T}\right)}\right]^2\right)^{1/2}} \tag{4.52}$$

$$= x\sqrt{\frac{V_T q n_i}{\epsilon_{si}}}$$

To simplfiy the above equation further, let

$$\sqrt{\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right)} = b\sec\theta \tag{4.53}$$

and

$$\sqrt{\exp\left(\frac{\psi_0 + \phi_B - V_{ch}}{V_T}\right)} = b \tag{4.54}$$

Partial differential of Eq. (4.53),

$$\begin{aligned}&\frac{1}{2}\left[\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right)\right]^{-1/2}\exp\left(\frac{\psi_1 + \phi_B - V_{ch}}{V_T}\right) \times \frac{\partial\psi_1}{V_T} \\ &= b\sec\theta\tan\theta\ \partial\theta\end{aligned} \tag{4.55}$$

Combining Eqs. (4.53), (4.54) and (4.55) reveals

$$\partial\psi_1 = 2V_T\tan\theta\ \partial\theta \tag{4.56}$$

Substituting Eqs. (4.53), (4.54) and (4.56) in Eq. (4.52)

$$x\sqrt{\frac{V_T q n_i}{\epsilon_{si}}} = \int \frac{2V_T\tan\theta}{\sqrt{b^2\sec^2\theta - b^2}}\partial\theta \tag{4.57}$$

as $b^2\sec^2\theta - b^2 = b^2\tan^2\theta$, so

$$x\sqrt{\frac{V_T q n_i}{\epsilon_{si}}} = \int \frac{2V_T\tan\theta}{b\tan\theta}\partial\theta = \frac{2V_T\theta}{b} + c_2 \tag{4.58}$$

Eqs. (4.53) and (4.54) can be used to generate the expression for θ

$$\sec^{-1}\left[\sqrt{\exp\left(\frac{\psi_1 - \psi_0}{V_T}\right)}\right] = \theta \tag{4.59}$$

consider $c_2 = 0$ and by rearranging Eq. (4.58), one gets

$$\sqrt{\frac{q n_i b^2}{V_T\epsilon_{si}}} \times \frac{x}{2} = \theta \tag{4.60}$$

Inserting the value of θ in Eq. (4.59)

$$\sqrt{\frac{qn_ib^2}{V_T\epsilon_{si}}} \times \frac{x}{2} = \sec^{-1}\left[\sqrt{\exp\left(\frac{\psi_1 - \psi_0}{V_T}\right)}\right] \tag{4.61}$$

Using $\cos(\sec^{-1}\theta) = 1/\theta$, above expression yields

$$\cos\left[\sqrt{\frac{qn_ib^2}{V_T\epsilon_{si}}} \times \frac{x}{2}\right]^2 = \exp\left(-\frac{\psi_1 - \psi_0}{V_T}\right) \tag{4.62}$$

Taking natural log of both the sides of Eq. (4.62) and using Eq. (4.44) reveals

$$\psi_1 = \psi_0 - \frac{2k_BT}{q}\ln\left[\cos\left(\sqrt{\frac{q^2n_i^2}{k_BTN_d\epsilon_{si}}\exp\left(\psi_0 - V_{ch}\right)} \times \frac{x}{2}\right)^2\right] \tag{4.63}$$

The potential caused by the inversion carriers is represented by Eq. (4.63). To assess the bulk carries potential contribution, consider

$$\frac{\partial^2\psi_2}{\partial x^2} = \frac{qN_d}{\epsilon_{si}} \tag{4.64}$$

Integrating Eq. (4.64) twice and using boundary conditions $\psi_2 = 0$ and $\partial\psi_2/\partial x|_{x=0} = 0$, one gets

$$\psi_2 = \frac{qN_dx^2}{2\epsilon_{si}} \tag{4.65}$$

The solution for ψ_{p1} as given in Eq. (4.47) becomes

$$\psi_{p1} = \psi_0(y) - \frac{2k_BT}{q}\ln\left[\cos\left(\sqrt{\frac{q^2n_i^2}{k_BTN_d\epsilon_{si}}\exp\left(\psi_0(y) - V_{ch}(y)\right)} \times \frac{x}{2}\right)^2\right] + \frac{qN_dx^2}{2\epsilon_{si}} \tag{4.66}$$

Also,

$$\frac{\partial^2\psi_{p2}}{\partial y^2} + \frac{\partial^2\psi_{p2}}{\partial z^2} = 0 \tag{4.67}$$

With boundary conditions $\psi_{p2}(y = 0, z) = V_s$, $\psi_{p2}(y = L_g, z) = V_d$, $\psi_{p2}(y, z = 0) = \psi_{p1}$, $\psi_{p2}(y, z = H_{fin}) = \phi_B$, and with $\eta = \pi/2L_g$, $\alpha_1 = \pi/2H_{fin}$, the solution

becomes

$$\frac{\partial^2 Y(y)Z(z)}{\partial y^2} = -\frac{\partial^2 Y(y)Z(z)}{\partial z^2} = -\alpha^2 \tag{4.68}$$

where, $\eta = \alpha^2 = \pi/(2L_g)$.

$$\frac{\partial^2 Y(y)}{\partial y^2} + \alpha^2 Y(y) = 0 \tag{4.69}$$

$$\frac{\partial^2 Z(z)}{\partial z^2} - \alpha^2 Z(z) = 0 \tag{4.70}$$

Solution of Eqs. (4.69) and (4.70) can be expressed as

$$Y(x, y, z) = c_3 \cos(\eta y) + c_4 \sin(\eta y) \tag{4.71}$$

$$Z(x, y, z) = c_5 \exp(-\eta z) + c_6 \exp(\eta z) \tag{4.72}$$

Using boundary conditions in Eq. (4.71) results,

$$Y(x, 0, \acute{z}) = c_3 = V_s \tag{4.73}$$

and

$$Y(x, L_g, \acute{z}) = c_4 = V_d \tag{4.74}$$

Combining Eqs. (4.71), (4.73) and (4.74)

$$Y(x, y, z') = V_s \cos(\eta y) + V_d \sin(\eta y) \tag{4.75}$$

Assuming $\acute{z} = (L_g/H_{fin})z$ and using the boundary condition in Eq. (4.72) yields,

$$Z(x, y, 0) = c_5 + c_6 = \psi_{p1} \tag{4.76}$$

and

$$Z(x, y, H_{fin}) = c_5 \exp(-\pi/2) + c_6 \exp(\pi/2) = \phi_B \tag{4.77}$$

Simplify Eqs. (4.76) and (4.77)

$$c_5 = \left(\psi_{p1} - \frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)}\right) \exp(-\alpha_1 \acute{z}) \tag{4.78}$$

and

$$c_6 = \frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)} \exp(\alpha_1 \acute{z}) \tag{4.79}$$

Substituting Eqs. (4.78) and (4.79) into Eq. (4.72) gives

$$\begin{aligned} Y(x, y, z') = &\left[\frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)} \exp(\alpha_1 \acute{z})\right. \\ &\left. + \left(\psi_{p1} - \frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)}\right) \exp(-\alpha_1 \acute{z})\right] \end{aligned} \tag{4.80}$$

The potential of Eqs. (4.75) and (4.80) is

$$\begin{aligned} \psi_{p2} = &[V_s \cos(\eta y) + V_d \sin(\eta y)] \times \left[\frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)} \exp(\alpha_1 \acute{z})\right. \\ &\left. + \left(\psi_{p1} - \frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)}\right) \exp(-\alpha_1 \acute{z})\right] \end{aligned} \tag{4.81}$$

here, $\acute{z} = (L_g/H_{fin})z$.

Combining Eqs. (4.81) and (4.66), the total potential becomes

$$\begin{aligned} \psi_p = &\psi_{p1} + [V_s \cos(\eta y) + V_d \sin(\eta y)] \left[\frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)} \exp(\alpha_1 \acute{z})\right. \\ &\left. + \left(\psi_{p1} - \frac{\phi_B - \exp(-\pi/2)\psi_{p1}}{\exp(\pi/2) - \exp(-\pi/2)}\right) \exp(-\alpha_1 \acute{z})\right] \end{aligned} \tag{4.82}$$

$\psi_0(y)$ is found by using Gauss's law applied on the channel

$$V_g = V_{fb} + \psi_p + \frac{\epsilon_{si}}{C_{ox}} \frac{\partial \psi_p}{\partial x}. \tag{4.83}$$

where V_{fb} is flat band voltage.

Combining Eqns. (4.66), (4.82) and (4.83), $\psi_0(y)$ can be evaluated iteratively. Finally, Q is obtained by

$$Q = C_{ox}(V_g - V_{fb} - \psi_p) \tag{4.84}$$

TABLE 4.1: Physical parameters of different devices used in this study.

Parameters	T_1 [104]	T_2 [98]	T_3 [149]	T_4 [98]
L_g (nm)	25	40	45	60
T_{fin} (nm)	3	20	30	35
H_{fin} (nm)	50	20	100	65
T_{ox} (nm)	1.5	1.0	2.0	1.7
N_d (m^{-3})	5.0×10^{20}	1.14×10^{16}	1.0×10^{24}	1.0×10^{21}
V_{fb} (V)	-1.1	-0.9	-0.93	-0.9

TABLE 4.2: Physical constants used in this study.

Parameters	**Value**
n_i ($\times$ 10^{16} m^{-3})	1
k_B ($\times$ 10^{-23}J.K^{-1})	1.38
T (K)	300
q ($\times$ 10^{-19} C)	1.6
ϵ ($\times$ 10^{-12} Fm^{-1})	8.85
ϵ_{si}	11.68ϵ
ϵ_{ox}	3.9ϵ

4.3 Results and Discussion

To calibrate and assess the validity of the proposed model, different devices of varying dimensions are selected, the details of which are given in Table 4.1. Transistor T_1 and T_2 are perceived using TCAD; whereas, T_3 and T_4 are fabricated devices and their fabrication details are given in [98, 149]. Devices T_1 and T_2 can also be materialized using a standard fabrication process involving: a) chip cleaning; b) mesa isolation; c) fin definition using lithographic process and etching; d) drain-source contacts formation using ohmic metal evaporation and lift-off; e) gate oxide and f) Schottky metal deposition using lithography and lift-off.

The proposed model also has physical parameters which are used to determine the output characteristics of trigate rectangular Si FinFETs and the same are given in Table 4.2. The devices mentioned in Table 4.1 are a mixture of actual and TCAD simulated devices which will provide a challenge for the proposed model in

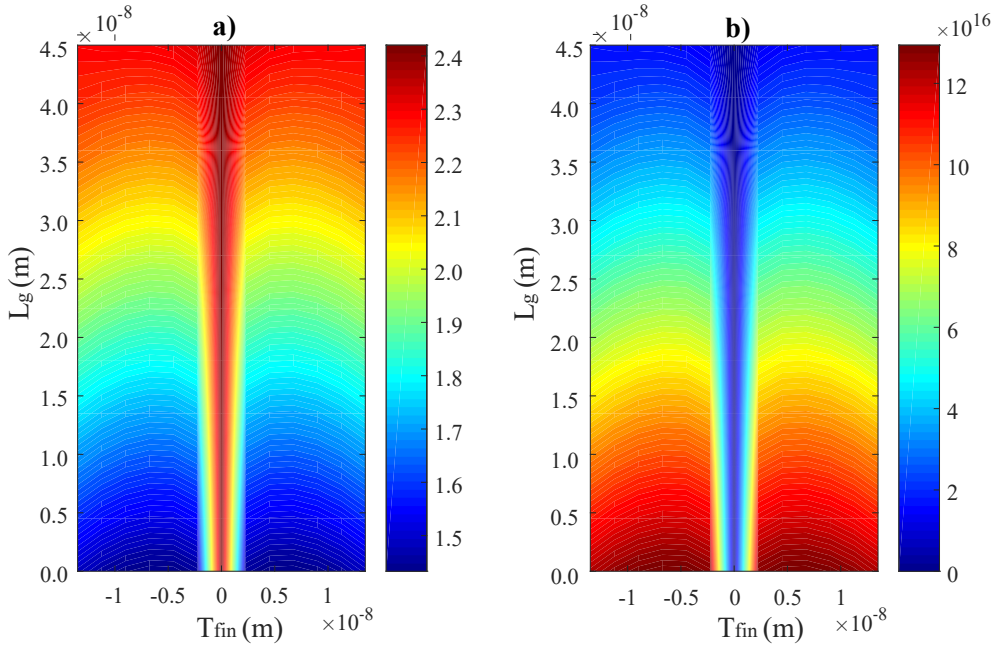

FIGURE 4.4: a) Variation in the channel potential predicted by the proposed model. b) Charge distribution inside the channel of a trigate FinFET. The simulations are at $V_{ds} = 1$ V and $V_{gs} = 1.5$ V using the physical dimensions of the device T_3.

determining its accuracy across devices of various dimensions. TCAD is used to design, examine, and simulate the structure of devices. The simulation of device characteristics consists of two steps: a) structure creation and b) selection of a numerical model. The structure creation includes the definition of mesh, identification of various regions of the device, its electrodes and doping concentration of active layers involved in the definition of the device. While in the selection of a numerical model, one requires the definition of gate work function, choice of a physical model and mathematical method to be engaged by the simulator. Finally, by engaging all above mentioned features, TCAD will generate $I - V$ characteristics of the device under consideration. Eq. (4.41) can be employed to plot the output characteristics of Si trigate FinFETs. To understand the workings of Eq. (4.41), one should keep in mind that the characteristics of the FinFET channel are determined by the Hamiltonian matrix given in Eq. (4.11). Moreover, the developed model is a nearest neighbor tight binding model which assumes that the channel characteristics at any point are only dependent upon its nearest neighbor in both x and y directions. This assumption eliminates the complexity of solving

the time-independent Schrödinger wave equation, as the wave function, $\boldsymbol{\psi}$, is only dependent upon its nearest neighbors as illustrated by Eq. (4.8).

The Hamiltonian matrix describes the channel properties when no bias is applied. To consider the effect of V_{ds} and V_{gs} on the FinFET energy levels, a modified time-independent Schrödinger wave equation is considered, as illustrated in Eq. (4.14). The terms $\boldsymbol{\Sigma\psi}$ and $\mathbf{s}$ depend upon the applied bias, as the inflow and outflow of electrons is dependent upon the difference of Fermi energy of the source and drain contacts. Using the channel surface potential given by Eq. (4.82), charge distribution inside the channel is evaluated and is shown by Fig. 4.4. Fig. 4.4 (a) shows the channel potential of the device T_3 at $V_{ds} = 1$ V and $V_{gs} = 1.5$ V. As observed from the figure, potential is maximum at $T_{fin} = 0$ nm, which is the mid point of channel thickness. This is due to the fact that the two side gates have the same voltages as illustrated by Fig. 4.1 (b). Fig. 4.4 (b) shows the charge distribution predicted by Eq. (4.84). Here, it can be observed that at the mid point of T_{fin}, electron concentration is minimum, whereas it increases at the edges

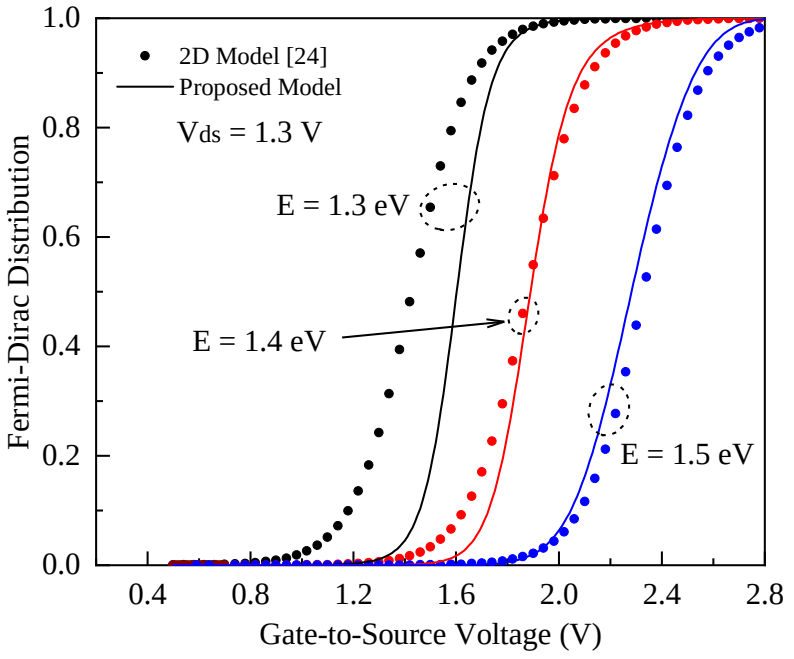

FIGURE 4.5: Fermi-Dirac distribution as a function of applied gate to source voltage, V_{gs} at different energy levels for device T_3.

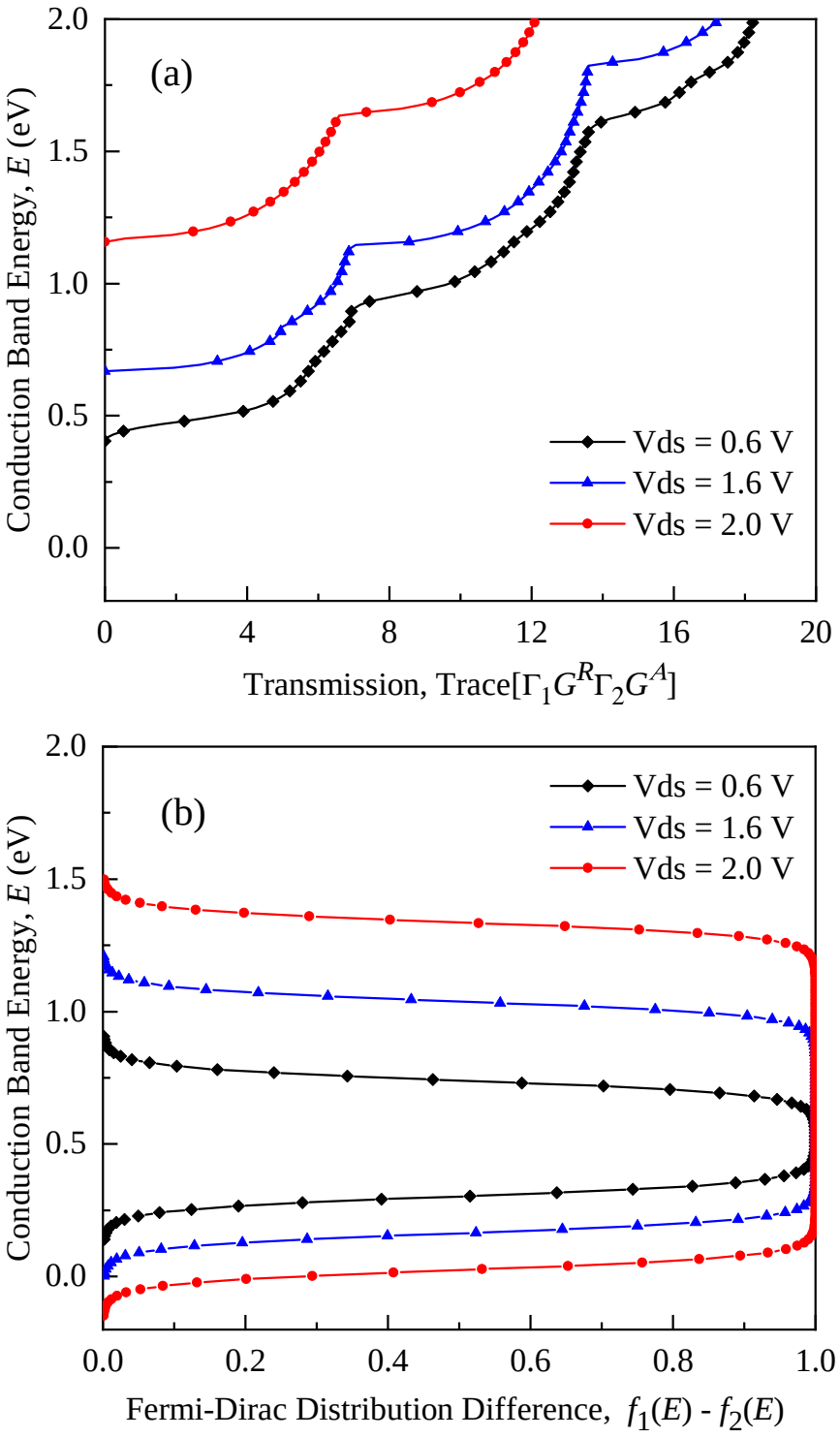

FIGURE 4.6: a) Channel transmission and b) difference in Fermi-Dirac distribution energies at V_{gs} = 2 V. The dimensions of the simulated device T_3 is provided in Table 4.1.

of T_{fin}. This can be explained by the inversion of carriers due to the applied V_{gs}, which causes a channel of electrons to formulate on the fringes of T_{fin}.

In the proposed model, Fermi-Dirac distribution is calculated using the solution of a 3D Poisson equation as given by Eq. (4.28). Fig. 4.5 shows the variation in Fermi-Dirac distribution as a function of V_{gs}. The Fermi function associated with the proposed model differs to that of the Fermi function evaluated by [8, 146] because the proposed model takes into account the charge distribution inside the channel of FinFETs using the solution of a 3D Poisson equation.

To evaluate the $I-V$characteristics of a trigate FinFET, Eq. (4.41) is used wherein ballistic transport is assumed thus, all the conduction band electrons from the source will flow towards the drain, provided that there is a difference in Fermi energies between the two respective contacts. Each energy level will provide current equivalent to hq^{-1} and the total current flowing through the channel is the summation of all the individual currents over the Fermi energy differences. The term Trace $\left[\mathbf{\Gamma}_1\mathbf{G}^{\mathbf{R}}\mathbf{\Gamma}_2\mathbf{G}^{\mathbf{A}}\right]$ represents the transmission of the electrons at any given energy level. Transmission is controlled by the applied V_{gs} and V_{ds} as shown by Fig. 4.6 (a). Fig. 4.6 (b) shows the Fermi energy difference at any given energy of the device T_3 at $V_{gs} = 2$ V. Examining Fig. 4.6 (a) and 4.6 (b) simultaneously, it can be observed that only those energy levels contribute towards the device current where the product of transmission and Fermi energy difference is greater than zero. The model is calibrated using TCAD simulations and Fig. 4.7 is plotted to show the ability of proposed model to predict $I-V$ characteristics of trigate FinFETs of varying dimensions. Fig. 4.8 shows the proposed model's performance against fabricated devices. In all reported cases, the model's performance is reasonable which is based on the evaluation of charges as a function of V_{ds} and V_{gs} followed by the device $I-V$ characteristics using Eq. (4.41). It is pertinent to mention that devices T_2, T_3 and T_4 are relatively larger compared to the device T_1. For device T_1, quantum effects are inevitable as its thickness is 3 nm and the model predicts its characteristics equally good as that of the other devices which have relatively larger L_g. The ability of the model to predict characteristics of varying

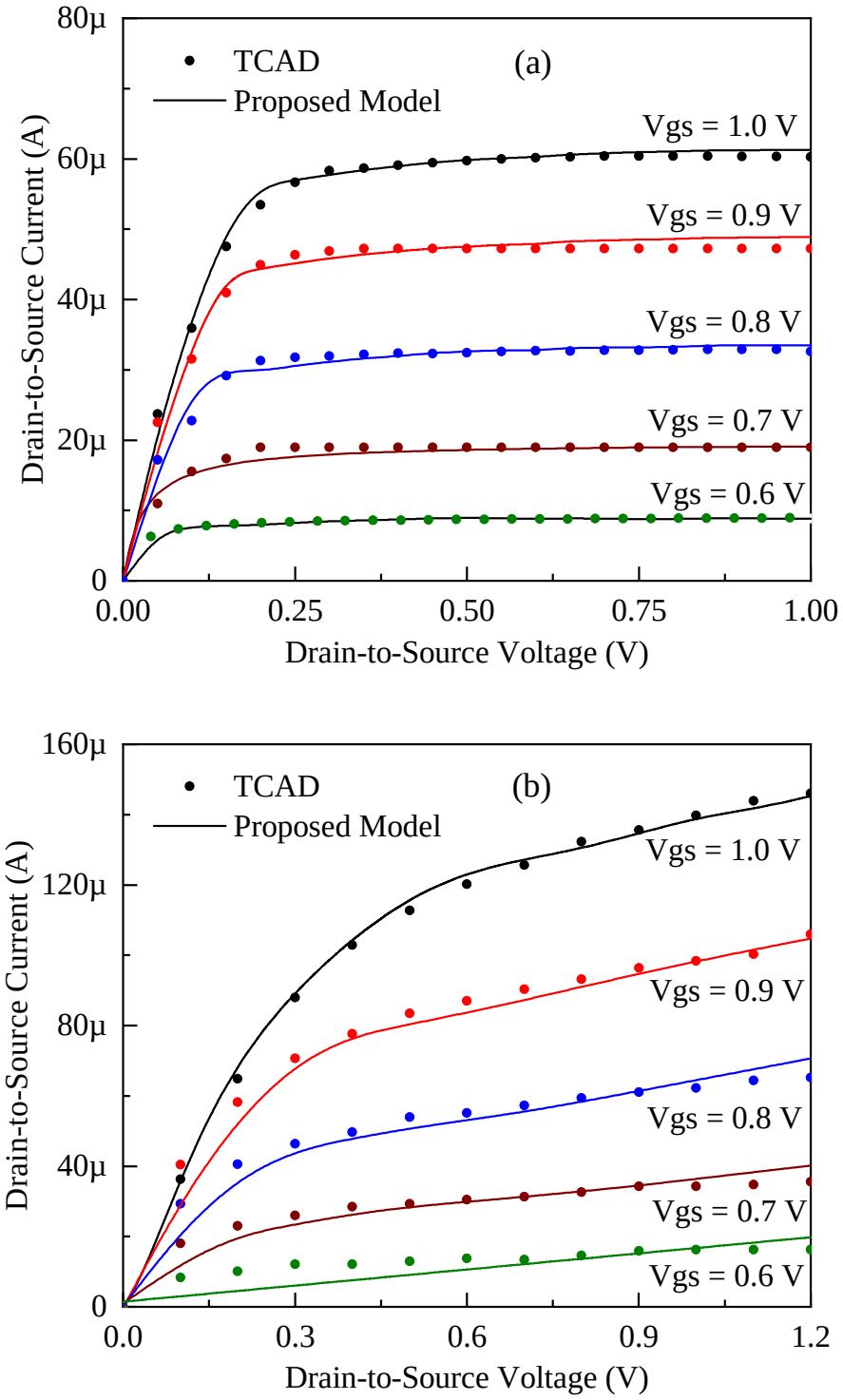

FIGURE 4.7: $I-V$ characteristics of trigate FinFETs for the devices of Table 4.1: a) T_1 and b) T_2.

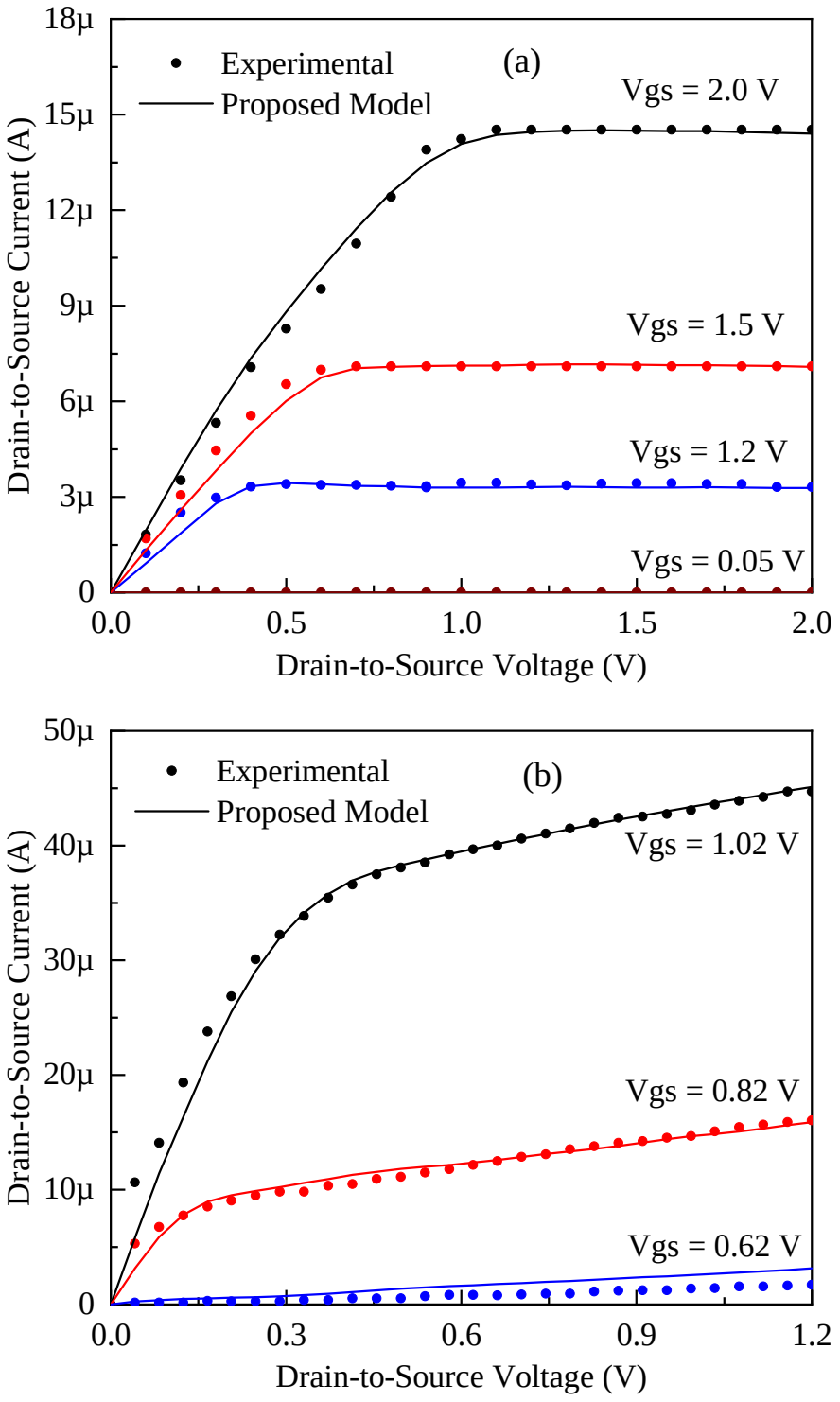

FIGURE 4.8: $I-V$ characteristics of trigate FinFETs: a) T_3 and b) T_4.

dimensions FinFETs with high accuracy, is primarily based on its comprehensive 3D formulation for both Poisson and Schrödinger equations.

To establish the validity of the proposed model further, output and transfer characteristics of all the transistors under discussion are plotted and shown in Figs. 4.9 and 4.10. Examining the plots of these figures, it is evident that the proposed model is capable of predicting both the output and transfer characteristics of FinFETs with high accuracy.

The data presented in Table 4.3 establishes the difference between $I-V$ characteristics modeled using a conventional 2D approach and the proposed 3D technique. The model given in [146] represents $I-V$ characteristics evaluated using a NEGF with conventional Fermi-Dirac distribution [8], while the proposed model uses a 3D NEGF with modified Fermi-Dirac distribution to predict difference in Fermi

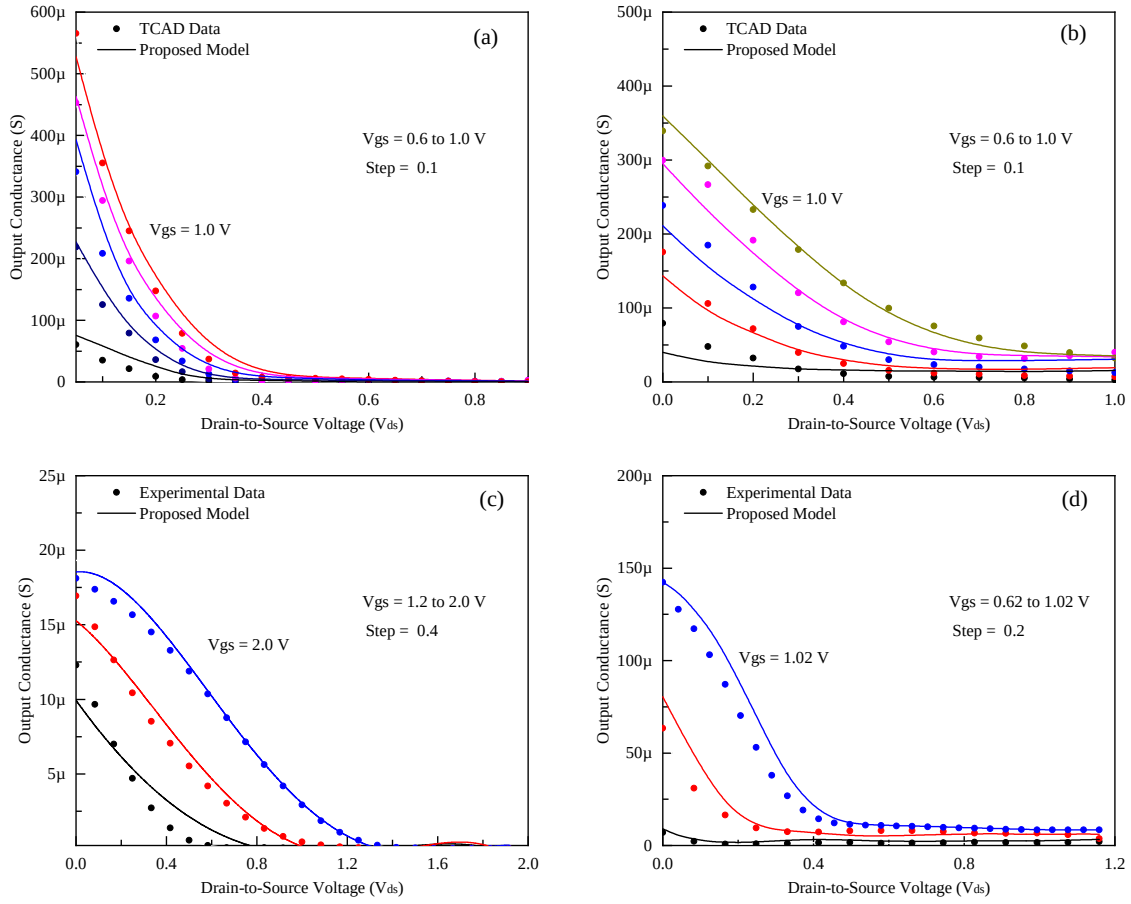

FIGURE 4.9: Output conductance of trigate FinFETs for the devices of Table 4.1: a) T_1 , b) T_2, c) T_3 and d) T_4.

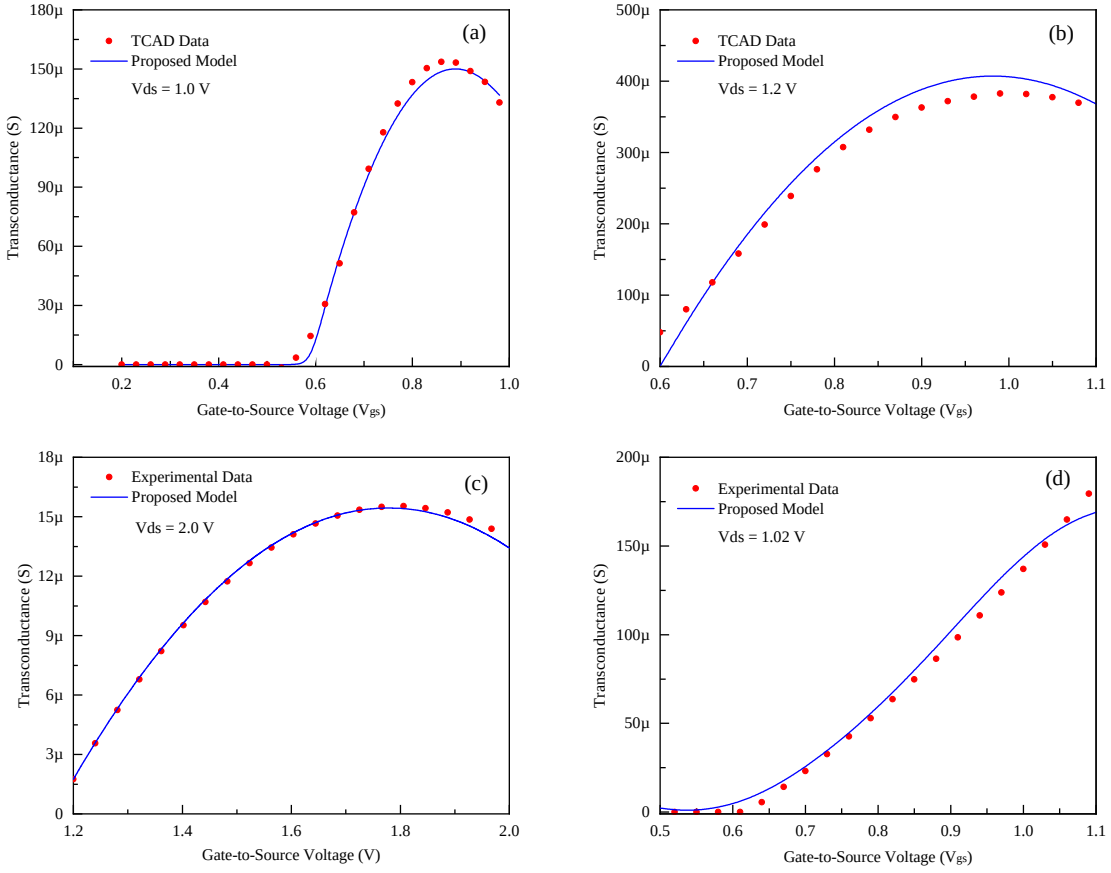

FIGURE 4.10: Transconductance characteristics of trigate FinFETs for the devices of Table 4.1: a) T_1 b) T_2 c) T_3 and d) T_4.

TABLE 4.3: Average root mean square error (RMSE) of the devices mentioned in Table 4.1.

Avg. RMSE ($\times$ 10^{-4})	**Device**			
	T_1	T_2	T_3	T_4
2D Model [146]	6.2	27	3.7	43
Proposed 3D Model	3.2	4.8	0.9	4.4
Relative Improvement	48%	82%	78%	92%

energies and then the device current. As seen from the table, at relatively small L_g, the errors of both the models are comparable i.e., for device T_1. However, when the device dimensions increase, error values for 2D model increase significantly compared to the proposed model, since quantum effects are significantly less at higher L_g and the proposed model caters for it by employing the 3D Poisson equation.

4.4 Summary

In this chapter, a 3D Schrödinger-Poisson model is presented to predict the DC characteristics of rectangular trigate FinFETs. In the proposed model, a 3D Schrödinger equation is solved for FinFET geometry to find the difference of Fermi energies between the source and drain contacts responsible for current flow. To determine the FinFET channel field, it is necessary to have the knowledge of charge distribution inside the channel. The same is evaluated by solving a 3D Poisson equation considering the constraints defined by the geometry of the device. Coupling Schrödinger-Poisson solution, the output current as a function of applied bias is evaluated using a non-equilibrium green function (NEGF). For validation, experimental FinFET $I-V$ characteristics are compared with the modeled data and a good degree of accuracy is observed. Output conductance and transfer characteristics are also compared which further confirm the validity of the proposed model to predict the DC response of nanoscale FinFETs. The model is checked for devices having $T_{fin} = 3-35$ nm to establish its reliability for a wider range of FinFETs. Based on the demonstrated results, the proposed model could be engaged in CAD related tools meant to predict DC characteristics of trigate FinFETs.

Chapter 5

Predict DC Characteristics of Nano FinFETs Using Deep Neural Network

5.1 Introduction

The semiconductor industry is the backbone of modern digital and analog devices wherein, transistors play a vital role. To improve performance, the device size is reduced for each coming generation [150, 151]. However, reducing the size of the device causes additional complexities in characteristics. Devices with dimensions less than 10 nm exhibit non-ideal behavior referred to as short channel effects. Special techniques are then required to overcome short channel effects and the inception of FinFET is one of those.

In recent years, FinFET have attracted considerable attention from researchers working in the field of nano-devices. FinFETs relative to conventional FETs offer improved performance because of the wrapped gate geometry which provides better control over the device channel [104, 152, 153]. The introduction of nano-FinFETs triggered a revolution in device scaling and opened a new era of scalability. Currently, tri-gate FinFETs are becoming highly competitive in the market

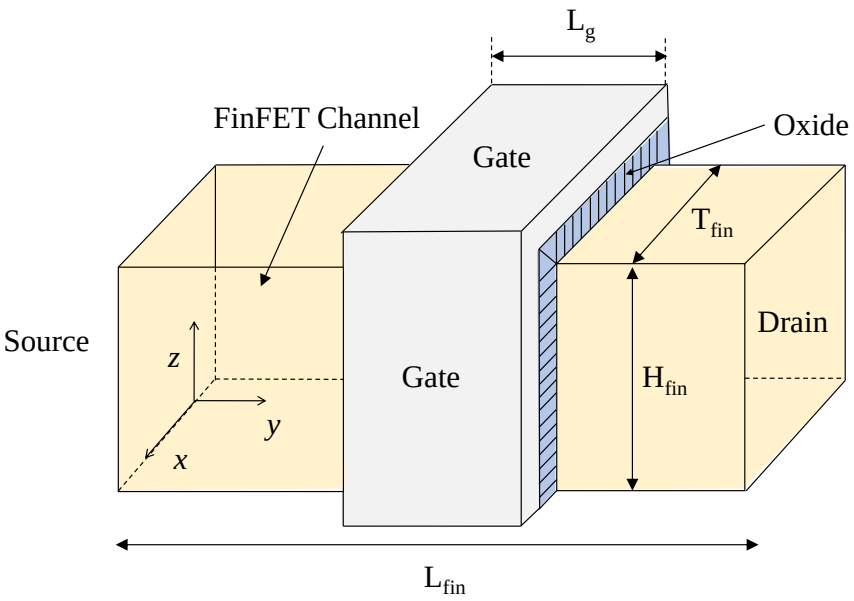

FIGURE 5.1: 3D view of a tri-gate FinFET.

with established 14 nm/16 nm technologies. Their tri-gate nature, in which a thin channel is wrapped by the gate from three sides gives superb control upon the flow of carriers hence, the design mitigates substantially the short channel effects. This also enables the device to exhibit relatively better transconductance with decreased leakage current when compared with conventional FETs [98, 150, 154–158].

Moreover, to improve the performance, different novel structures of FinFETs have been proposed by varying their physical parameters such as: gate length (L_g); fin height (H_{fin}); fin thickness (T_{fin}); oxide thickness (T_{ox}); and doping concentration (N_d) [152, 155, 156, 159]. Fig. 5.1 shows a 3D view of a tri-gate FinFET and its associated physical dimensions. The fin height to thickness ratio (H_{fin}/T_{fin}) plays an important role in determining the performance of the device [160]. A high-aspect ratio FinFET offers improved performance at the cost of additional fabrication challenges [152]. Such devices require several iterations and time; resulting in increased developmental cost. Moreover, while scaling down the device, reduction in T_{fin} beyond certain limits poses serious challenges such as quantum confinement, along with gate wrapping limitations [156]. Source-drain punch-through is another challenge that could cause a large leakage current due to the absence of gate at the bottom of the fin [155]. A punch-through stopping layer

can be employed to stop this leakage current, but this can also induce some other critical issues such as: large drain junction tunneling current and large junction leakage current, and also makes the fabrication process more complicated [161].

In ultra-thin devices, where the complete device has been scaled down, the analysis of its performance is considered to be a challenging task. Researchers working on such devices, usually rely upon computational tools referred to as technology computer-aided design (TCAD), to assess the device performance. Normally, TCAD tools employ numerical computation methods based on the device physics to simulate output characteristics. Though, TCAD is believed to be a fairly successful technique, such an approach is time consuming and computationally expensive and requires a high performance simulation system to predict the device characteristics [98, 162].

Numerous techniques have been proposed to reduce the time, including analytical, numerical, and empirical models which are developed, for a given device, to deal with electrical characteristics as a function of device bias and physical variables [45, 92, 101, 163, 164]. The development of an analytical model requires complete knowledge of carrier transport mechanism and its dependence on the device physics and applied bias which is a cumbersome job and usually not preferred by a design engineer. On the other hand, device characteristics can also be realized by developing an empirical model which can generate the device response as a function of the applied bias [26]. Such a modeling technique is relatively easy and is also a time efficient approach. However, it is usually based on a high number of assumptions, and largely has little or no dependence on the device physics.

The industry has been flooded with less artificial and more intelligent problem solving systems in every field. The analytical models can be referred to as unintelligent models that completely succumb to out-of boundary variation in the system instead of learning from it. On the other hand, machine learning approaches, in this respect have outperformed analytical based modeling techniques. A machine learning approach has the capability of teaching itself in a given environment and then predicting an unknown scenario within a framework for which it has been

trained. As a result, machine learning based device modeling has been a focus of research aimed to reducing the computational time, cost, and human effort for device characteristics [110, 111, 152, 165, 166]. Numerous models have been reported using artificial intelligence based techniques such as an artificial neural network (ANN) model developed by Hatami *et al.* [166] to generate $I-V$ characteristics of metal oxide semiconductor field effect transistor (MOSFET). Hatami *et al.* model requires training to assess $I-V$ characteristics of MOSFETs. However, their model was incompetent when tested on out-of-sample data. This, showed that the developed ANN architecture was not capable of understanding and linking all those variables responsible for generating $I-V$ characteristics of MOSFETs. He *et al.* [110] also proposed a model with a similar approach and presented the approach with less than 1% error compared with measured data. Choi *et al.* [111] reported a complex approach in which finite equations based on the device physics were employed. They used a machine learning technique to find appropriate modeling functions to predict DC characteristics of a Si MOSFET. Recently, Mehta *et al.* [112] proposed a machine learning approach to predict the drain current and bias dependent capacitance of FETs by taking datasets from simulated devices.

In general, machine learning approaches are more efficient than conventional techniques but face tough challenges in the dataset that is required for training. Already established algorithms for MOSFETs/MESFETs can be trained for FinFETs, with less effort by using a transfer learning approach [167]. However, the use of a transfer learning approach in such a case will have limitations because the dataset for training purposes will be altogether a different one [168]. In view of these constraints, a comprehensive machine learning model has been devised that works on FinFET by involving its physical dimensions. The developed approach can be modified to predict MESFET/MOSFET characteristics provided it has been trained appropriately by using the relevant device dataset. Hence it can safely be assumed that the proposed technique would be sufficiently a versatile for predicting the FET characteristics of various natures.

In this chapter, a machine learning approach has been developed which uses FinFETs' physical parameters, bias voltage, and DC characteristics to train a deep neural network (DNN). The technique optimizes the solution by learning the device physical parameters through hidden nodes and an activation function which eventually generates the DC characteristics of the device. Once the DNN is trained, it is then engaged to predict the DC characteristics of an unknown FinFET by using its physical parameters. The validity of the proposed technique was checked using COMSOL Multiphysics [169] which showed that the predicted DC characteristics of the nano-FinFETs were within a maximum mean square error (MSE) margin of 3.36×10^{-3}. The proposed technique is highly time efficient, and provides fast prediction of FinFET DC characteristics. To the best of our knowledge, DNN based prediction of nano-FinFET characteristics as a function of their physical dimensions is not reported in the literature. Hence, the technique could be a useful tool for the design engineer to obtain the output characteristics of the FinFET using its physical parameters prior to its realization.

5.2 Modeling Methodology

To develop a technique involving DNN to predict the FinFET's DC characteristics, the first and foremost requirement is selecting an appropriate DNN architecture, involving fundamental FinFET design parameters and associated characteristics. Once the architecture is designed, both its validity and accuracy can be assessed using the FinFET's known characteristics. By evaluating the error values of the target and predicted characteristics, the DNN architecture can be fine-tuned to arrive at an optimized solution. The DNN model thus developed will be trained on a known dataset generated for the purpose. The trained DNN model can then be used to assess the device characteristics as a function of its physical parameters before its realization.

5.2.1 DNN Model

Inspired by the human brain, an artificial neural network is used to solve complex problems by transforming them into various interconnecting nodes [170, 171]. Each node is a linear combination of weights and bias values which processes through an activation function interconnected to adjacent layers. Fig. 5.2 shows the functioning of a single neuron in the network which can be written as

$$x_1^{l+1} = \sum_{j=1}^{n} x_j^l \omega_j^l + b^l \tag{5.1}$$

here, n is the total number of neurons in previous layer l where $l+1$ is the current

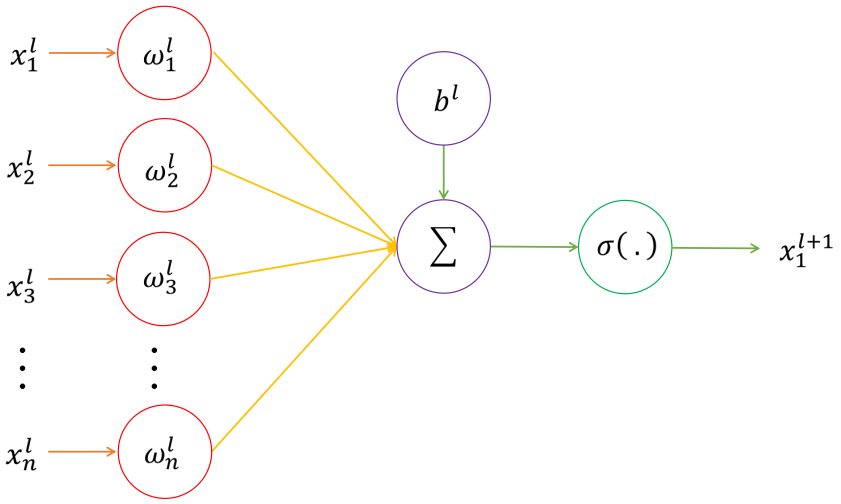

FIGURE 5.2: Processing flow to get output from a single neuron of a multilayer network system.

layer. Eq. (5.1) is used to represent a single neuron in a multilayer network. However, for more than one neuron and layer, this equation is required to be generalized and can be written in matrix form as

$$\begin{bmatrix} x_1^{l+1} \\ x_2^{l+1} \\ \vdots \\ x_m^{l+1} \end{bmatrix} = \begin{bmatrix} \omega_{11}^l & \omega_{12}^l & \dots & \omega_{n1}^l \\ \omega_{12}^l & \omega_{22}^l & \dots & \omega_{n2}^l \\ \vdots & \vdots & \ddots & \vdots \\ \omega_{1m}^l & \omega_{2m}^l & \dots & \omega_{nm}^l \end{bmatrix} \begin{bmatrix} x_1^l \\ x_2^l \\ \vdots \\ x_n^l \end{bmatrix} + \begin{bmatrix} b_1^l \\ b_2^l \\ \vdots \\ b_n^l \end{bmatrix} \tag{5.2}$$

here, m is the number of neurons in the current layer.

Equation. (5.2) is used to calculate the output of each neuron of a multilayer network. To incorporate non-linear properties in a neural network, activation function (σ) is used to arrange the data into a specific range. There are different types of activation functions such as tanh, softmax, rectified linear unit (ReLU) and sigmoid [171]. Although, the activation function is chosen according to the complexity of the neural network, number of inputs, and nature of the problem where it has to be applied, there is no specific rule for the selection of an activation function to achieve better accuracy. A couple of activation functions were tried in the developed DNN and based on MSE it was observed that the sigmoid activation function, defined in Eq. 3.3, offers better performance compared to others as shown in Table 5.1.

$$\sigma(x_j^l) = \frac{1}{1 + \exp(-x_j^l)} \tag{5.3}$$

It is observed from Eq. (5.2) that, the output is a linear combination of input, weights, and bias data. Eq. (5.3) is used to add nonlinearity in the DNN model. The matrices of weight and bias vectors are updated to fit the training datasets in each epoch, where an epoch is one complete training iteration through the entire dataset. Thus, each epoch tries to update the weights to reduce the error between predicted output and actual output. On initialization of DNN training, the model assigns random weights and bias values, which are processed through each layer of neurons to reach the output layer. In addition, the error obtained in the output

TABLE 5.1: MSE attained using various activation functions during DNN training process.

Activation function	MSE (10^{-3})
Softmax	45.6
Linear	24.2
Tanh	5.2
ReLU	3.3
Sigmoid	3.0

TABLE 5.2: Effects of number of hidden layers and neuron on the proposed DNN technique to predict DC characteristics of FinFETs.

Hidden Layer	Epochs	MSE (10^{-3})
512, 256, 128	120	3.7
256, 128, 64	200	3.7
128, 64, 32	350	3.7
64, 32, 16	800	3.7
512, 512, 512	50	3.7
256, 256, 256	70	3.7
128, 128, 128	200	3.7
64, 64, 64	400	3.7
512, 256, 128, 64	500 to 1000	4.6
256, 128, 64	280	3.7
256, 128	130	3.7
256	500 to 1000	3.9

is also propagated in the next epoch to adjust the weights accordingly in order to minimize the error.

The proposed model is built in the Python programming language using Keras [172]. A learning rate of 0.001 is used in the ADAM optimizer [173], which is computationally efficient, requires less memory, and is suitable for a large dataset and or/ a large feature vector. Different combinations of layers along with epochs, listed in Table 5.2, are also tested to achieve the optimum value of training mean square error (MSE). The minimum MSE is achieved using a three layer network with sigmoid as an activation function, having $512, 256, \text{and} 128$ neurons in each layer. Other training parameters, used in DNN training to achieve the minimum MSE, are summarized in Table 5.3.

5.2.2 DC Characteristics of FinFETs

FinFET has a 3D channel referred to as the fin of the device which is enveloped on three sides by the gate metal is called a tri-gate device [111]. The 3D gate structure allows better control over the channel current which reduces the device

TABLE 5.3: Various parameters used in DNN architecture developed to predict DC characteristics of FinFETs.

Parameter	Description
Traning algorithm	Back Propagation
Network Type	Feed-Forward
Activation Function	Sigmoid
Number of Hidden Layers	03
Number of Neurons in 1^{st} layer	512
Number of Neurons in 2^{nd} layer	256
Number of Neurons in 3^{rd} layer	128
Test data	20%
Loss Function	MSE
Epoch	2000
Learning Rate	0.001
Optimizer	ADAM

leakage and short channel effects. Fig. 5.1 shows a 3D view of a tri-gate FinFET with its physical dimensions marked as L_g, T_{fin}, H_{fin}, and L_{fin}. This is n-channel depletion type FinFET and same has been employed for the generation of dataset for COMSOL simulation.

FinFET device structure employs either bulk or silicon on insulator (SOI) substrate. In SOI substrate, the buried oxide thickness, T_{ox} under the gate contact cannot induce an inversion layer at the bottom surface [162]. Further, depending upon the dominant carrier concentration $N_{d,a}$, they are classified into either p or $n-$channel devices. For extracting the DC characteristics, $n-$channel FinFETs have been used in this study, and the device output and transfer characteristics are evaluated as a function of drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltage. It has been observed that, the magnitude and shape of drain-to-source current (I_{ds}) in both the linear and saturation region of operation are dependent upon the bias and chosen physical dimensions of the FinFETs. For the devices under discussion, V_{ds} bias was kept lower than the breakdown value whilst V_{gs}, which controls the amount of I_{ds} trasversing through the channel by changing the depletion inside, was varied from threshold to a value where a tangible I_{ds} was observed. Depending

upon the channel parameters, both normally OFF and ON devices were realized for this study. The dataset of output characteristics as a function of applied bias was prepared by varying the physical variables ($L_g, N_d, T_{fin} \ldots$).

5.2.3 Features and Output Vector of the DNN Model

The proposed DNN model was trained using simulated DC characteristics with associated physical parameters: L_g, H_{fin}, T_{fin}, T_{ox}, L_{fin} and N_d, (Table 5.4). It was noted through series of experimentations that 60 FinFETs provide sufficient data out of which 80 % can be used to train the DNN. The dimensions of the devices were varied randomly and each device was simulated for multiple V_{gs} values to obtain a family of output characteristics to be employed for training purposes. Furthermore, each $I-V$ curve was also attained for a range of V_{ds} values, which in return adds V_{ds} into the input vector for the training of the model. Using COMSOL, a family of Ids(V_{ds};V_{gs}) curves are generated for each device and a minimum number of curves for one device was at least five. If the dataset is based on 60 devices then the minimum number of $I-V$ curves the dataset will have is $60\times5 = 300$. Additionally the data was generated by using ordinary and extraordinary dimensions of FinFETs to ensure that the model works both for usual and limiting dimensions of the device. The other variables chosen during DNN training are explained in Table 5.3.

A basic architecture of the training model is shown in Fig. 5.3. The model accepts an input vector comprising of device dimensions L_g, H_{fin}, T_{fin}, T_{ox}, L_{fin}, and N_d and bias voltage. All these are interconnected by a set of weights as shown in Eq. (5.1). Initially, using random weights and biases, the information is processed from the input to the output layers passing through each hidden layer in a process called feedforward propagation. During the feed-forward propagation, Eq. (5.1) is used to evaluate the next neuron, based on the previous layer information. At the output layer, an error is generated between the output and target characteristics which is back propagated [174], to be used in the next epoch. The loop continues until the total number of epochs are reached or the error is minimized [112]. For

TABLE 5.4: FinFET parameters used in COMSOL software to generate dataset by varying the given dimensions randomly between the two limits given in the Table.

Parameters	Values
L_s	10 nm
L_d	10 nm
L_g	5 nm to 75 nm
L_{fin}	20 nm to 100 nm
T_{fin}	5 nm to 50 nm
H_{fin}	5 nm to 50 nm
T_{ox}	2 nm to 20 nm
N_d	1×10^{24} m^{-3} to 10×10^{24} m^{-3}
Electron Effective Mass	0.197
Hole Effective Mass	0.8
Relative Permittivity (Si)	11.68
Relative Permittivity (SiO_2)	3.9
Gate Metal Work Function	4.37 V
Electron Affinity	4.05 V
Electron Mobility	1450 cm^2(Vs)$^{-1}$
Hole Mobility	500 cm^2(Vs)$^{-1}$

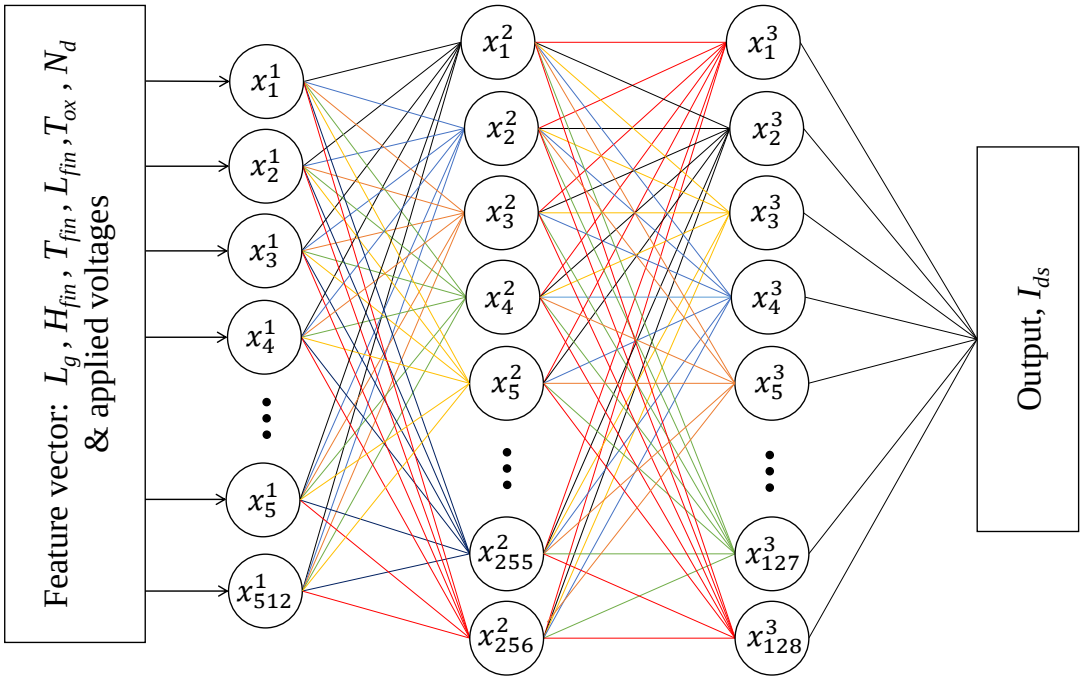

FIGURE 5.3: Schematics diagram of the proposed DNN model developed to predict output characteristics of nano-FinFETs.

updating the weights, gradient descent algorithm is used in the back propagation in an attempt to reduce the error. Error is defined by the average mean square of the difference between target and network output. Mathematically it can be represented as:

$$\text{MSE} = \frac{1}{M}\sum_{j=1}^{M}\left[\frac{1}{N}\sum_{i=1}^{N}\left(I_{ds}^{A}(i,j) - I_{ds}^{P}(i,j)\right)^{2}\right] \tag{5.4}$$

where i, j represent the variation in I_{ds} as a function of V_{ds} and V_{gs}, respectively, such that I_{ds}^{A} represents the actual value of the drain current whilst I_{ds}^{P} is the predicted value at the same point by the network output layer. N represents the number of points while sweeping V_{ds} from minimum to maximum and M represents the number of curves.

The whole methodology for developing a system that can predict the characteristics of an unknown device, is summarized in a flow chart given in Fig. 5.4. The data generated by COMSOL Multiphysics are split into training/test data with 80/20 ratio. After initializing all the DNN parameters as listed in Table 5.3, the model is trained using the training data. It is worth mentioning that the network is trained to attain a minimum value of MSE for given epochs. The trained model is then tested and error is evaluated by comparing the predictions based on the feature vector and the test data. The model is said to be well trained, if it shows a prediction error lower than or closer to the average training MSE.

5.3 Results and Discussion

Since the fin of the device is the structure through which the current flows, its height, thickness and length are the most influential parameters. Further, doping concentration also has a direct influence on the current flow from the device therefore, this same was also taken into consideration as a variable. The 3D structure of the simulated device is shown in Fig. 5.1 and the dimensions of variables are explained in Table 5.4. The device geometry was created in COMSOL software

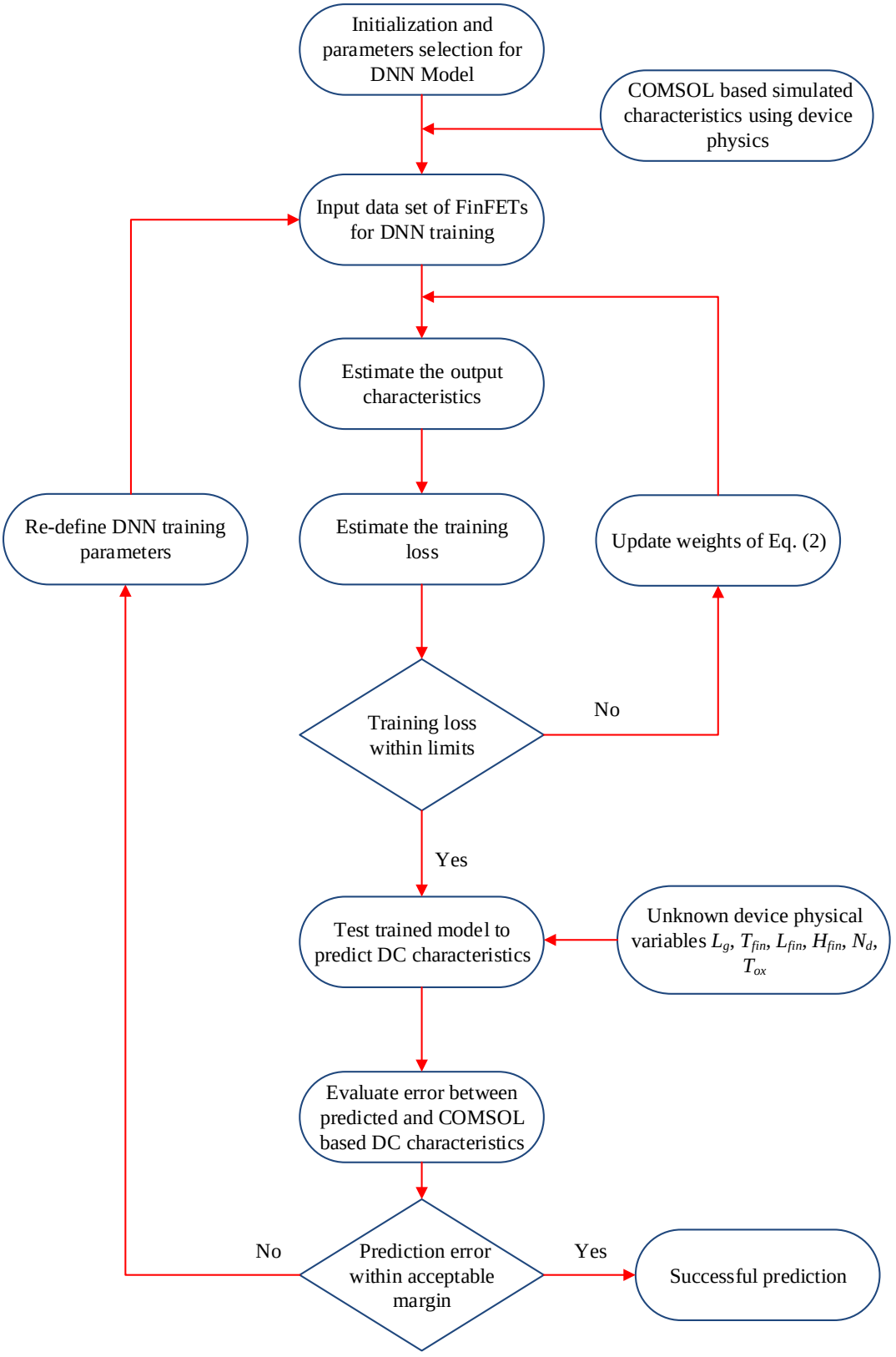

FIGURE 5.4: DNN based training and prediction mechanism to compute DC characteristics of FinFETs.

and each feature of the device is identified uniquely including: ohmic contact; schottky contact; oxide nature (SiO_2), channel layer and doping density. Then the parameters against which the DC characteristics will be plotted are defined as V_{gs} and V_{ds}. Knowing the device dimensions and associated material properties, COMSOL software uses finite element method to solve Schrödinger–Poisson equations governing the channel properties. It divides the entire channel into small pieces using a grid and the size of the grid plays a crucial role in attaining an appropriate solution. It has been noted that a wider grid can solve a problem quickly but at the expense of accuracy. Furthermore, for large grid sizes, the solution has a tendency to diverge. Therefore, for accurate output with high probability of convergence, the grid size should be as fine as possible.

The DNN used herein had five layers such that input and output were represented by one layer coupled with three hidden layers as shown in Fig. 5.3. The number of neurons in first, second, and third hidden layers were 512, 256 and 128, respectively. It was noted that an increase in the hidden layers deteriorated the system performance, and the system also became inefficient with respect to time. During DNN training, the system attained optimized weights for each neuron of the hidden layers and became intelligent enough to predict DC characteristics of a FinFET for which it did not have the data; this is commonly known as a controlled device. After optimization, it was noted that the system attained an overall minimum MSE $\sim 3 \times 10^{-3}$. This value was found from number of training sessions and graphical inspection of training and DNN output data. It is pertinent to mention here that on average the training session took around 330 s and prediction afterward was achieved in a fraction of a second. The trained model afterwards has the ability to predict a device having parameters within the range listed in Table 4.

On the other hand, the simulations performed in COMSOL take much longer compared to DNN prediction. The time consumed by COMSOL for two typical extreme cases in each experiment is listed in Table 5.5. Examining the table it is obvious that varying, H_{fin} from 5 nm to 50 nm changes the required simulation time from 6 min to 3 h and 29 minutes. The highest observed time in Table 5.5 is

41+ h for a FinFET with the following dimensions: $L_g = 10$ nm, $H_{fin} = 50$ nm, $T_{fin} = 30$ nm, $T_{ox} = 2$ nm, $L_{fin} = 10$ nm and $N_d = 1 \times 10^{24}$ m^{-3}. This clearly demonstrates that the time cost for the COMSOL model is significantly higher than for the DNN model which takes milliseconds to compute the characteristics once it has been appropriately trained. Thus, the proposed technique can save considerable industrial time; resulting in a possible reduction in the cost of the product.

Figure 5.5 shows the results of the DNN model in comparison to the COMSOL simulation. The devices were chosen such that their output characteristics would have variations in their profiles associated with the device physical dimensions. This enables us to assess the robustness of DNN based prediction. Figure 5.5(a) shows that the device relative to the device of Fig. 5.5(b) offers better output characteristics both in the linear as well as in the saturation region of operations. The only variation in the device physics is the value of L_g which is 70 nm for 5.5(a) and 10 nm for 5.5(b). Increasing the L_g decreases the fringing effects, and thus allows the gate metal to have better control on the channel. Figure 5.6 shows transfer characteristics of the devices under consideration. This figure once again exhibits the validity of the proposed technique to predict FinFET characteristics.

Examining the plots of Figs. 5.5 and 5.6, it is obvious that one can optimize the physical variables of the device to achieve target characteristics. However, this will generally, will be a cumbersome task and require a considerable amount of time and resources. By employing the proposed technique, this can phenomenally reduced without compromising the quality. MSE values of DNN based predicted characteristics relative to COMSOL data are evaluated and given in Table 5.6. In all the predicted devices the average MSE is less than 3×10^{-3} which demonstrates that the achieved MSE of the predicted characteristics of the test devices is within system defined limits.

Prediction accuracy in any DNN model cannot be associated with a specific element as the DNN passes the patterns of information attained from the input layer to the neurons in the next layers which finally arrive at the output units. This accuracy can nevertheless be increased by increasing the data size and/or improving

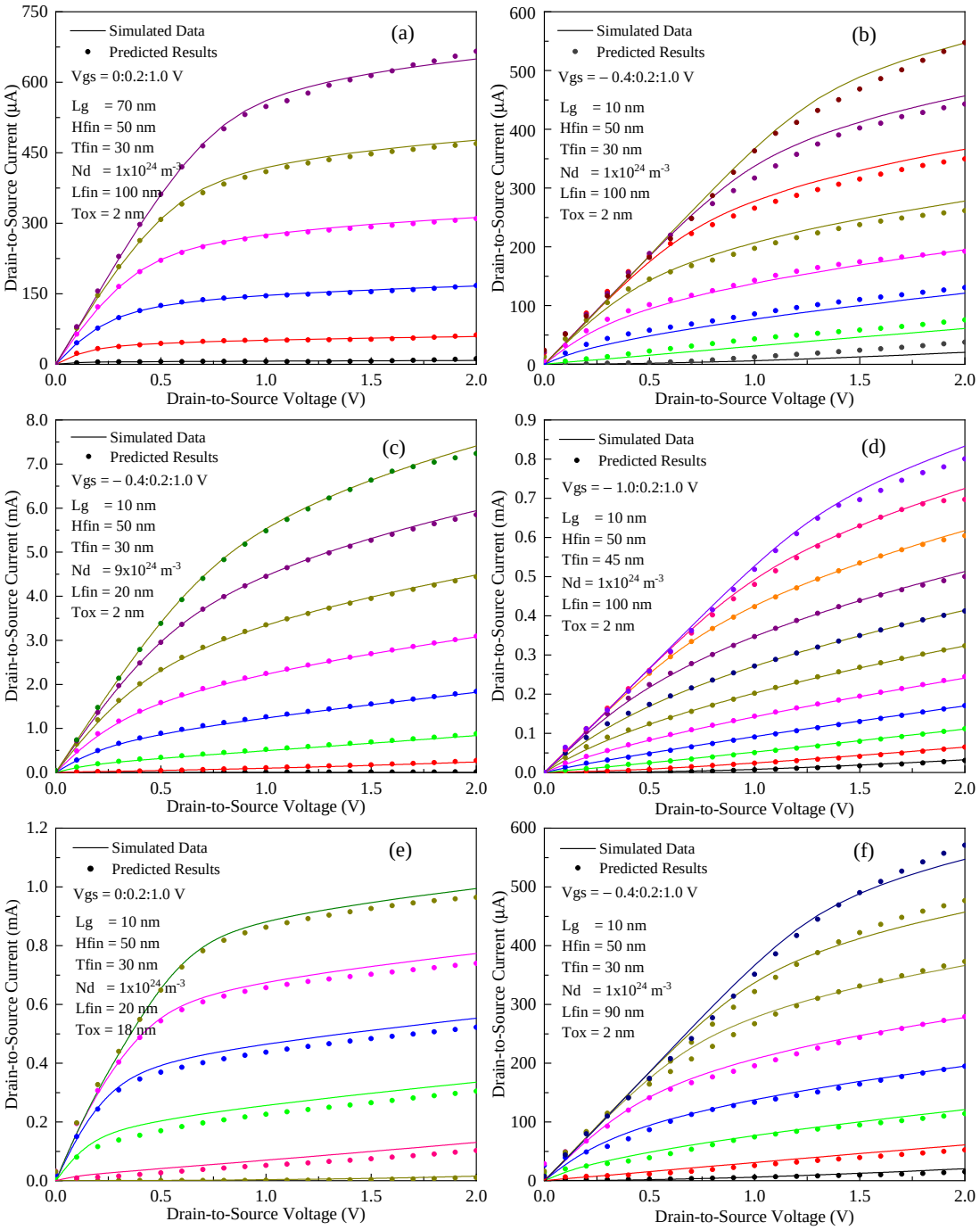

FIGURE 5.5: $I-V$ characteristics of nano-FinFETs predicted using a DNN model. From (a) to (f) solid lines indicate data attained from COMSOL simulation while dots represent the characteristics generated by the DNN technique.

network layers design [175]. Training data size, however constrains the number of layers such that more training samples are required for shallower models. The variation of accuracy from device to device as observed in Fig. 5.5 and depicted in Table 5.6 cannot be explicitly associated with any chosen physical parameter

of the device, DNN architecture or variables.

To further validate the proposed DNN framework, the output characteristics of another set of six devices are shown in Fig. 5.7. In this comparison, the maximum observed average MSE value was 2.29×10^{-3} for the device of Fig. 5.7(f) and the minimum observed MSE was 0.37×10^{-3} for Fig. 5.7(a). Both these values are within the margin defined by the system ($\approx 3 \times 10^{-3}$).

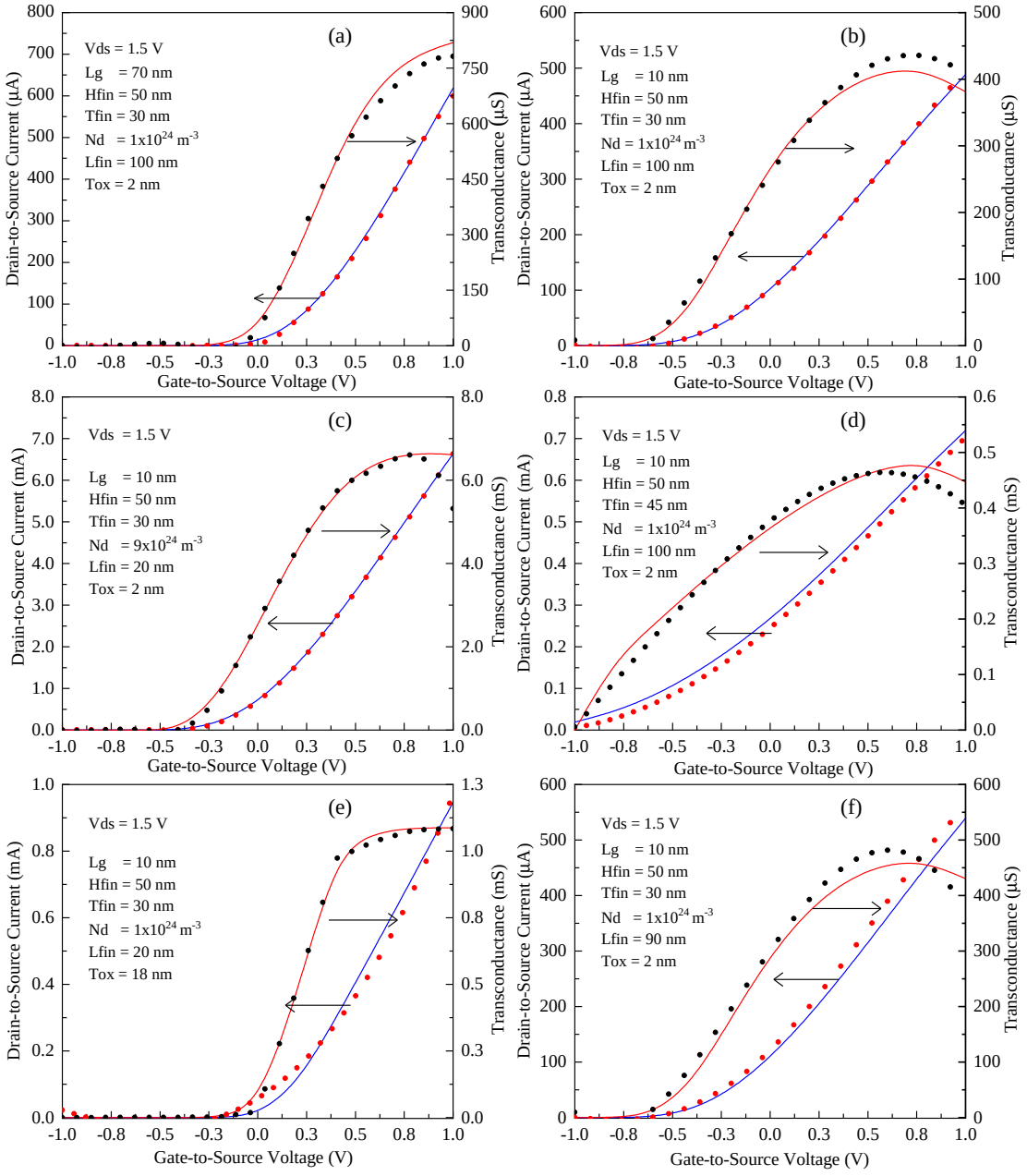

FIGURE 5.6: Transconductance and drain current variation of nano-FinFETs as function of applied bias. (a) to (f) solid lines indicate COMSOL data while dots represent DNN based predicted characteristics.

TABLE 5.5: Typical time consumed by the COMSOL software to generate DC characteristics for two extreme values of various physical variables of FinFETs. A complete set of variables for these devices are given in Table 5.4.

Variable	Min, Max Values	Time (hours:minute)
Fin Height, H_{fin}	05 nm	00:06
	50 nm	03:29
Gate Length, L_g	05 nm	03:11
	75 nm	03:29
Fin Thickness, T_{fin}	05 nm	00:12
	50 nm	07:56
Oxide Thickness, T_{ox}	02 nm	04:50
	20 nm	14:57
Fin Length, L_{fin}	10 nm	41:28
	100 nm	03:19
Doping Concentration, N_d	1×10^{24} m^{-3}	07:20
	10×10^{24} m^{-3}	32:56

TABLE 5.6: Mean square error (MSE) values of simulated and DNN based predicted characteristics of six different FinFET having physical dimensions of that of Fig. 5.5

	Devices MSE (10^{-3})					
V_{gs} (V)	Fig. 5.5a	Fig. 5.5b	Fig. 5.5c	Fig. 5.5d	Fig. 5.5e	Fig. 5.5f
-1.0	-	-	-	0.472	-	-
-0.8	-	-	-	0.261	-	-
-0.6	-	-		0.174	-	-
-0.4	-	3.364	0.0001	0.120	-	1.04
-0.2	-	1.846	1.317	0.129	-	1.042
0	0.501	0.100	1.204	1.001	1.40	0.614
0.2	0.214	0.416	0.560	0.148	2.403	0.398
0.4	0.177	0.699	0.328	0.274	1.913	0.434
0.6	0.224	0.794	0.499	0.222	1.242	0.536
0.8	0.360	0.712	0.653	0.471	0.898	0.754
1.0	0.382	0.637	0.920	0.806	0.687	0.679
Avg	0.310	0.12	0.685	0.292	1.40	0.687

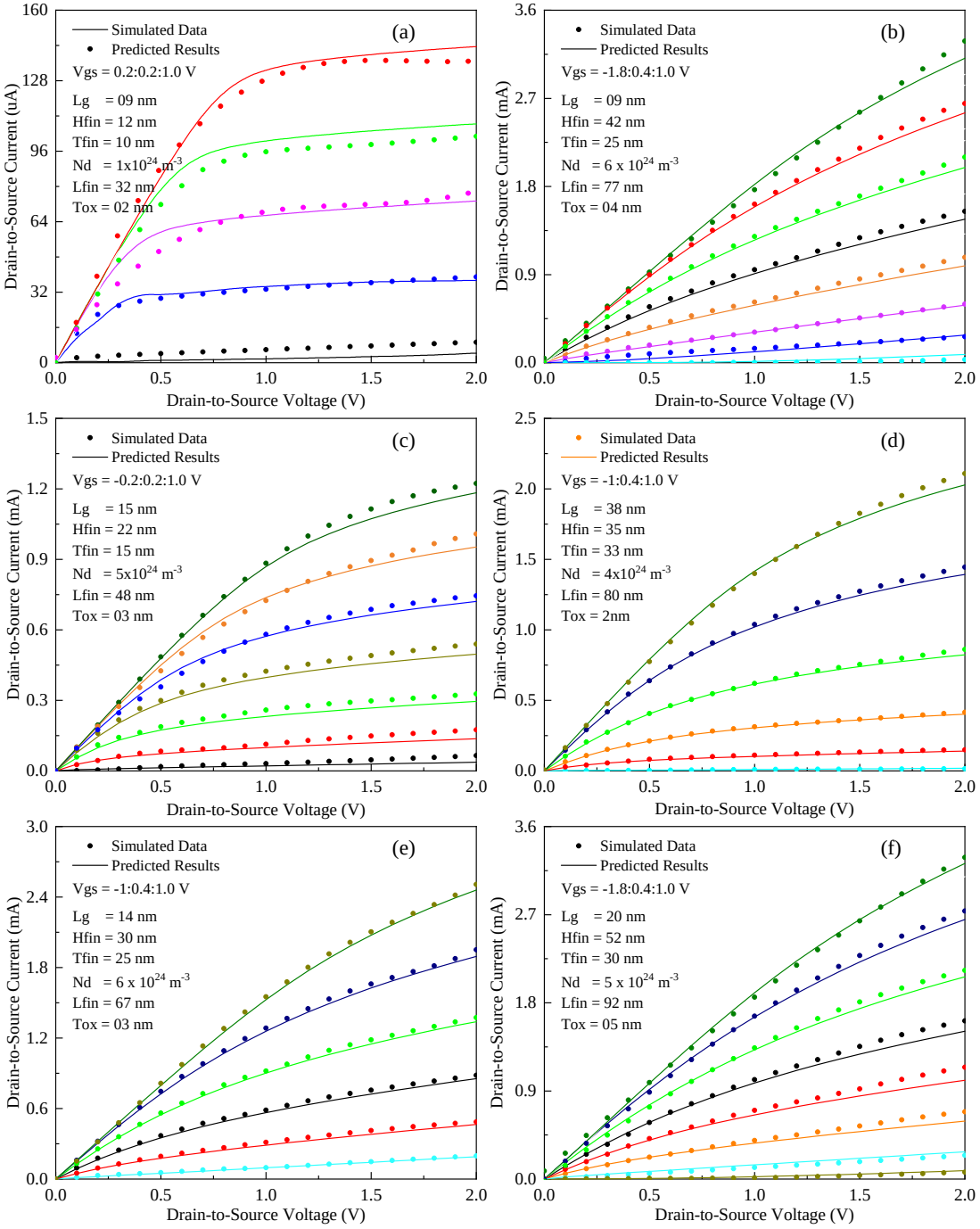

FIGURE 5.7: Transconductance and drain current variation of nano-FinFETs as function of applied bias. (a) to (f) solid lines indicate COMSOL data while dots represent DNN based predicted characteristics.

5.4 Summary

In this chapter, a technique has been proposed using a deep neural network (DNN) to predict DC characteristics of nano-FinFETs. A sizable dataset of DC characteristics was first generated using an established software tool (COMSOL) by varying the device physical dimensions such as gate length (L_g), fin height (H_{fin}), fin thickness (T_{fin}), and fin length (L_{fin}). The DNN was then trained using the selected data (80%) and the accuracy of the training process was ensured through minimum target error value. The trained DNN model successfully predicted FinFETs DC characteristics as a function of applied bias for a given device physical dimensions. The established technique is exceptionally time efficient when compared with standard device simulation software (COMSOL). A comparison of the simulated and predicted data suggests that the developed technique provides on average MSE lower than 2.29×10^{-3}, and can predict the device response with acceptable accuracy by varying the device physical dimensions. The technique, therefore, provides a useful tool for predicting the DC characteristics of a FinFET prior to its fabrication and can save valuable industrial process time.

Chapter 6

Conclusion and Future Work

The electronics being used nowadays are compact in size, consume less power, have high data rate, and can be transported into space quite easily. This has been made possible due to high performing semiconductor FETs that are improved a lot over the decades. The use of FETs increased exponentially after their invention but the end products involving FETs faced certain performance challenges discussed in detail in this research work. These performance factors are affected increasingly because of the fast reduction in device size along with a pressing demand of better or at least similar level of performance. FET based circuitry, both in analogue and digital domains, have a crucial role in electronic industry, however, FET performance is clamped down due to increased degradation in its characteristics caused by the downscaling of the device.

To overcome the challenges faced by the planar FETs; FinFETs having 3D geometry with multi-dimensional gate to control the channel current are introduced. They offer a viable option for microwave high-tech applications, because of their 3D structure, which permits effective gate control over the channel. Owing to 3D gate geometry, FinFETs have effectively mitigated short-channel effects and offered considerably lower switching time, lower dynamic power loss, and higher current density compared to planar FETs. Because of the improved sub-threshold characteristics and exceptionally low leakage current, FinFETs provided a greater

level of integration compared to other FET technologies hence, paved the way for future scaling of integrated circuits.

FinFET performance is heavily reliant on the wafer properties and device geometry. The wafer properties include mobility, doping density, saturation velocity, quality of 2DEG etc. Whereas, device geometry includes; fin height, fin thickness, gate length, fin length and oxide thickness. The electrical performance of a finished FinFET depends upon the carriers mobility, their transportation under applied bias and channel response to the signal received at the gate electrode. In order to get an optimum device both from material and design perspective, it is important to have an appropriate selection of device wafer and also a suitable device geometry as per need of the circuitry. It is pertinent to mention here that in FinFETs, the dimensions pertained to the fin such as fin height, fin length and fin thickness coupled with the gate length are of prime importance. At nanoscale, such devices exhibit non-traditional characteristics known as ballistic transportation of carriers. In ballistic transport, carriers are represented by a quantum wave function and the device, therefore, can be referred to as a quantum device. This necessitate the need of involvement of quantum mechanics to explain its characteristics.

FinFETs channel can be made using a bulk semiconductor material such as SiC, GaN or GaAs. If the bandgap of the material is relatively low, i.e. ≤ 1.5 eV, then the device performance deteriorates at higher temperatures. In order to make the device compatible for harsh environments including higher temperatures, the channel could be defined by using a wide bandgap material, i.e. ≥ 3 eV. A FinFET with bulk semiconductor channel, its characteristics are determined by the properties of semiconductor along with the applied bias. The applied potential creates a field inside the channel and as a result of that, the channel carriers drift from drain to source defining the device output characteristics. The magnitude of the current can be altered by varying the potential applied at the gate electrode. FinFETs can also be made by using a combination of high and low bandgap materials to generate 2DEG. The 2DEG is controlled by a 3 dimensional gate simultaneously and thus determines the response of the device. Such FinFETs exhibit their

output and transfer characteristics much better than the bulk FinFETs or planar FETs.

If FinFET has a 2DEG channel, then such FinFETs can offer characteristics both in depletion and inversion modes. To describe the response of such devices, a unified model, which can cater both depletion and inversion characteristics simultaneously, would be required. In the first part of the research, a comprehensive $I-V$ model has been developed and it has been shown that the model works reasonably well both in inversion as well as in depletion modes of operation. In the depletion mode, the drain current was assessed using a modified definition of 2DEG carrier concentration caused by the trigate geometry of the device. On the other hand, the inversion part of the model employed Poisson distribution to evaluate the channel potential to be used for the assessment of channel current. The total drain current offered by such devices would then be $I_{ds} = I_{2\mathrm{D}} + I_{inv}$. It has been demonstrated that main contributor to I_{ds} for the gate bias $V_{th} \leq V_{gs} \leq V_{fb}$ is 2DEG of the device, whilst a further increase in V_{gs} potential beyond V_{fb} generates an additional component of the current. This part of the current could be associated with inversion of carriers originated in two side gates of an AlGaN/GaN FinFET.

In the second part of the research, a model has been developed using Schrödinger-Poisson equations to predict DC characteristics of trigate Si FinFETs. In this model, quantum-mechanical ballistic transport of carriers has been considered and channel characteristics have been modeled using a 3D Schrödinger wave equation. Source-drain Fermi energy difference, which is responsible for the flow of carriers, has been evaluated using non-equlibrium green function (NEGF) and 3D Poisson equation. Ohmic contact resistance is an important feature that influences upon the magnitude of drain current and cannot be overlooked in models where accuracy is of prime importance. This feature, in the developed technique, is adjusted using modeled parameters in Fermi-Dirac distribution function. Furthermore, in FinFET at V_{ds}>$V_{ds(\mathrm{sat})}$, the drain current saturates which could be associated to the finite supply of carriers from the source electrode of the device. The developed model is calibrated using a standard tool commonly known as technology computer

aided design (TCAD). On the other hand, the validity of the developed technique is demonstrated using the experimental data of nanoscale FinFETs both for their output and transfer characteristics and a good degree of accuracy is observed. It has been established that the developed technique has the ability to predict FinFETs characteristics having $T_{fin} = 3 - 35$ nm. Hence, the technique could be engaged in CAD related tools meant to predict DC characteristics of trigate FinFETs.

In the last part of research, an attempt has been made to develop an efficient and reliable DNN model to predict DC characteristics of nano-FinFETs. DNN model has been developed by realizing an appropriate set of input and output variables with logical links between them. Keeping in view the required accuracy and efficiency, an appropriate number of layers and associated neurons have been selected. To train DNN, there was a need to have an accurate dataset of ample size comprising of FinFETs DC characteristics. For this purpose, by using an established software tool (COMSOL), a sizable dataset was generated by varying the device geometrical parameters such as, gate length (L_g), fin height (H_{fin}), fin thickness (T_{fin}), fin length (L_{fin}), oxide thickness (T_{ox}) and doping density (N_d). The DNN was trained using the selected data (80%) and the accuracy of the training process was ensured by monitoring minimum target error value. The trained DNN model was then used to predict FinFETs DC characteristics as a function of applied bias for a given device physical dimensions. Comparison of the simulated and predicted data demonstrated that the developed technique is fairly accurate, and can predict the device response by varying the device physical dimensions to an acceptable accuracy. It has been shown that the established technique is highly efficient in time when compared with standard device simulation softwares such as COMSOL. The technique can, therefore, be a useful tool to predict FinFETs DC characteristics prior to their fabrication and can save valuable industrial process time and cost.

This research primarily deals with the prediction of DC characteristics of nanoscale FinFETs irrespective of their materials. Normally, FinFETs are either Si or heterostructure based devices therefore, two famous structures were chosen to develop

techniques for FinFETs DC characteristics which should cover both types of FinFETs. In the first part of research, AlGaN/GaN FinFETs were studied and based on their characteristics, a model has been developed and validated against the experimental data. On the other hand, in the second part of the research, another model for DC characteristics prediction of Si based FinFETs has been developed to provide two independent analytical models to cover a complete range of FinFET devices. In the third part of research, an AI based technique has been worked out and its validity has been demonstrated using Si FinFET data. However, the developed technique is of generic nature and it has the potential to predict AlGaN/GaN FinFET characteristics if the training data of such devices are provided as an input data. Thus, all the three parts of research carried out in this thesis are fairly linked with each other.

6.1 Future Works

1. Since FinFETs are being used in next generation high density SRAMs and other such circuitries, where the temperature of the chip rises with increasing density of transistors. Therefore, temperature dependent FinFETs performance evaluation shall provide a crucial knowledge for determining future growth of high-tech circuitry involving nano-scale FinFETs. At high temperatures, which is inevitable in nanoscale high density circuitries, the conventional device models may exhibit their limitations and hence bound to deviate from the observed data. This aspect needs to be investigated by developing temperature dependent FinFETs models and their validity at the end of day with experimental data, to establish a complete understanding of the device performance.

2. In Chapter-3, a unified depletion–inversion model for heterojunction trigate FinFETs DC characteristics was developed and the same was tested for FinFETs having $L_g = 5$ μm to 100 nm. Its validity for devices having $L_g < 100$ nm would be an exciting challenge, which may require certain

modifications in the developed model and the same could be carried out as one of the future extension of this research.

3. In FinFETs, the gate length (L_g) of the device plays a crucial role in defining the response of the device. As a rule of thumb, reduction in gate length enhances the high frequency operation of the device. However, this reduction requires an appropriate scaling of other associated physical parameters of the device such as fin height (H_{fin}), fin thickness (T_{fin}), fin width (W_{fin}), fin length (L_{fin}), oxide thickness (T_{ox}) etc. A comprehensive parametric studies to assess the effect of each of these upon other variables, will help in determining an optimum device having high transconductance, high unity gain frequency with minimum short channel effects.

4. The mathematical formulation carried out in this research is restricted to the DC performance of the device. A next logical step to extend this work would be to establish AC characteristics of these FinFETs and then to extract scattering parameters of the device for comparison with experimental AC data to have improved understanding of the device AC response.

5. A machine learning technique developed in this study has successfully predicted the device characteristics. However, it was noted that in some cases (less than 5%) the prediction accuracy was not within acceptable range. Hence there is a room to improve the developed technique by incorporating more layers or/and by enhancing the number of neurons of a layer along with other design variables. Additionally, the prediction carried out in this thesis is only for the device DC characteristics, it is therefore, recommended that an appropriate AC dataset can also be generated and a modified DNN may be trained using both AC and DC characteristics to generate full range of characteristics either two independent systems or a single system incorporated with both types of characteristics.

6. The machine learning demonstration has been formulated that works on FinFETs DC characteristics by engaging its physical parameters. The proposed DNN model can be altered to anticipate heterostructure, nanowires,

nanosheets, vertically stacked 3D devices etc. Consequently it can safely be said that, the proposed technique is a flexible one to be adopted for a variety of electronic devices provided the model is trained accordingly.

7. In mobile applications, battery life is treated to be an important feature in determining the usefulness of a product. The battery life heavily depends upon the magnitude of off-state current drawn by a circuitry. In case of FinFETs based circuitry, this off-state current defines sub-threshold characteristics of a FinFET. Ideally, in sub-threshold region the current drawn by the device should be zero. To bring the device off-state current closer to ideal value, the sub-threshold performance requires to be enhanced by improving the wafer as well as by optimizing the device geometry. So the device geometry dependent sub-threshold characteristics model will then be a useful tool to enhance the device performance and the same will provide a beneficial knowledge for industrial applications and fundamental understanding of the device.

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